HARD DISK CONTROLLER
SINGLE CHIP AT-WINCHESTER CONTROLLER

■ DESCRIPTION

The SPC3010 is a single chip disk drive controller designed for high performance. Combined with a data separator, ENDEC, and microcontroller, this chip will support the functions necessary to build a high performance disk drive. It is packaged in a 100 pin quad flat package and contains the data sequencer, bus interface, and buffer manager. It will support disk data rates up to 24 mbits per second and 16 bit host data transfers up to 10 mword per second. Included is a 4K byte buffer to accommodate smaller foot print disk drives. The SPC3010 can control an additional 128K bytes of SRAM. This device incorporates Servo Gap Skip Circuitry to support zone bit recording.

■ FEATURES

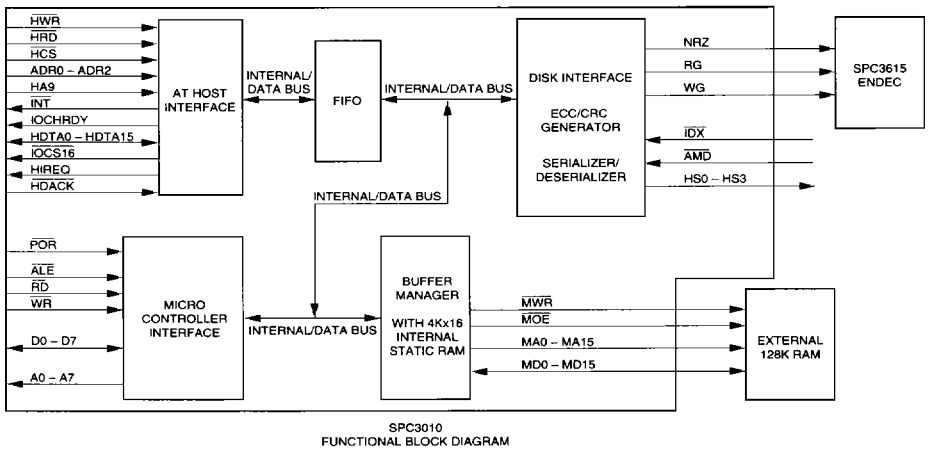
○ Enhanced Host Interface
- Compatible with PC/AT and compatible products
- 24 mA output drivers connects directly to PC/AT Bus
- Provides selectable DMA or PIO transfers in all host modes
- Supports PC/AT 16MHz zero wait states
- Implements fast command decode logic
- Allows two daisy chained embedded drives

○ Advanced Buffer Manager
- Supports 1:1 Interleave
- Internal 16 bit data path for all I/O and memory accesses
- Internal static RAM 2K x 16 bits wide eliminates the need for external buffer
- Supports external static RAM up to 128K x 16 bits wide
- Sustained RAM bandwidth of 20 Mbytes/sec
- Allows full track buffering and facilitates look ahead cacheing algorithms

○ Microcontroller Interface
- Automatically detects either 80XX or 68XX type microcontrollers
- Internal ROM address latch to reduce part count
- Multiplexed Address/Data Bus reduce pin count
- Interrupt driven or Programmed I/O interface
- Programmable low power mode (standby operation)

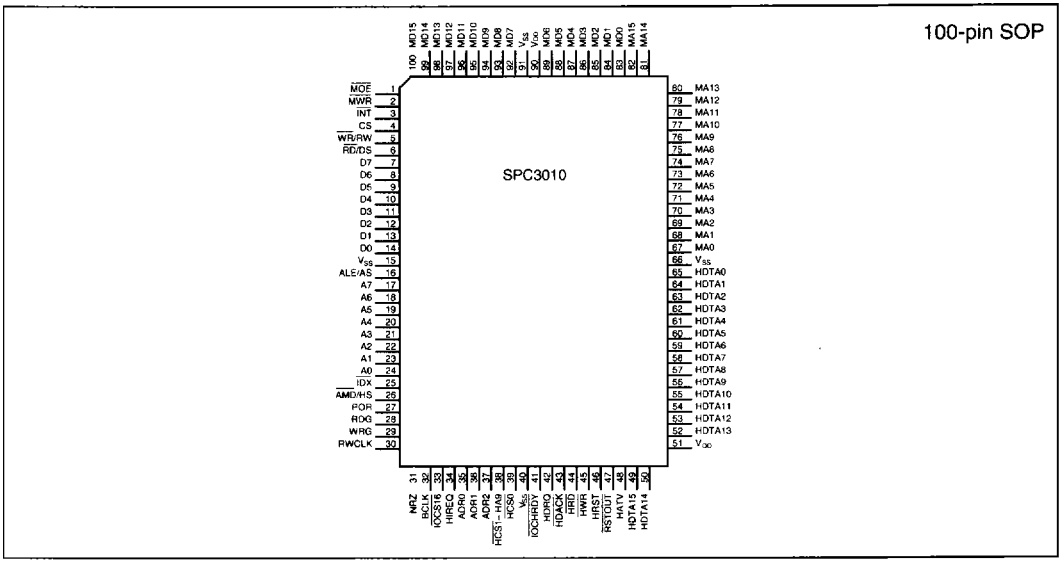
○ Advanced Disk Interface
- Supports NRZ data rates up to 24 Mbits/sec.
- Supports both hard and soft sector formats
- Supports sustained 1:1 interleave operation
- Supports multiple sector transfers
- User programmable sector length up to 64K bytes per sector
- Selectable 32, 48 and 56 bit ECC polynomials
- Hardware generated syndrome and offset data for fast error correction
- Supports zone bit recording with servo area skip capabilities
- Interfaces to most industry standard ENDEC's

■ BLOCK DIAGRAM



SPC3010
FUNCTIONAL BLOCK DIAGRAM

■ PIN DIAGRAM



■ PIN DEFINITIONS

○ Microcontroller Interface

Pin Name	Pin #	Signal Name	I/O	Function
D0–D7	14–7	ADDRESS DATA	I/O	UP multiplexed address/data bus used to load the register buffer address on the falling edge of ALE; used for data transfers between the local microcontroller
ALE/AS	16	ADDRESS LATCH ENABLE/ ADDRESS STROBE	I	ALE is used to latch the lower eight bits of the multiplexed address/data lines (AD0-AD7). AS is used for this function when tied to a 68XX type UP.
$\overline{WR}$/RW	5	UP WRITE ENABLE/ UP READ/WRITE	I	Active low input: asserted by the UP to write a register or the buffer; also used by 68XX type UP's to set the direction of data transfers.
$\overline{RD}$/DS	6	UP READ ENABLE/ UP DATA STROBE	I	Active low input: asserted by the UP to read a register or the buffer; also used in 68XX type UP's to enable data transfers.
A0–A7	24–17	LATCHED ADDRESS	O	Internal address latch output: used to eliminate an external address latch.
$\overline{INT}$	3	INTERRUPT	O	Active low output: used by UP to signal when it is necessary to check command parameters or status.
$\overline{RSTOUT}$	47	RESET	O	Active low output: used to reset the microcontroller
$\overline{CS}$	4	CHIP SELECT	I	Active low input: used by the UP to enable of internal the selection registers

NOTE: UP is used in place of microcontroller

○ Buffer Extension

Pin Name	Pin #	Signal Name	I/O	Function
MD0–MD15	83–89 92-100	BUFFER MEMORY DATA BUS	I/O	Used to transfer data to and from the external buffer
MA0–MA15	67–82	BUFFER MEMORY ADDRESS BUS	O	Used to address external memory and address bits MA12–MA15 can be programmed as Head select bits (HS0–HS3).
$\overline{MWR}$	2	BUFFER MEMORY WRITE ENABLE	O	Active low output: asserted low when a buffer write operation is active.
$\overline{MOE}$	1	BUFFER MEMORY OUTPUT ENABLE	O	Active low output: asserted low when a buffer read operation is active.

o Host Interface

Pin Name	Pin #	Signal Name	I/O	Function
ADR0–ADR2	35–37	HOST ADDRESS BUS	I	Used to access host interface register set
$\overline{\text{HCS1}}$/ADR9	38	HOST CHIP SELECT1/ HOST ADDRESS BIT A9	I	Active low programmable input via internal Mode register Doubles as Host chip select and high order address bit.
$\overline{\text{HCS0}}$	39	HOST CHIP SELECT0	I	Active low input: used to select host internal register set.
$\overline{\text{HWR}}$	43	HOST WRITE ENABLE	I	Active low input: used by the host to write to internal register set.
$\overline{\text{HRD}}$	44	HOST READ ENABLE	I	Active low input: used by the host to read to internal register set.
$\overline{\text{IOCS16}}$	33	I/O CHIP SELECT	O	Active low output: indicates that a 16-bit buffer transfer is active on the AT bus.
HRST	46	MASTER RESET	I	Active high input: when asserted initializes internal control and status registers; all commands are aborted.
HDTA0– HDTA15	65–52, 50, 49	HOST DATA BUS	I/O	Operates in 16 bit mode during data transfers to and from the sector buffer and 8 bit mode for commands, status and ECC byte accesses.
HIREQ	34	HOST INTERRUPT REQUEST	O	Active high output: used by the host to signal when the controller needs attention
$\overline{\text{IOCHRDY}}$	42	I/O CHANNEL READY	O	Active low output: asserted when controller needs to extend host transfer time.
HDRQ	42	HOST DATA REQUEST	O	Active high output: asserted during DMA operation to signal when data is ready to transfer.
$\overline{\text{HDACK}}$	43	HOST TRANSFER ACKNOWLEDGE	I	Active low input: asserted by the host during DMA transfers in response to HDRQ.

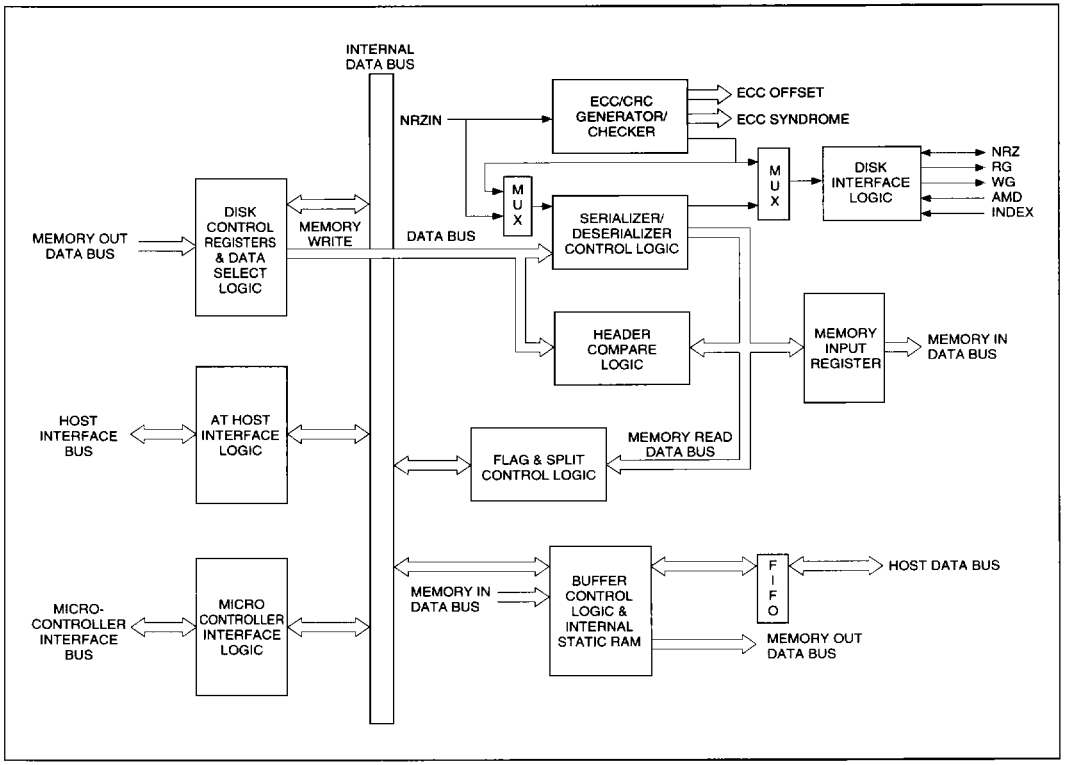
o Read/Write Sequencer

Pin Name	Pin #	Signal Name	I/O	Function
NRZ	31	NON RETURN TO ZERO	I/O	Serial input/output data qualified by RDG for Reads and WRG for Writes.
WRG	29	WRITE GATE	O	Active high output: used to qualify Valid write data from the drive.
RDG	28	READ GATE	O	Active high output: used to qualify Valid read data from the drive.
$\overline{\text{AMD}}$/HS	26	ADDRESS MARK DETECT	I	Active low input: used to signal the controller that an has been address mark detected from the drive.
RWCLK	30	Read Ref Clock	I	Used to synchronize incoming NRZ data.

o Miscellaneous

Pin Name	Pin #	Signal Name	I/O	Function
HATV	48	CONTROLLER BUSY/ SECOND CONTROLLER AVAILABLE	I/O	Used as controller busy signal to drive external LED; also used to indicate when a second disk is available.
BCLK	32	BUFFER SEQUENCE CLOCK	I	Used to control internal buffer control timing.
$\overline{\text{POR}}$	27	POWER ON RESET	I	Initializes all internal logic on power up.
$\overline{\text{IDX}}$	25	INDEX	I	Active low input: the INDEX pulse is a reference signal supplied by the drive.
Vcc	51, 90	INPUT POWER	PWR	+5 Volts DC
Vss	15, 40, 66, 91	GROUND	GND	Digital Ground

■ FUNCTIONAL BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Item	Rating	Unit
V_{DD} with respect to Vss (ground)	+5 ± 5%	V
Max voltage on any pin with respect to Vss	-0.5 to 5.5	V
Operating temperature (T_A)	0 to 70	°C
Storage temperature	55 to 125	°C

NOTE: Maximum limits where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

● DC Characteristics

V_{DD}=5V±10%, V_{SS}=0° to 70°C

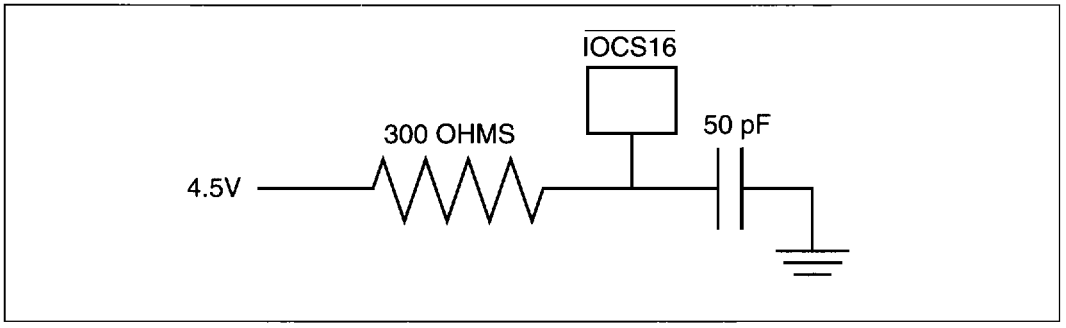
Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Input leakage	I_{IL}	V_{IN}=0.4 to V_{DD}			±10	µA
Tri-state and open drain output leakage	I_{OZ}	V_{OUT}=0.4 to V_{DD}			±10	µA
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OUT}=–800µA	2.4			V
Output Low Voltage	V_{OL1}	I_{OUT}=2.0mA			0.4	V
Output Low Voltage	V_{OL2}	I_{OUT2}=24.0mA			0.5	V
Supply Current	I_{CC}	All outputs open			50	mA
Supply Current (Standby Mode)	I_{CCS}	All inputs at V_{DD} or V_{SS}, disk controller sleep mode			20	µA

● AC Characteristics

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Input leakage	I_{IL}	V_{IN}=0.4 to V_{DD}			±10	µA

NOTE: Load capacitance = 50 pF each for all other outputs. Timings must be derated for larger load capacitances.

● Test Circuit

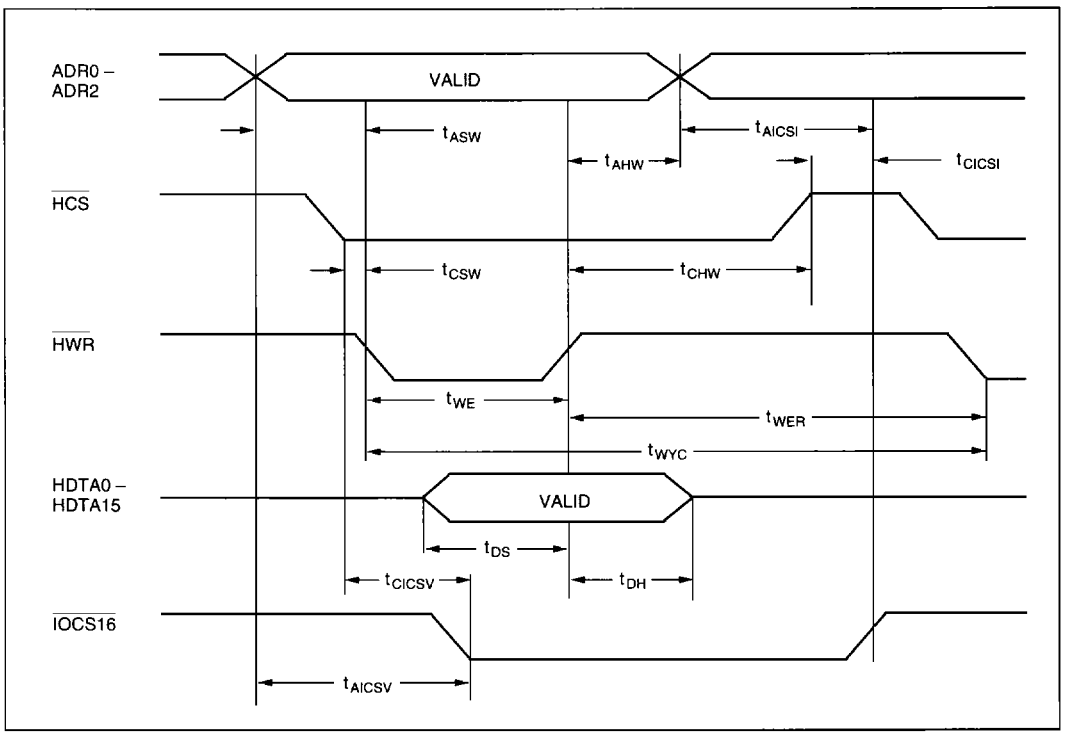


NOTE: A write occurs during the overlap of $\overline{HCS}$ and $\overline{HWR}$.

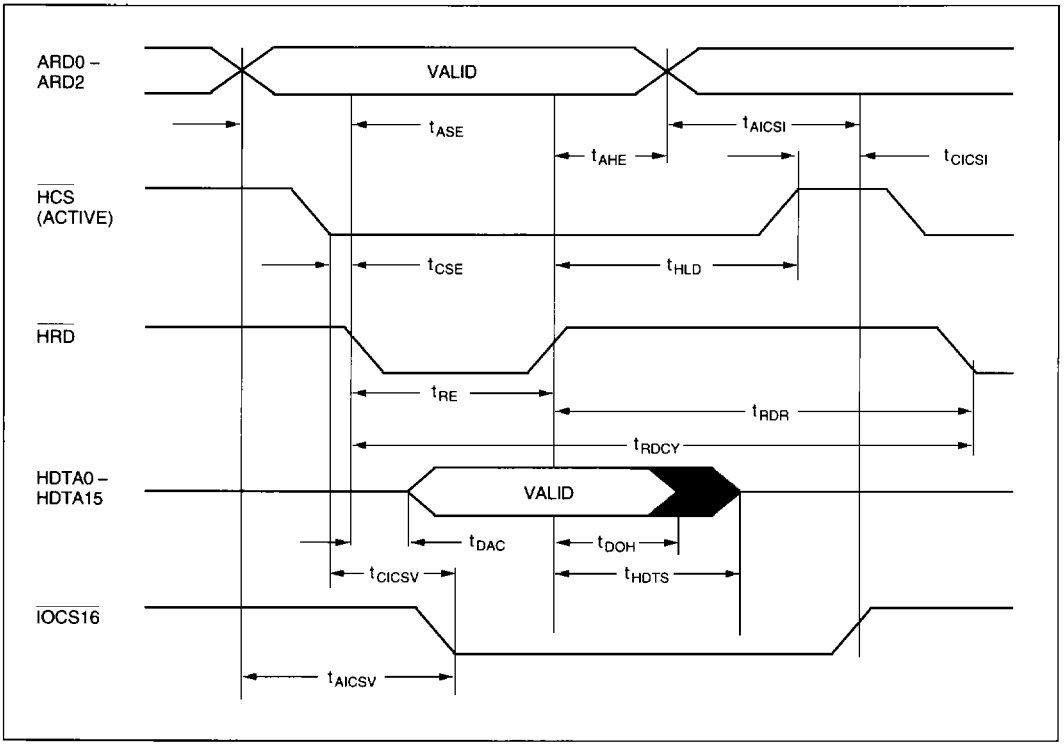
● **Host Programmed I/O Write Timing**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Address Setup to $\overline{HWR}$ Low	tASW		0			ns
$\overline{HCS}$ Setup to $\overline{HWR}$ Low	tCSW		30			ns
Data Setup to $\overline{HWR}$ High	tDS		40			ns
$\overline{HWR}$ Pulse Width	tWE		80			ns
Data Setup to $\overline{HWR}$ High	tDS		40			ns
Data Hold From $\overline{HWR}$ High	tDH		10			ns
Address Hold From $\overline{HWR}$ High	tAHW		10			ns
$\overline{HCS}$ Hold From $\overline{HWR}$ High	tCHW		10			ns
$\overline{HCS}$ and $\overline{HWR}$ Inactive	tWER		20			ns
Write Cycle Time	tWCY		120			ns
$\overline{IOCS16}$ Valid from $\overline{HCS}$	tCICSV				20	ns
$\overline{IOCS16}$ Valid from Address	tAICSV				20	ns
$\overline{IOCS16}$ Inactive from $\overline{HCS}$	tCICSI	Test Circuit 1			30	ns
$\overline{IOCS16}$ Inactive from Address	tAICSI	Test Circuit 1			45	ns

● **Host Programmed I/O Write Timing**



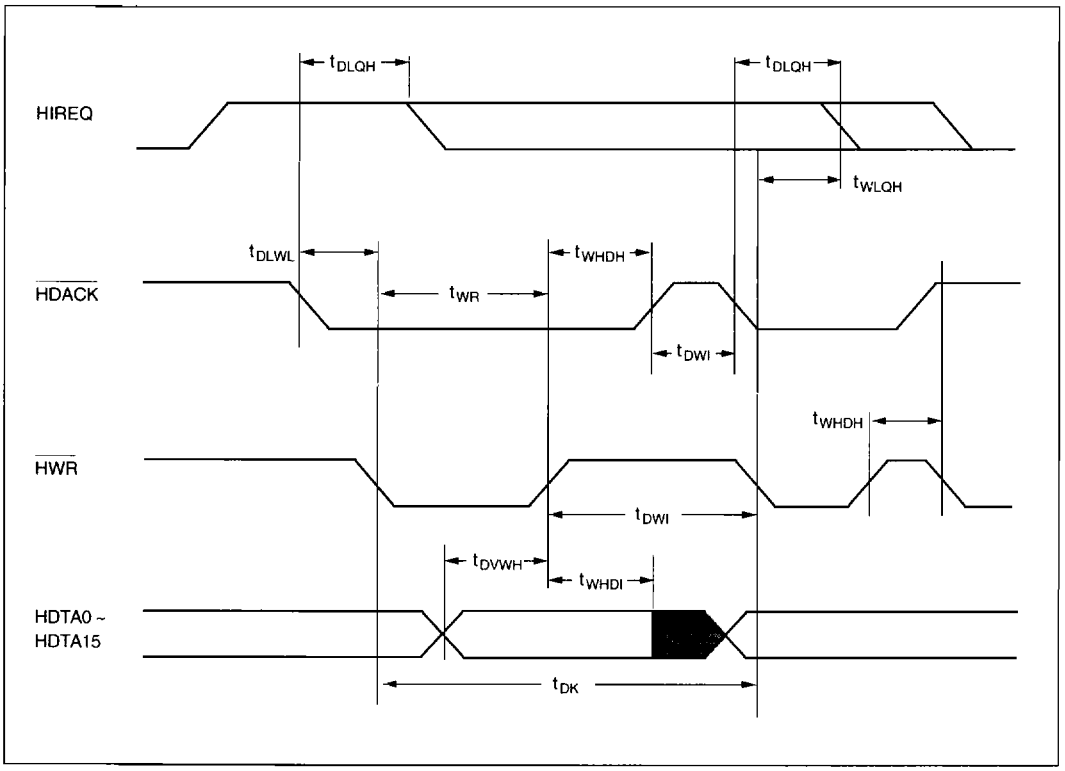
● **At Host Programmed I/O Read Timing**



● **At Host Programmed I/O Read Timing**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Address Setup to HRD Low	tASE		0			ns
HCS Setup to HRD Low	tCSE		30			ns
Data Valid From HRD Low	tDAC				60	ns
HRD Pulse Width	tRE		80			ns
Data Hold From HRD High	tDOH		5			ns
Data Tri-State From HRD	tHDTS				30	ns
Address, HCS Hold From HRD High	tHLD		10			ns
HCS and HRD Inactive	tRDR		20			ns
Read Cycle Time	tRDCY		120			ns
IOCS16 Valid from HCS	tCICSV				20	ns
IOCS16 Valid from Address	tAICSV				20	ns
IOCS16 Inactive from HCS	tCICSI	Test Circuit 1			30	ns
IOCS16 Inactive from Address	tAICSI	Test Circuit 1			45	ns

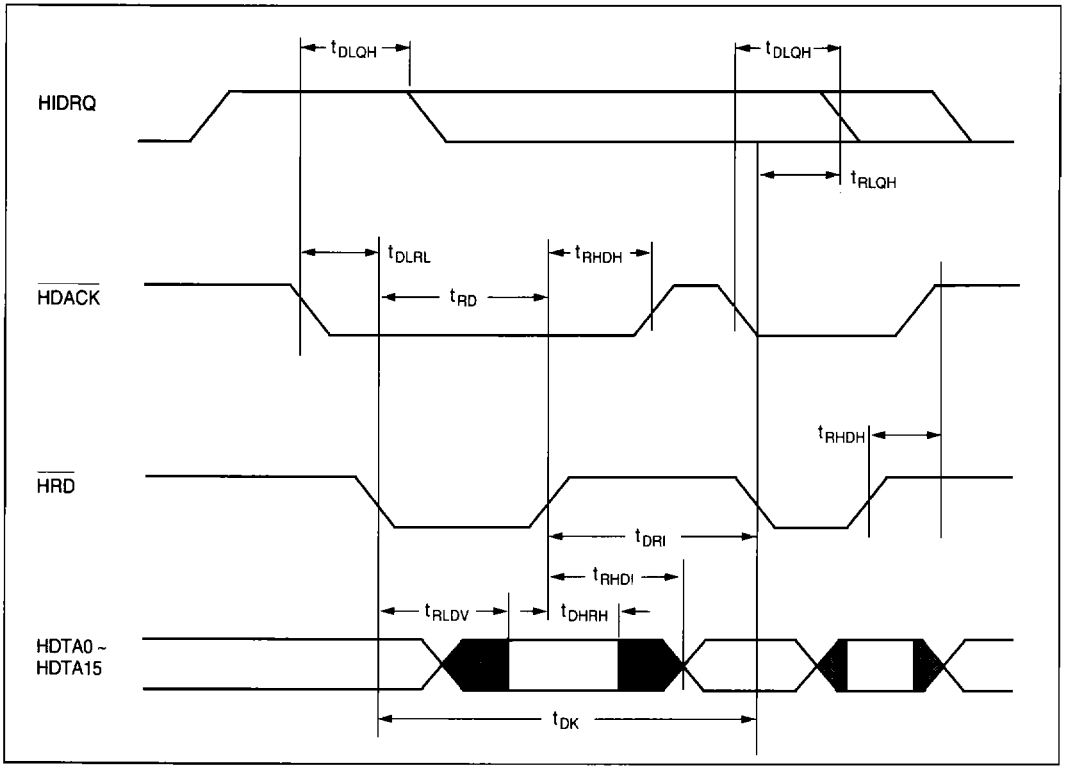
- **At Host DMA Write Timing**



- **At Host DMA Write Timing**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
$\overline{\text{HDACK}}$ Low to $\overline{\text{HIREQ}}$ Low	t_{DLQH}				60	ns
$\overline{\text{HWR}}$ Low to $\overline{\text{HIREQ}}$ Low	t_{WLQH}				60	ns
$\overline{\text{HWR}}$ High to $\overline{\text{HIREQ}}$ Low	t_{WHQH}					ns
DMA Cycle	t_{DK}		100			ns
$\overline{\text{HDACK}}$ Low to $\overline{\text{HRW}}$ Low	t_{DLWL}		10			ns
$\overline{\text{HRW}}$ Pulse Width	t_{WR}	$t_{DLWL} \geq 20$	80			ns
Data Valid From $\overline{\text{HWR}}$ High	t_{DVWH}		20			ns
$\overline{\text{HWR}}$ High to $\overline{\text{HDACK}}$ High	t_{WHDH}		10			ns
$\overline{\text{HWR}}$ High to Data Invalid	t_{WHDI}		10			ns
$\overline{\text{HDACK}}$ and $\overline{\text{HWR}}$ Inactive	t_{DWI}		20			ns

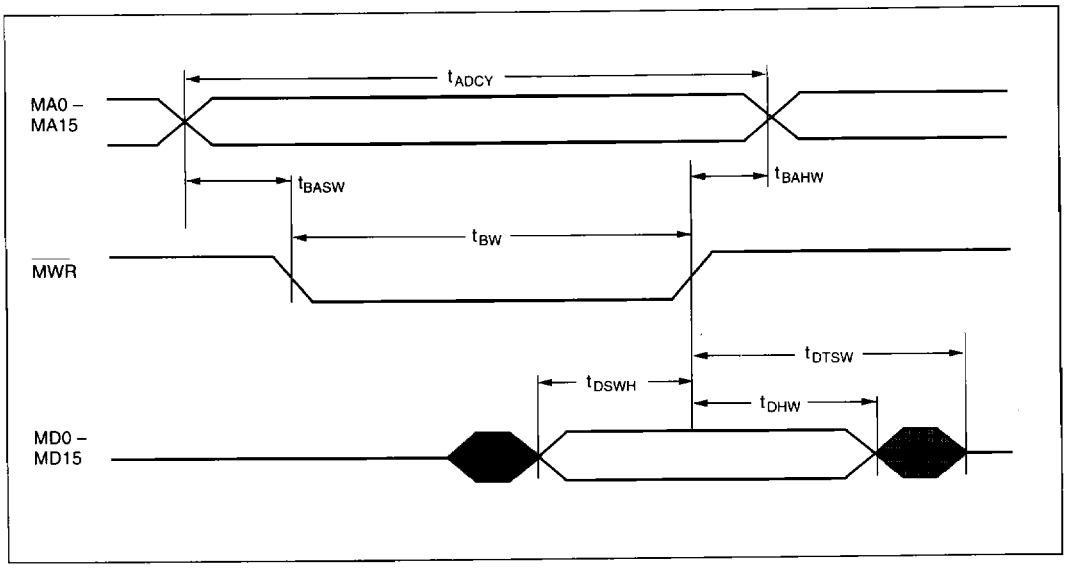
● **At Host DMA Read Timing**



● **At Host DMA Read Timing**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
HDACK Low to HIREQ Low	tDLQH				60	ns
HWR Low to HIREQ Low	tRLQH				60	ns
HRD High to HIREQ Low	tRHQH				100	ns
DMA Cycle	tDK		100			ns
HDACK Low to HRD Low	tDLRL		10			ns
HRD Pulse Width	tRD	tDLWL ≥ 20	80			ns
HRD Low to Data Valid	tRLDV				50	ns
HRD High to HDACK High	tRHDH		10			ns
Data Hold From HRE High	tDHRH		5			ns
HRE High to Data Tri-state	tRHDI				30	ns
HDACK and HRD Inactive	tDRI		20			ns

● **Buffer RAM Write Timing**



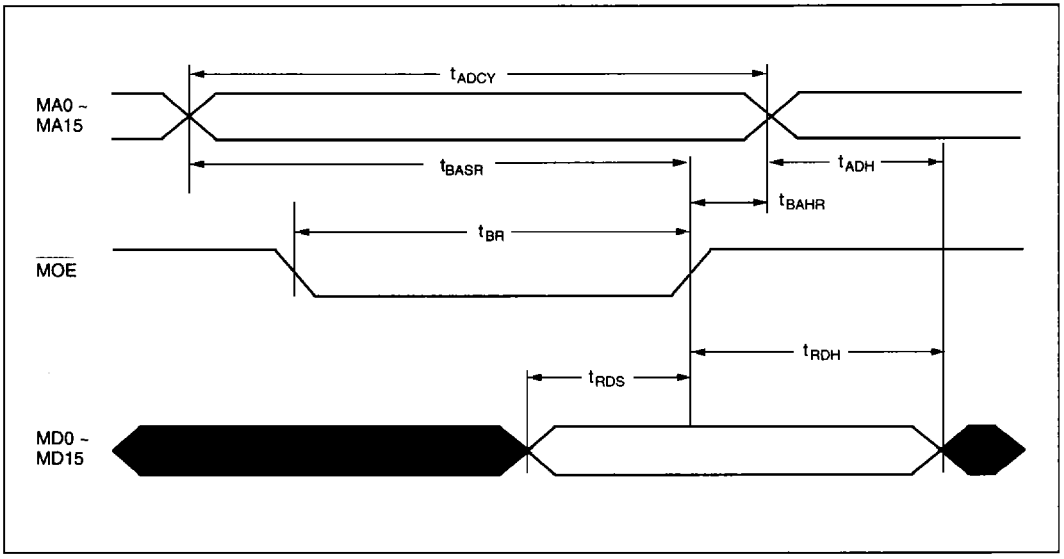
● **Buffer RAM Write Timing**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Address Cycle Time	tADCY				tmc*	ns
Address Setup to $\overline{\text{MWR}}$ Low	tBASW				tmc/2	ns
$\overline{\text{MWR}}$ Pulse Width	tBW				tmc/2	ns
Address Hold From $\overline{\text{MWR}}$ High	tBAHW		0			ns
Data Valid to $\overline{\text{MWR}}$ High	tDSWH				tmc/2	ns
Data Hold From $\overline{\text{MWR}}$ High	tDHW		0			ns

NOTE: 100-pin QFP5

* tmc = Period of B clock or B clock/2, if BhLf is set in Buffer Control Register (08)

● **Buffer RAM Read Timing**

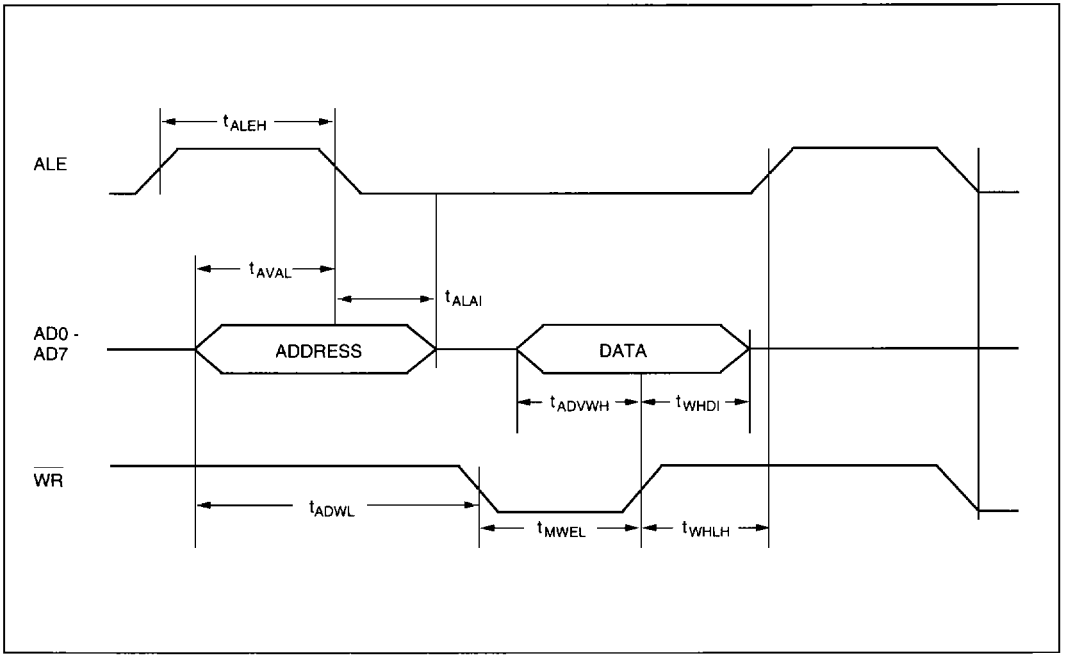


● **Buffer RAM Read Timing**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Address Cycle Time	tADCY				tmc*	ns
Address Setup to $\overline{MOE}$ High	tBASR				tmc/2	ns
$\overline{MOE}$ Pulse Width	tBR				tmc/2	ns
Address Hold From $\overline{MOE}$ High	tBAHR		0			ns
Data Setup to $\overline{MOE}$ High	tRDS		0		tmc/2	ns
Data Hold From Address	tDHW		0			ns

* tmc = Period of B clock or B clock/2, if BhLf is set in Buffer Control Register (08)

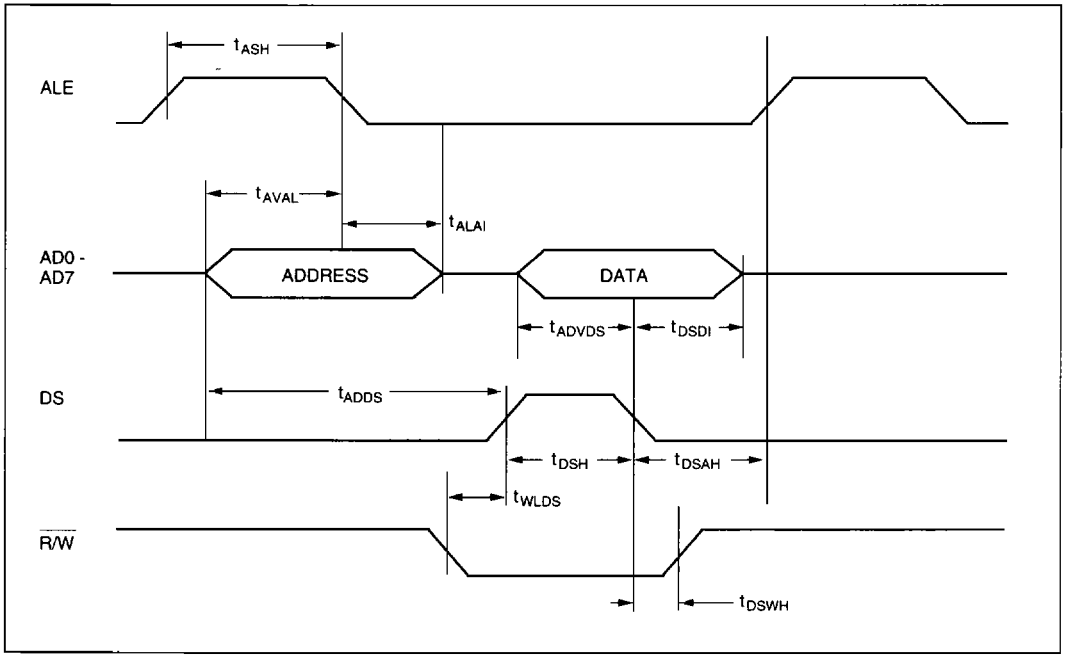
- **Microprocessor Write Timing (Intel Bus)**



- **Microprocessor Write Timing (Intel Bus)**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Address Setup to $\overline{ALE}$ Low	tAVAL		5			ns
Address Hold From $\overline{ALE}$ Low	tALAI		5			ns
$\overline{ALE}$ High Pulse Width	tALEH		20			ns
Data Setup to $\overline{WR}$ High	tADVWH		20			ns
Data Hold From $\overline{WR}$ High	tWHDI		10			ns
$\overline{WR}$ Low Pulse Width	tMWEL		50			ns
Address Valid From $\overline{WR}$ Low	tADWL		15			ns
$\overline{WR}$ High to $\overline{ALE}$ High	tWHLH		10			ns

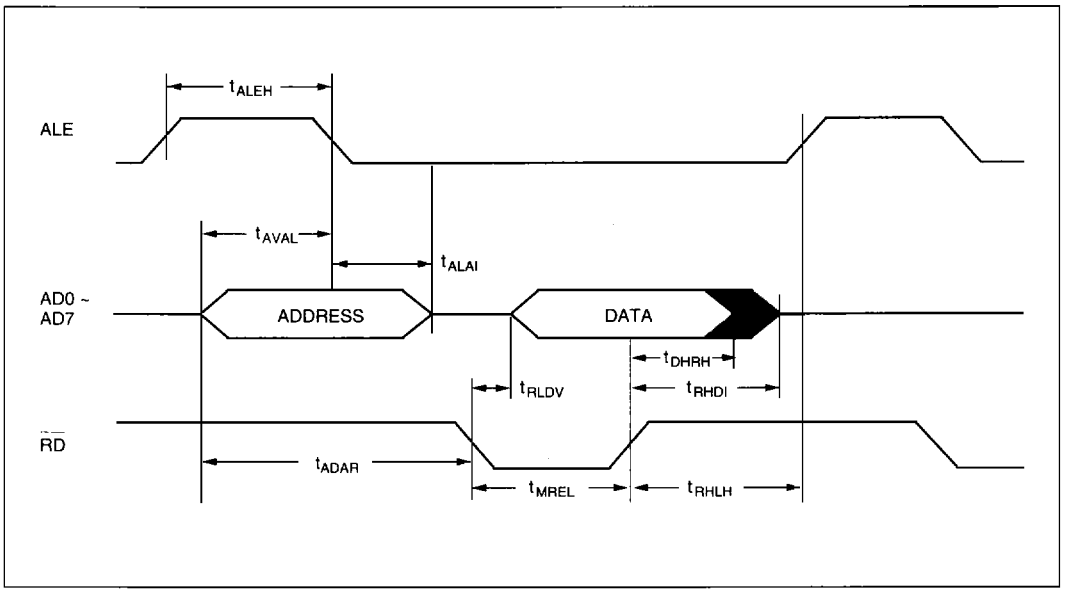
● **Microprocessor Write Timing (Motorola Bus)**



● **Microprocessor Write Timing (Motorola Bus)**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Address Setup to AS Low	tAVAL		15			ns
Address Hold From AS	tALAI		5			ns
AS High Pulse Width	tASH		30			ns
Data Setup to DS Low	tADVDS		50			ns
Data Hold From DS Low	tDSDI		5			ns
DS High Pulse Width During Write	tDSH		75			ns
R/W Low to DS High	tWLDS		5			ns
DS Low to R/W High	tDSWH		20			ns
Address High to DS High	tADDS		55			ns
DS Low to AS High	tDSAH		10			ns

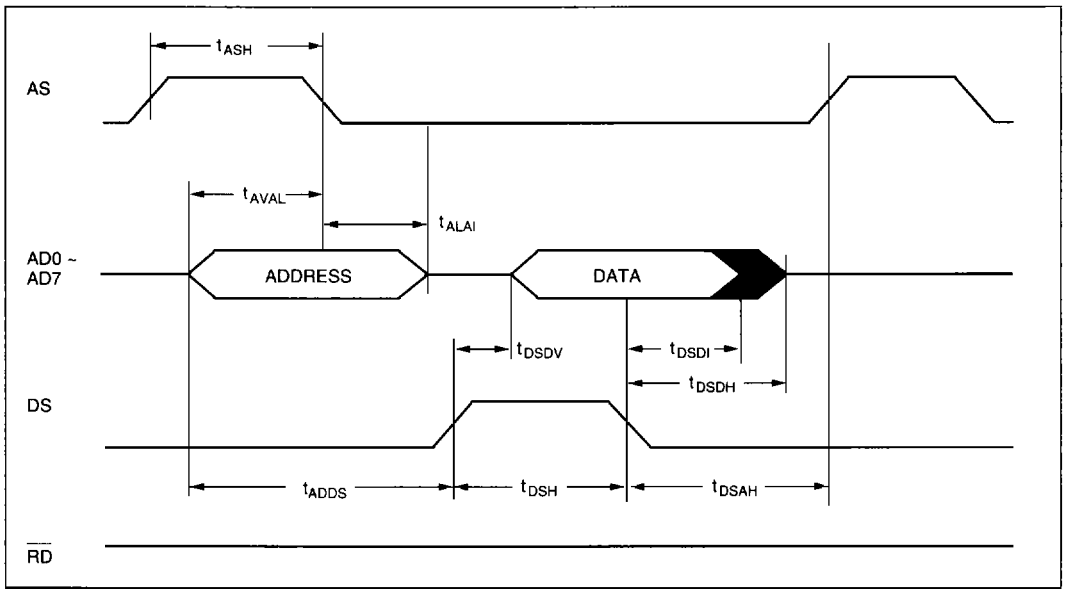
● **Microprocessor Read Timing (Intel Bus)**



● **Microprocessor Read Timing (Intel Bus)**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Address Setup to ALE Low	tAVAL		5			ns
Address Hold From ALE Low	tALAI		5			ns
ALE High Pulse Width	tALEH		20			ns
Data Valid $\overline{RD}$ Low	tRLDV		40			ns
Data Hold From $\overline{RD}$ High	tDHRH		0			ns
Data Tri-state from $\overline{RD}$ High	tRHDI		15			ns
$\overline{RD}$ Low Pulse Width	tMREL		60			ns
Address Valid to $\overline{MRE}$ Low	tADAR		15			ns
$\overline{RD}$ High to ALE High	tRHLH		10			ns

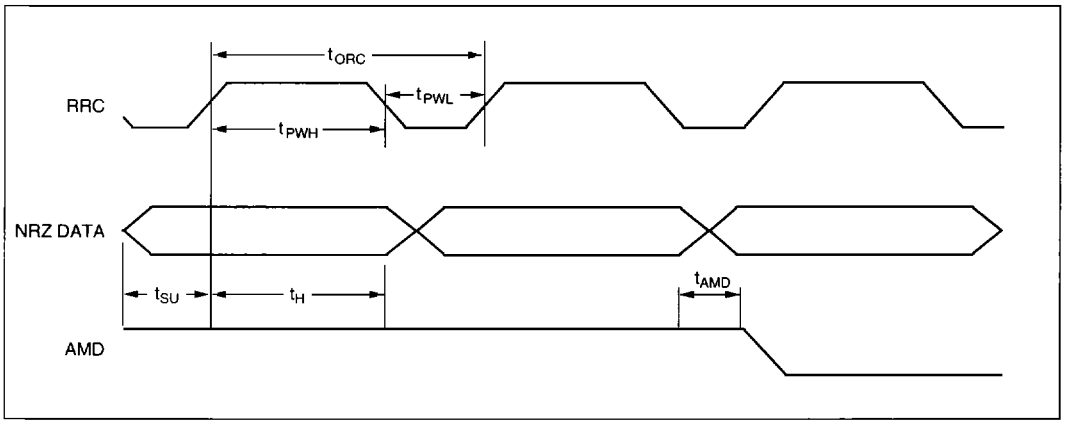
● **Microprocessor Read Timing (Motorola Bus)**



● **Microprocessor Read Timing (Motorola Bus)**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Address Setup to AS Low	tAVAL		15			ns
Address Hold From AS Low	tALAI		5			ns
AS High Pulse Width	tASH		30			ns
Data Valid From DS High	tDSDV				100	ns
Data Tri-state from DS Low	tDSDI				50	ns
DS High Pulse Width During Read	tDSH		100			ns
Address Valid to DS High	tADDS		55			ns
DS Low to AS High	tDSAH		10			ns

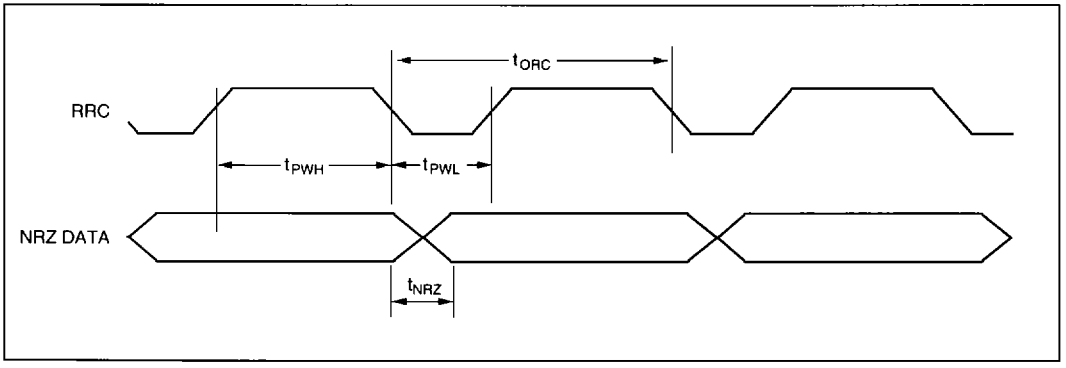
● **NRZ Read Timing**



● **NRZ Read Timing**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Positive Pulse Width	tPWH		12			ns
Negative Pulse Width	tPWL		12			ns
NRZ to RRC Set Up Time	tSU		10			ns
NRZ to RRC Hold Time	tH		0			ns
Negative Edge of RRC to AMD true	tAMD		10			ns

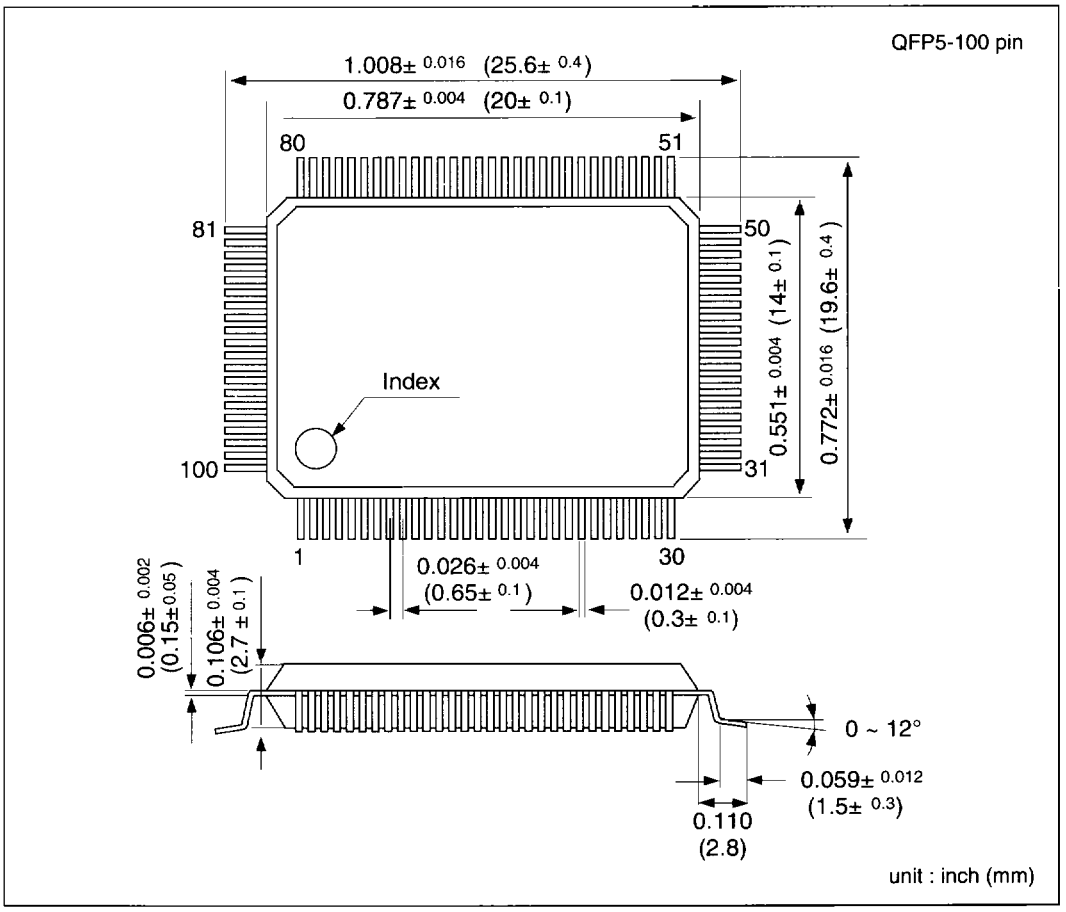
● **NRZ Write Timing**



● **NRZ Write Timing**

Item	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Negative Edge of RRC to NRZ true	tNRZ				12	ns
RRC Period	tORC		24			MHz

■ PACKAGE DIMENSIONS



■ TECHNICAL SUPPORT

● IDE Interface Pinout

Pin Number	Signal	Pin Number	Signal
01	/HOST RESET	21	RESERVED
02	GND	22	GND
03	/HOST DATA 7	23	/HOST IOW
04	/HOST DATA 8	24	GND
05	/HOST DATA 6	25	/HOST IOR
06	/HOST DATA 9	26	GND
07	/HOST DATA 5	27	RESERVED
08	/HOST DATA 10	28	/HOST ALE
09	/HOST DATA 4	29	RESERVED
10	/HOST DATA 11	30	GND
11	/HOST DATA 3	31	/HOST IRQ14
12	/HOST DATA 12	32	/HOST IO16
13	/HOST DATA 2	33	/HOST ADDR 1
14	/HOST DATA 13	34	/HOST PDIAG
15	/HOST DATA 1	35	/HOST ADDR 0
16	/HOST DATA 14	36	/HOST ADDR 2
17	/HOST DATA 0	37	/HOST CS0
18	/HOST DATA 15	38	/HOST CS1
19	GND	39	/HOST SLV/ACT
20	KEY	40	GND

Comprehensive Support Tools:

S-MOS Systems provides to the system designer a complete set of resources and tools for the development of hard disk controllers.

Evaluation/Demonstration Board:

- Assembled and fully tested SPC3010 Eval PCB
- Schematic of Evaluation/Demo board
- Parts List
- Device Data Sheets
- Application Notes

Firmware:

- BIOS on EPROM or Floppy

Application Engineering Support:

In order to help customers implement the SPC3010 in their design, S-MOS offers training, technical support, and the following services:

- Technical Support
- Design Assistance
- Applications Notes
- Technical Bulletins
- Text or Drawing Support
- Consultant Referral