VITESSE

VSC6424
Data Sheet

500Mb/s Video Shift Register IC

FEATURES

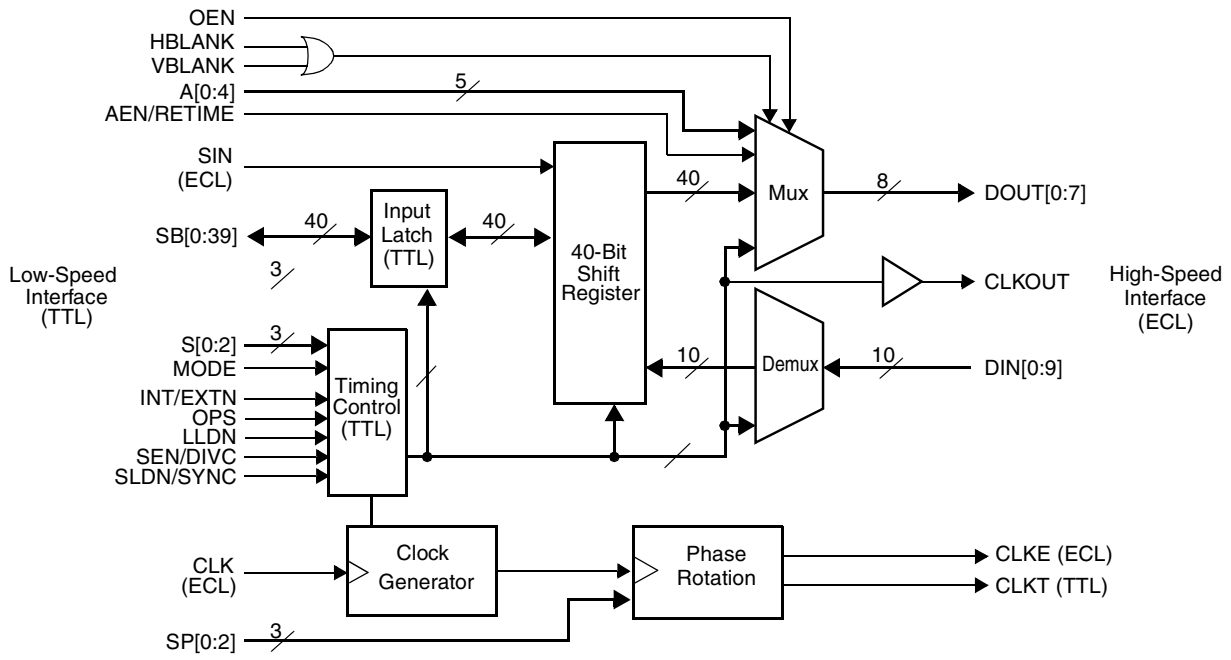
- Multiplex or Demultiplex Operation
- Selectable Shift Register Length
- 500Mb/s Operation Using Internal Timing
- 250Mb/s Operation Using External Timing
- Functional Replacement for Bt424
- External ECL Reference Voltage: –1.32V
- ECL I/Os for High-Speed Interface and TTL I/Os for Low-Speed Interface
- Power Supplies: +3.3V and –2V
- Maximum Power Dissipation: 2.7 Watts
- Temperature Range: 0°C to +70°C
- Package: 128-pin PQFP, 14mm x 20mm

GENERAL DESCRIPTION

The VSC6424 is a 500Mb/s video shift register IC based on a 40-bit user-configured shift register. The shift register may be used either as a multiplexer (parallel in, serial out) or as a demultiplexer (serial in, parallel out). The VSC6424 can be configured into one of following shift register modes: eight 5-bit, eight 4-bit, five 8-bit, four 10-bit, two 16-bit, two 20-bit, one 32-bit, or one 40-bit. See Table 1 on page 2.

The VSC6424 is available in a 128-pin, 14mm x 20mm PQFP package with an exposed heat spreader.

VSC6424 Block Diagram



FUNCTIONAL DESCRIPTION

The VSC6424 is a 40-bit user-configurable shift register designed to provide general-purpose serialization or de-serialization for high-speed designs. The VSC6424 provides both multiplexer (Mux) and demultiplexer (Demux) operations in a single package. With the ability to generate timing signals internally or have them provided externally the VSC6424 maintains the highest design flexibility.

The low-speed signals (parallel data, configuration, and external timing) use a TTL interface and the high-speed signals (serial data and high-speed clock) use an ECL interface. Two power supplies are utilized, +3.3V and –2V, with dissipation of a 2.7 Watts maximum. A –1.32V external reference voltage is required for the ECL interface.

Shift Register Mode Selection

The shift register can be set up to function as a multiplexer or as a demultiplexer, with the MODE pin controlling the direction of operation. The select pins, S[0:2], put the shift register in one of eight configurations shown in Table 1.

Table 1. Mode of Operation

S2	S1	S0	Multiplexer MODE = 0	Demultiplexer MODE = 1
0	0	0	8 4:1	10 1:4
0	0	1	8 5:1	8 1:5
0	1	0	5 8:1	5 1:8
0	1	1	4 10:1	4 1:10
1	0	0	2 16:1	2 1:16
1	0	1	2 20:1	2 1:20
1	1	0	1 32:1	1 1:32
1	1	1	1 40:1	1 1:40

Internal Timing

The VSC6424 can be set up to use either internal or external timing sources. The VSC6424 contains an internal timing generator that provides load and output rates, depending on the modulus selected for the shift register. The timing generator takes an external high-speed differential clock (CLK).

NOTE: *Internal timing mode must be used for designs above 250MHz.*

The internal timing generator also provides two low-speed clock outputs, CLKT (TTL) and CLKE (ECL). The low-speed clock is brought out so that other ICs can use this to latch the low-speed data while in Demux mode. The slow-speed clock output can be the same as the internal clock, or one-half the internal frequency by setting DIVC HIGH. These outputs can also be shifted in 45 degree increments, using the phase select pins, SP[0:2], to allow compensation for trace delays on the board. Phase rotation is not available in divide-by-5 or divide-by-10 modes.

The internal high-speed clock is also brought out to the differential ECL output, CLKOUT. This output is provided for clocking of the high-speed data into the next IC.

The output phase shift (OPS) signal gives the capability of selecting which edge of the high-speed clock the DOUT data is synchronized to. When OPS is LOW, DOUT comes out on the rising edge of CLK. When OPS is HIGH, DOUT comes out on the falling edge of CLK. The high-speed output clock, CLKOUT, is not affected by the state of OPS.

External Timing

By setting the INT/EXTN pin LOW to bypass the internal timing generator, the VSC6424 provides an external timing mode as a functional replacement for older designs using the Bt424 (formerly manufactured by BrookTree). The load and shift timing signals are provided through the shift enable (SEN), shift register load control (SLDN), and the latch load control (LLDN) pins.

The VSC6424 has two cycles of propagation delay in multiplexer mode, where the Bt424 only has one. The two cycles provide the ability to control which edge of the output clock the output data is clocked on. If the OPS pin is LOW, the output data (DOUT) is synchronous with the positive edge of CLKOUT, and if OPS is HIGH, the output data is synchronous to the negative edge of CLKOUT. See Figure 6 for a timing diagram with OPS LOW.

The shift register can also be loaded with serial data while in external timing mode by inputting data into the shift register through the serial input (SIN) pin. The data is latched on the rising edge of the CLK while SLDN is HIGH and SEN is LOW. The data is then shifted to the output pins on each clock cycle once SEN is set HIGH.

I/O Mapping

There are ten high-speed ECL data inputs and eight high-speed ECL data outputs. Some configurations of operation do not use all these inputs and outputs. The state of the outputs not being used in a given mode is not guaranteed. Table 2 and Table 3 show how the high-speed bus (DOUT or DIN) maps to the low-speed bus (SB) for a given configuration.

Data is taken and supplied least significant bit (LSB) first. The numbers in Table 2 refer to the data bit on the low-speed bus, SB[0:39]. SB[0:39] are inputs in the Mux mode and outputs in the Demux mode.

Table 2. Mux Mode SB to DOUT Cross Reference

S[2:0]	Modulus	DOUT7	DOUT6	DOUT5	DOUT4	DOUT3	DOUT2	DOUT1	DOUT0
000	8 4:1	28:31	24:27	20:23	16:19	12:15	8:11	4:7	0:3
001	8 5:1	35:39	30:34	25:29	20:24	14:19	10:14	5:9	0:4
010	5 8:1	32:39	24:31		16:23		8:15		0:7
011	4 10:1		30:39		20:29		10:19		0:9
100	2 16:1		24:39				8:23		
101	2 20:1				20:39				0:19
110	1 32:1						0:31		
111	1 40:1								0:39

Table 3. Demux Mode DIN to SB Cross Reference

S[2:0]	Modulus	DIN9	DIN8	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
000	10 1:4	36:39	32:35	28:31	24:27	20:23	16:19	12:15	8:11	4:7	0:3
001	8 1:5	35:39	30:34	25:29		20:24	14:19	10:14		5:9	0:4
010	5 1:8	32:29		24:31		16:23		8:15		0:7	
011	4 1:10	30:39		20:29			10:19			0:9	
100	2 1:16			16:32				0:15			
101	2 1:20	20:39					0:19				
110	1 1:32			0:31							
111	1 1:40	0:39									

Initialization

The VSC6424 requires that the SYNC/SLDN input be LOW for at least one clock cycle after powering up, then be set HIGH for at least one clock period to initialize the device. (This is an edge-sensitive function.) In internal timing mode this serves to start the internal clock dividers and set the shift register and low-speed output clocks in motion. Additional edges, while in internal timing mode, serves to synchronize the output clocks as described below. Once this has been done the device takes 2(n) cycles to stabilize. During this time the slow bus (SB) should be set to 0. The first data is then latched from SB at the end of the 2(n) cycles. The device is now set to run and will latch data from SB every (n) cycles. To determine (n) for a selected modulus, see Table 5 on page 9.

In MUX mode with internal timing, the VSC6424 chip can also be initialized by providing a slow-speed clock to the SYNC input. This slow-speed clock must be synchronized with high-speed clock and based on the modulus that the MUX is set to. For example, if the VSC6424 is set to 4:1 mode and the high-speed clock is set to 500MHz then the SYNC input must be 125MHz. The initialization at power on will still take 2(n) cycles of the high-speed clock, allowing the system to dictate when the slow-speed data is latched and where the shifting begins.

In external timing mode the SLDN/SYNC signal serves to set the shift register in motion once the data has been latched from the slow-speed bus.

Synchronization

In internal timing mode, several VSC6424s can be synchronized together by connecting the slow-speed TTL clock output, CLKT, of a master chip to the synchronization input, SYNC, of a slave chip. The internal timing generator synchronizes to the rising edge of the SYNC input. Given that (n) is the number of high-speed clock cycles for a given modulus mode, synchronization takes two times (n) or 2(n) clock cycles to lock in. If it is necessary to synchronize more than two VSC6424 devices, use the TTL clock output, CLKT, from one chip to drive the SYNC inputs of each of the slave devices. See Figure 1 for a block diagram and Figure 7 for a timing illustration of the synchronization timing of the slave chip. To determine (n) for a selected modulus, see Table 5 on page 9.

In Mux mode, several VSC6424s can also be synchronized by providing a slow-speed clock to the SYNC input on all of the devices. This slow-speed clock must be synchronized with high-speed clock and based on the modulus that the MUX is set to. For example, if the VSC6424 is set to 8:1 mode and the high-speed clock is set to 400MHz, the SYNC input must be 50MHz.

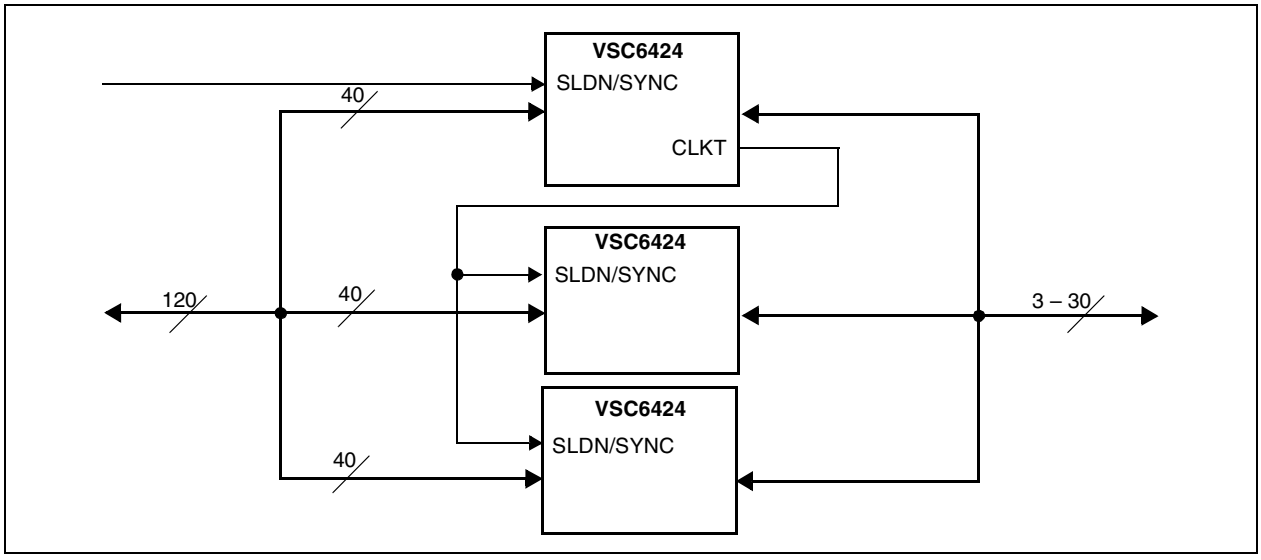


Figure 1. Synchronized VSC6424 Block Diagram

MPU Address Interface

An address interface mode translates TTL-compatible addresses to ECL-compatible output levels and is provided for compatibility with the Bt424. When the address enable signal (AEN) is LOW, data from the address line (A[0:4]) TTL input pins is transferred to the DOUT[0, 2 ,4, 6, 7] ECL output pins with one clock cycle delay. When AEN is HIGH, the A[0:4] inputs are ignored. The DOUT[0:7] data is always synchronized to CLK, regardless of the state of AEN. See Figure 9 on page 10 for a timing illustration of this function.

Video Blanking

The VSC6424 also has a blanking function for video applications. In multiplexer mode, this function allows zeroing of the high-speed outputs (DOUT[0:7]). Setting HBLANK or VBLANK LOW drives all DOUT[0:7] outputs LOW synchronously with CLK. The outputs will be driven LOW on the modulus boundary. The outputs are driven LOW for (n) clock cycles given that (n) is the modulus mode that the chip is set to. See Table 5 on page 9 to determine the value of (n) for a given modulus.

HBLANK or VBLANK must be driven LOW for at least one clock cycle before the desired point of blanking. See Figure 8 on page 10 for a timing illustration of this function.

Retimer

The VSC6424 also contains a retimer function and is enabled in the Demux mode. The RETIME signal is routed to DOUT7 through a flip-flop. The flip-flop is internally clocked by the low-speed ECL output clock, CLKE. The retimer function is shown in Figure 2. See Figure 4 on page 7 for a timing illustration.

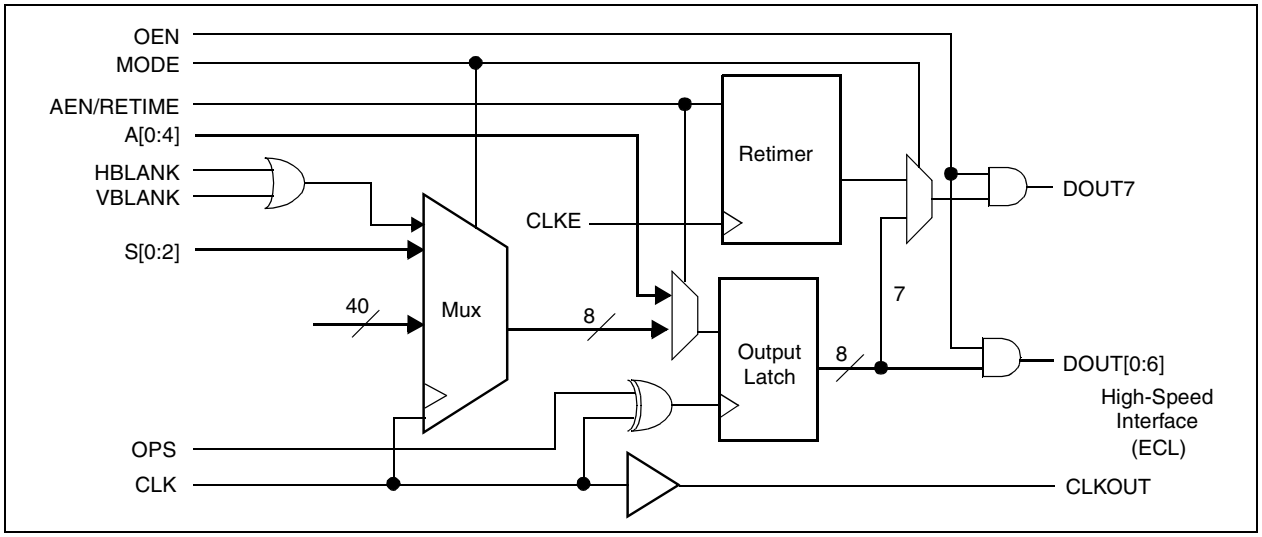


Figure 2. Output Detailed Block Diagram

Termination

It is recommended to leave all unused ECL outputs floating and that unused ECL inputs be terminated LOW (–2V supply). See Table 4 for the recommended input termination for all levels.

Table 4. Input Termination Recommendations

Type	State	Input
ECL	HIGH	Ground via a diode
ECL	LOW	–2V power supply
TTL	HIGH	+3.3V power supply
TTL	LOW	Ground

SPECIFICATIONS

AC Characteristics

Over Recommended Operating Conditions.

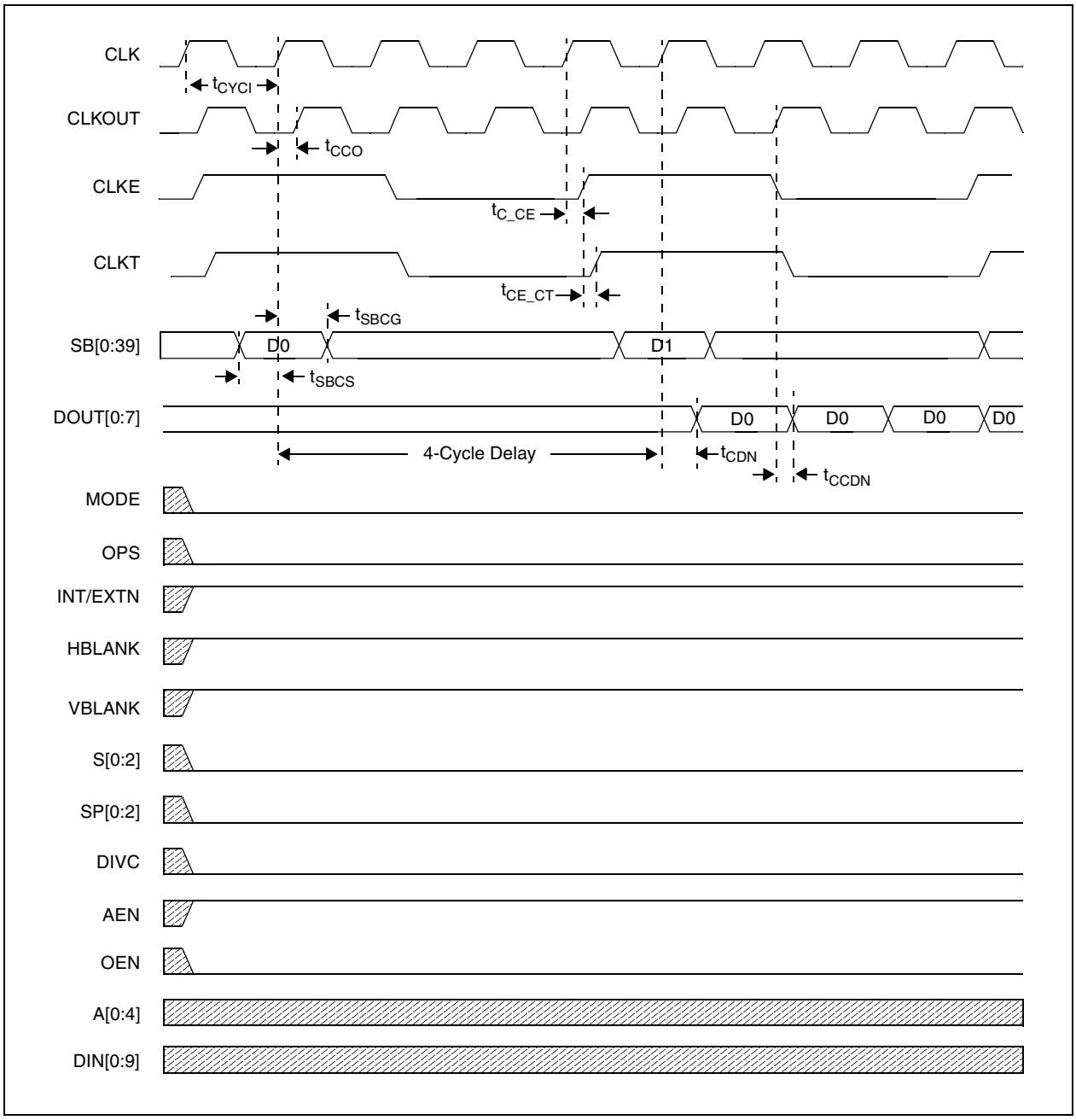


Figure 3. Multiplexer Timing Diagram (internal timing, 4:1 mode)

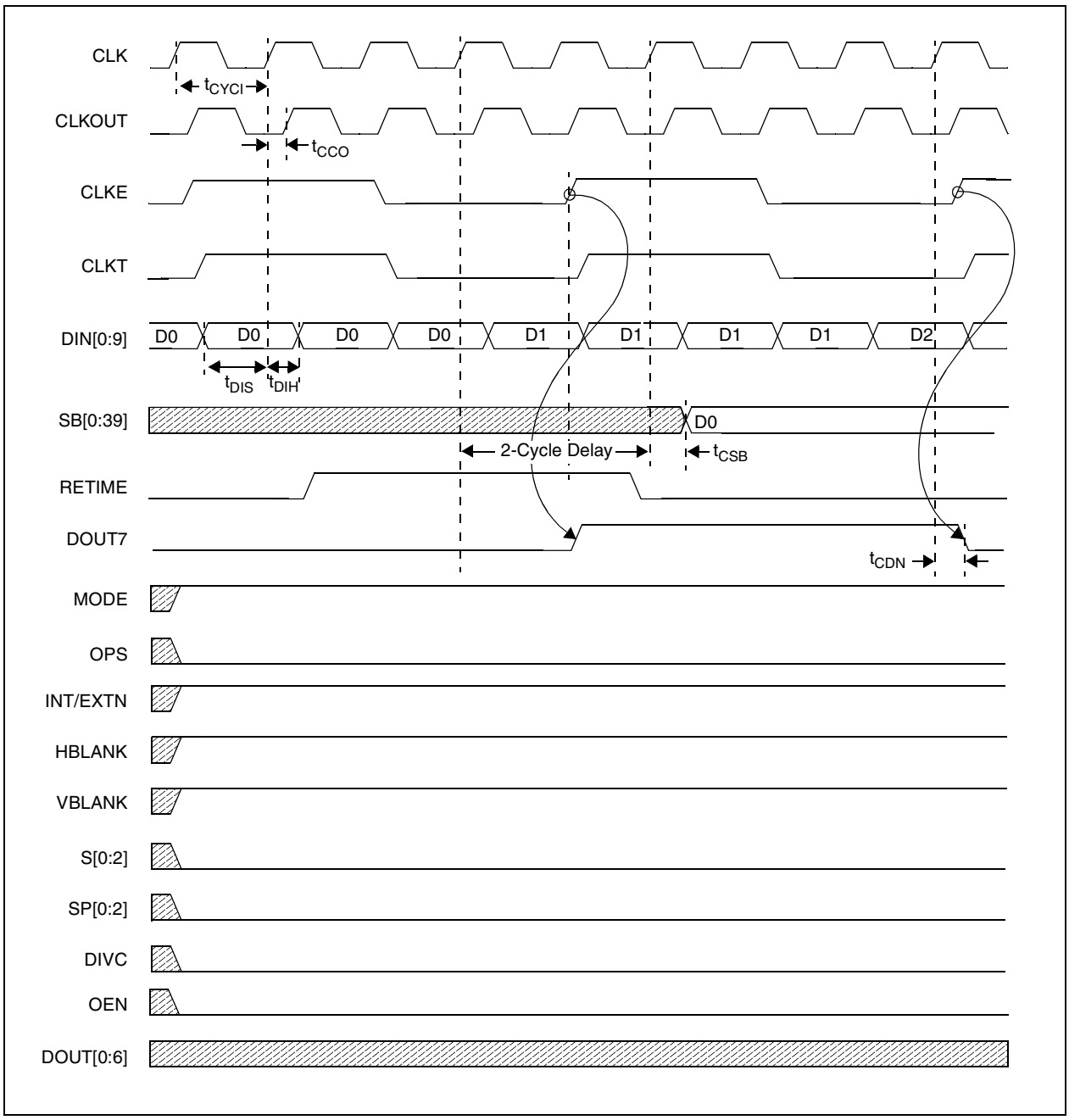


Figure 4. Demultiplexer and Retimer Timing Diagram (internal timing, 1:4 mode)

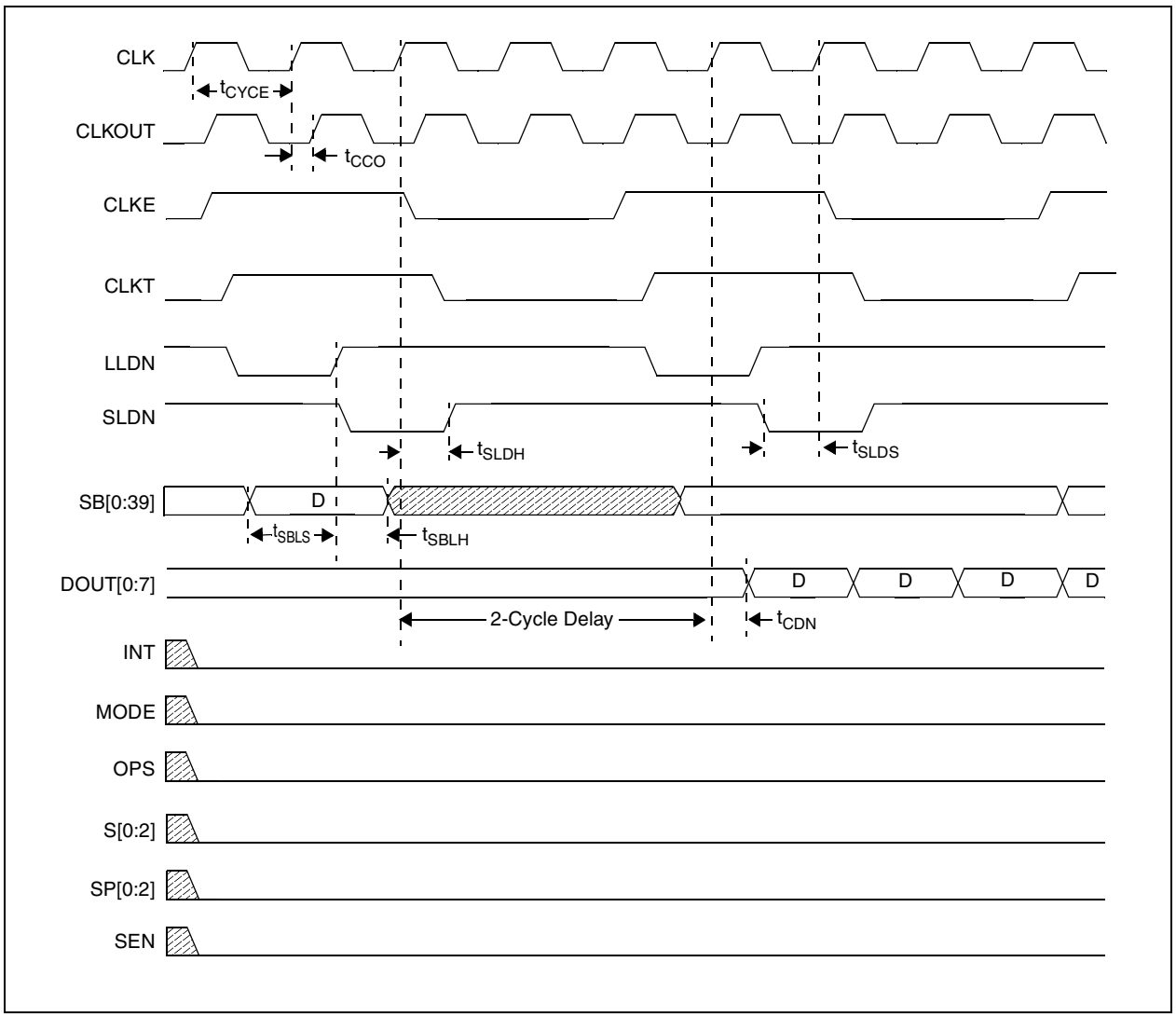


Figure 5. Multiplexer Timing Diagram (external timing, 4:1 mode)

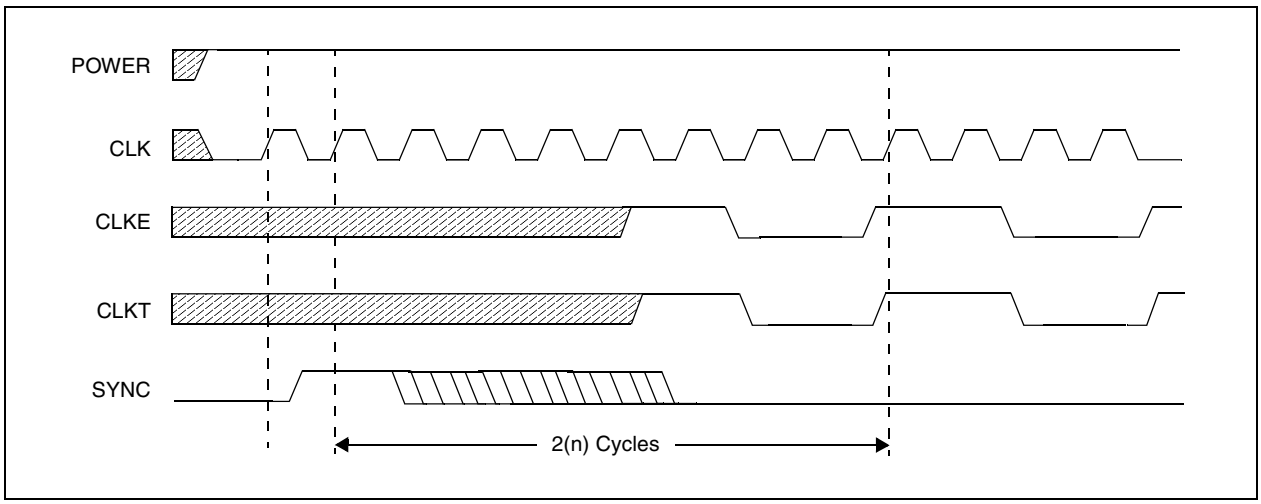


Figure 6. Initialization Timing Diagram (4:1 mode)

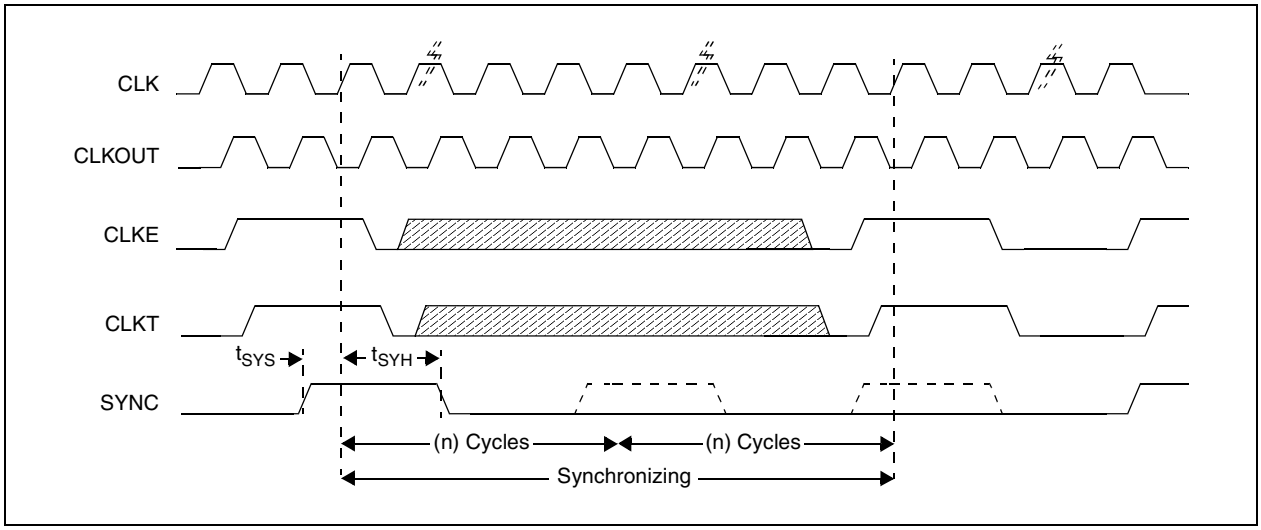


Figure 7. Synchronization Timing Diagram

Table 5. Synchronization and Blanking Timing

S[0:2]	000	001	010	011	100	101	110	111
n	4	5	8	10	16	20	32	40

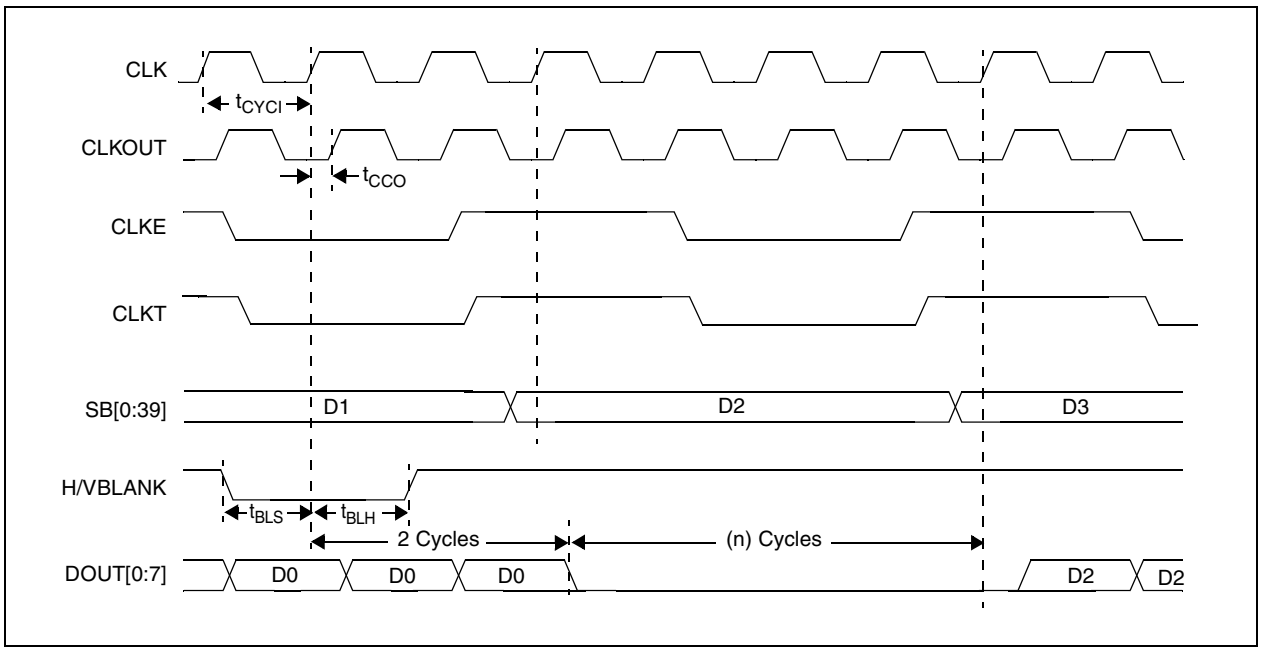


Figure 8. Blanking Timing Diagram (internal timing)

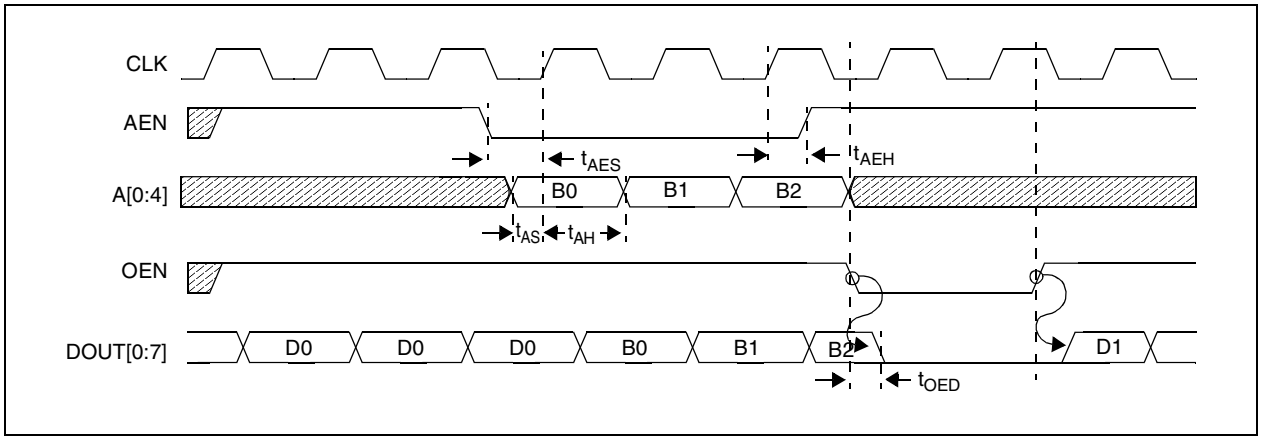


Figure 9. Address Interface/Output Enable Timing Diagram

Table 6. Timing Table

Symbol	Parameter	Min	Typ	Max	Units
t_{CYCI}	Minimum cycle time in internal timing mode	2.0			ns
t_{CYCE}	Minimum cycle time in external timing mode	4.0			ns
t_{DIS}	DIN setup time	200			ps
t_{DIH}	DIN hold time	900			ps
t_{SBCS}	SB setup with respect to CLK	600			ps
t_{SBCH}	SB hold time with respect to CLK	800			ps
t_{SBLS}	SB setup with respect to LLDN	100			ps
t_{SBLH}	SB hold with respect to LLDN	1200			ps
t_{CCO}	CLK to CLKOUT delay	1100		3500	ps
t_{CDN}	CLK rising edge to DOUT with OPS LOW	1200		3700	ps
t_{CDI}	CLK falling edge to DOUT with OPS HIGH	1300		3900	ps
t_{CCDN}	CLKOUT to DOUT skew with OPS LOW	–140		1100	ps
t_{CCDI}	CLKOUT to DOUT skew with OPS HIGH	–50		1200	ps
t_{OED}	OEN to DOUT	900		3000	ps
t_{DDS}	DOUT<x> to DOUT<y> skew			100	ps
t_{AS}	A[0:4] setup time	1100			ps
t_{AH}	A[0:4] hold time	200			ps
t_{AES}	AEN setup time	900			ps
t_{AEH}	AEN hold time	600			ps
t_{BLS}	H/VBLANK setup time	1000			ps
t_{BLH}	H/VBLANK hold time	200			ps
t_{SLDS}	SLDN setup time	1300			ps
t_{SLDH}	SLDN hold time	100			ps
t_{SYS}	SYNC setup time	800			ps
t_{SYH}	SYNC hold time	300			ps
t_{SIS}	SIN setup time	700			ps
t_{SIH}	SIN hold time	300			ps
t_{CSB}	CLK to SB delay	1700		5800	ps
t_{C_CE}	CLK to CLKE delay	1500		5200	ps
t_{CE_CT}	CLKE to CLKT skew	400		2500	ps

DC Characteristics

Over Recommended Operating Conditions.

Table 7. ECL Inputs and Outputs[1, 2]

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{OH}	Output HIGH voltage	–1020		–700	mV	
V_{OL}	Output LOW voltage	–2000		–1620	mV	
V_{IH}	Input HIGH voltage	–1165		–700	mV	
V_{IL}	Input LOW voltage	–2000		–1475	mV	
I_{IH}	Input HIGH current			200	µA	$V_{IN} = V_{IH}$ (max)
I_{IL}	Input LOW current	–50			µA	

1. *Load = 50Ω to –2.0V.*
2. *External reference (V_{REF}) = ±25mV.*

Table 8. TTL Inputs and Outputs

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{OH}	Output HIGH voltage	2.4			V	I_{OH} = –12mA
V_{OL}	Output LOW voltage			0.4	V	I_{OL} = 12mA
V_{IH}	Input HIGH voltage	2.0		V_{TTL} + 1.0	V	
V_{IL}	Input LOW voltage	0		0.8	V	
I_{IH}	Input HIGH current			300	µA	V_{IN} = 2.4V
I_{IL}	Input LOW current	–50			µA	V_{IN} = 0.4V
I_{OZH}	Tri-state output OFF, current HIGH			200	µA	V_{OUT} = 2.4V
I_{OZL}	Tri-state output OFF, current LOW	–100			µA	V_{OUT} = 0.4V
I_{OZHB}	Tri-state output OFF, current HIGH for bidirectional			500	µA	V_{OUT} = 2.4V
I_{OH}	Open current output leakage current			200	µA	V_{OUT} = 2.4V

Table 9. Power Supply Requirements

Symbol	Parameter	Min	Typ	Max	Units	Condition
I_{TT}	Power supply current from V_{TT} (–2.0V ± 0.1V max –2.1V)			850	mA	
I_{TTL}	Power supply current from V_{TTL} (+3.3V – 0.3V max +3.6V)			850	mA	
P_D	Power dissipation			2.7	W	With outputs open circuit.

Table 10. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{TT}	Power supply voltage	–2.1	–2.0	–1.9	V
V_{TTL}	Power supply voltage	+3.0	+3.3	+3.6	V
T	Operating temperature range[1]	0		+70	°C

1. Lower limit of specification is ambient temperature and upper limit is case temperature.

Table 11. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{TT}	Power supply voltage, potential to ground	–2.5	+0.5	V
V_{TTL}	Power supply voltage, potential to ground	–0.5	+4.3	V
	Input voltage applied, ECL	+0.5	V_{TT} – 0.5	V
	Input voltage applied, TTL	–0.5	$V_{TT\,L}$ + 1.0	V
I_{OUT}	Output current		50	mA
T_C	Case temperature under bias	–55	+125	°C
T_S	Storage temperature	–65	+150	°C
V_{ESD}	ESD voltage (Human Body Model)		1500	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PACKAGE INFORMATION

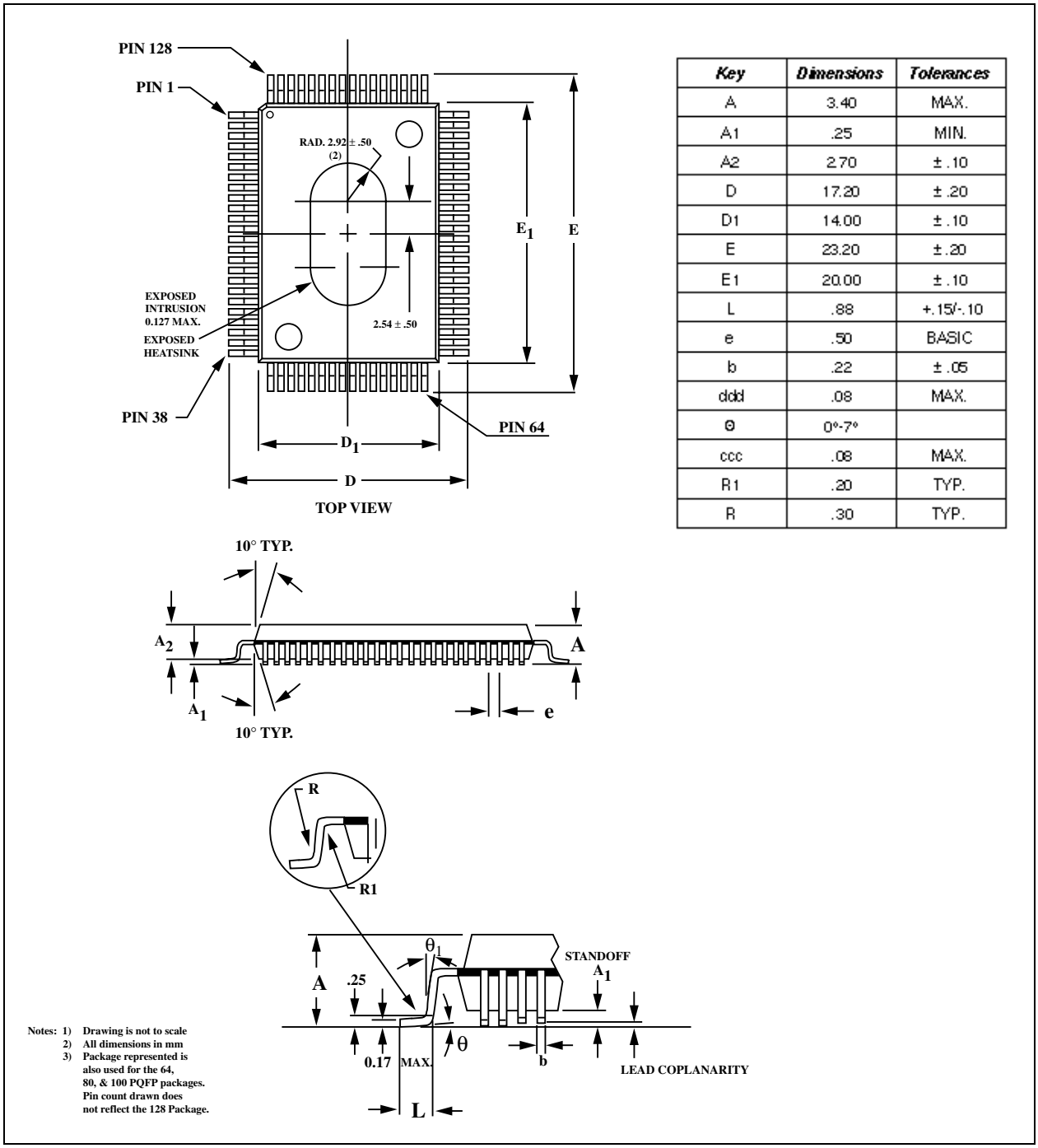
The VSC6424 is packaged in a thermally-enhanced 128-pin PQFP with an exposed heat spreader.

Table 12. Pin Identifications

Signal	Pin Number5	Type	Level	Description
VCC	7, 9, 18, 30, 32, 44, 45,58, 59, 71, 72, 73, 82, 85, 94, 96, 108, 109, 122, 123		Pwr	0V Ground.
VTT	3, 6, 13, 26, 33, 70, 77, 90, 97		Pwr	–2V Power Supply.
VTTL	5, 8, 21, 31, 34, 48, 55, 69, 95, 98, 112, 119		Pwr	+3.3V Power Supply.
VREF	4			–1.32V External ECL Reference Voltage.
DIN[0:9]	101, 102, 103, 104, 105, 68, 67, 66, 65, 64	I	ECL	Demultiplexer High-Speed Inputs.
DOUT[0:7]	86, 84, 83, 81, 80, 76, 75, 74	O	ECL	Multiplexer High-Speed Outputs.
SB[0:39]	89, 91, 92, 93, 110, 111, 113, 114, 115, 116, 117, 118, 120, 121, 10, 11, 12, 14, 15, 16, 17, 19, 20, 22, 23, 24, 25, 27, 28, 29, 46, 47, 49, 50, 51, 52, 53, 54, 56, 57	Bidirec-tional	TTL	Slow Bidirectional Bus. These pins are inputs in the Mux mode and outputs in the Demux mode.
MODE	62	I	TTL	Mux/Demux Select Signal. Set to 1 for Demux and 0 for Mux.
AEN RETIME	100	I	TTL	Address Enable. In Mux mode, while AEN is LOW, the clock transfers A[0:4] to DOUT[0, 2, 4, 6, 7]. In Demux mode, this pin provides retimer input.
CLK	60	I	ECL	Differential Clock Input, True.
CLKN	61	I	ECL	Differential Cock Input, Complement.
S[0:2]	39, 40, 41	I	TTL	Shift Register Modulus Control.
CLKE	87	O	ECL	Low-Speed Clock, ECL. The clock used for latching the low-speed bus in the internal timing mode.
CLKT	88	O	TTL	Low-Speed Clock, TTL. The clock used for latching the low-speed bus in the internal timing mode.
SP[0:2]	36, 37, 38	I	TTL	Phase Select for Output Clocks (CLKE, CLKT).
SYNC SLDN	106	I	TTL	Shift Register Load Control. This pin is used to transfer data from input latch to shift register in the external timing mode. Data is transferred on the rising edge of CLK while SLDN is LOW. In the internal timing mode, SYNC is the synchronization input.
LLDN	43	I	TTL	Input Latch Control. In the external timing mode, LLDN LOW makes the low-speed input latches transparent.
SIN	42	I	ECL	Serial Data In. The shift register can be serially loaded using this pin. The data is latched on rising edge of CLK. If this pin is not used, connect to VTT.
SEN DIVC	63	I	ECL	Shift Enable. In the external timing mode, SEN HIGH stops the shift register from shifting. In the internal timing mode, DIVC HIGH divides the output clocks (CLKE, CLKT) by 2.

Table 12. Pin Identifications (continued)

Signal	Pin Number5	Type	Level	Description
OEN	107	I	ECL	Output Enable. OEN HIGH forces the DOUT[0:7] LOW. This signal is asynchronous.
INT EXTN	99	I	TTL	Timing Control. HIGH sets the chip for internal timing and LOW sets the chip for external timing.
A[0:4]	2, 1, 128, 127, 126	I	TTL	Address Pins. These pins get transferred to DOUT[0:7] in Address Interface mode.
HBLANK	124	I	TTL	Horizontal Blank Function, Active LOW.
VBLANK	125	I	TTL	Vertical Blank Function, Active LOW.
OPS	35	I	TTL	Clock Phase Select. When this signal is LOW the low-speed outputs, DOUT[0:7], are clocked with the rising edge of the clock. Setting this pin HIGH clocks them with the falling edge of the clock.
CLKOUT	78	O	ECL	High-Speed Clock Output, True.
CLKOUTN	79	O	ECL	High-Speed Clock Output, Complement.



Key	Dimensions	Tolerances
A	3.40	MAX.
A1	.25	MIN.
A2	2.70	± .10
D	17.20	± .20
D1	14.00	± .10
E	23.20	± .20
E1	20.00	± .10
L	.88	+.15/-.10
e	.50	BASIC
b	.22	± .05
ddd	.08	MAX.
Θ	0°-7°	
ccc	.08	MAX.
R1	.20	TYP.
R	.30	TYP.

Figure 10. Package Drawing for 128-PQFP (QW)

Moisture Sensitivity Level

This device is rated moisture sensitivity level 3 or better as specified in JEDEC standard IPC/JEDEC J-STD-020B. For more information, see the JEDEC standard.

ORDERING INFORMATION

VSC6424 500Mb/s Video Shift Register IC

Part Number	Description
VSC6424QW	128-pin thermally enhanced PQFP with exposed heat spreader, 14mm x 20mm body Temperature range: 0°C ambient to +70°C case

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