

Section 19 Electrical Specifications

19.1 Absolute Maximum Ratings

Table 19-1 lists the absolute maximum ratings.

Table 19-1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.3 to +7.0	V
Input voltage (except port 7)	V _{in}	-0.3 to V _{CC} + 0.3	V
(port 7)	V _{in}	-0.3 to AV _{CC} + 0.3	V
Analog supply voltage	AV _{CC}	-0.3 to +7.0	V
Analog input voltage	V _{AN}	-0.3 to AV _{CC} + 0.3	V
Operating temperature	T _{opr}	Regular specifications: -20 to +75	°C
		Wide-range specifications: -40 to +85	°C
Storage temperature	T _{stg}	-55 to +125	°C

Note: Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions.

19.2 Electrical Characteristics

19.2.1 DC Characteristics

Table 19-2 lists the DC characteristics.

Table 19-2 DC Characteristics

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%^{*1}$, $V_{SS} = AV_{SS} = 0\text{ V}$,
 $T_a = -20\text{ to }+75^\circ\text{C}$ (Regular Specifications)
 $T_a = -40\text{ to }+85^\circ\text{C}$ (Wide-Range Specifications)

Item		Sym- bol	Min	Typ	Max	Measurement	
						Unit	Conditions
Input High voltage	RES, STBY,	V_{IH}	$V_{CC} - 0.7$	–	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	–	$V_{CC} + 0.3$		
	Port 7		2.2	–	$AV_{CC} + 0.3$		
	Other input pins (except port 4)		2.2	–	$V_{CC} + 0.3$		
Input Low voltage	RES, STBY,	V_{IL}	–0.3	–	0.5	V	
	MD ₂ , MD ₁ , MD ₀		–0.3	–	0.8		
	Other input pins (except port 4)		–0.3	–	0.8		
Schmitt trigger input voltage	Port 4	V_{T^-}	1.0	–	2.5	V	
		V_{T^+}	2.0	–	3.5	V	
		$V_{T^+} - V_{T^-}$	0.4	–	–	V	
Input leakage current	RES	$ I_{in} $	–	–	10.0	μA	$V_{in} = 0.5\text{ to}$
	STBY, NMI, MD ₂ , MD ₁ , MD ₀ , port 7		–	–	1.0	μA	$V_{CC} - 0.5\text{ V}$
Leakage current in 3-state (off state)	Port 8, ports 6 to 1	$ I_{TSI} $	–	–	1.0	μA	$V_{in} = 0.5\text{ to}$ $V_{CC} - 0.5\text{ V}$
Output High voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	–	–	V	$I_{OH} = -200\ \mu\text{A}$
			3.5	–	–	V	$I_{OH} = -1\ \text{mA}$
Output Low voltage	All output pins	V_{OL}	–	–	0.4	V	$I_{OL} = 1.6\ \text{mA}$
	RES		–	–	0.4	V	$I_{OL} = 2.6\ \text{mA}$
Input capacitance	All input pins	C_{in}	–	–	20	pF	$V_{in} = 0\text{ V}$ $f = 1\ \text{MHz}$ $T_a = 25^\circ\text{C}$

Note: *1 AV_{CC} must be connected to the power supply even when the A/D converter is not used.

Table 19-2 DC Characteristics (cont)

Item		Sym- bol					Measurement	
			Min	Typ	Max	Unit	Conditions	
Current dissipation*1	Normal operation	I _{CC}	–	15	30	mA	f = 6 MHz	
			–	20	40	mA	f = 8 MHz	
			–	25	50	mA	f = 10 MHz	
	Sleep mode		–	9	20	mA	f = 6 MHz	
			–	12	25	mA	f = 8 MHz	
			–	15	30	mA	f = 10 MHz	
	Standby		–	0.01	5.0	μA	T _a ≤ 50°C	
			–	–	20.0	μA	T _a > 50°C	
Analog supply current	During A/D conversion	Al _{CC}	–	1.0	2.0	mA		
	While waiting		–	0.01	5.0	μA		

Note: *1 Current dissipation values assume that V_{IH} min = V_{CC} – 0.5 V, V_{IL} max = 0.5 V and all output pins are in the no-load state.

Conditions: V_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to +75°C (Regular Specifications)
AV_{CC} = 5.0 V ±10%*1

Item		Sym- bol					Measurement	
			Min	Typ	Max	Unit	Conditions	
Input High voltage	RES, STBY, EXTAL	V _{IH}	V _{CC} × 0.9	–	V _{CC} + 0.3	V		
	Port 7		V _{CC} × 0.9	–	V _{CC} + 0.3	V		
	Other input pins (except port 4)		V _{CC} × 0.7	–	AV _{CC} + 0.3	V		
			V _{CC} × 0.7	–	V _{CC} + 0.3	V		
Input Low voltage	RES, STBY, MD2, MD1, MD0	V _{IL}	–0.3	–	V _{CC} × 0.1	V		
	Other input pins (except port 4)		–0.3	–	V _{CC} × 0.15	V		
Schmitt trigger input voltage	Port 4	V _T [–]	V _{CC} × 0.2	–	V _{CC} × 0.6	V		
		V _T ⁺	V _{CC} × 0.4	–	V _{CC} × 0.7	V		
		V _T ⁺ –V _T [–]	V _{CC} × 0.07	–	–	V		
Input leakage current	RES	I _{in}	–	–	10.0	μA	V _{in} = 0.5 to	
	STBY, NMI, MD2, MD1, MD0, port 7		–	–	1.0	μA	V _{CC} – 0.5 V	

Note: *1 AV_{CC} must be connected to the power supply even when the A/D converter is not used.

Table 19-2 DC Characteristics (cont)

Item		Sym- bol	Min	Typ	Max	Unit	Measurement Conditions
Leakage current in 3-state (off state)	Port 8, ports 6 to 1	I _{TSI}	–	–	1.0	μA	V _{in} = 0.5 to V _{CC} – 0.5 V
Output High voltage	All output pins	V _{OH}	V _{CC} – 0.4	–	–	V	I _{OH} = –200 μA
			V _{CC} – 0.9	–	–	V	I _{OH} = –1 mA
Output Low voltage	All output pins	V _{OL}	–	–	0.4	V	I _{OL} = 1.6 mA
	RES		–	–	0.4	V	I _{OL} = 2.6 mA
Input capacitance	All input pins	C _{in}	–	–	20	pF	V _{in} = 0 V f = 1 MHz T _a = 25°C
Current dissipation*1	Normal operation	I _{CC}	–	20	28	mA	f = 5 MHz
	Sleep mode		–	12	18	mA	f = 5 MHz
	Standby		–	0.01	5.0	μA	T _a ≤ 50°C
			–	–	20.0	μA	T _a > 50°C
Analog supply current	During A/D conversion	A _{ICC}	–	1.0	2.0	mA	
	While waiting		–	0.01	5.0	μA	

Note: *1 Current dissipation values assume that V_{IH} min = V_{CC} × 0.9 V, V_{IL} max = 0.3 V and all output pins are in the no-load state.

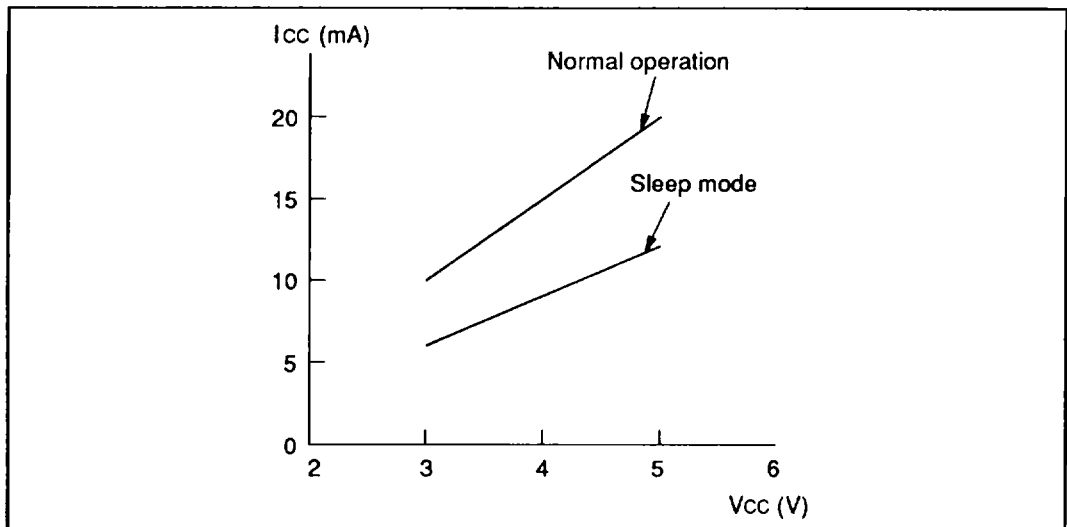


Figure 19-1 Relation between I_{CC} and V_{CC}

Table 19-3 Allowable Output Current Sink Values

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0\text{ V}$,
 $T_a = -20\text{ to }+75^\circ\text{C}$ (Regular Specifications)
 $T_a = -40\text{ to }+85^\circ\text{C}$ (Wide-Range Specifications)

Item		Symbol	Min	Typ	Max	Unit
Allowable output Low current sink (per pin)	Per output pin	IoL	-	-	2.0	mA
Allowable output Low current sink (total)	Total of all output pins	Σ IoL	-	-	80	mA
Allowable output High current sink (per pin)	All output pins	-IoH	-	-	2.0	mA
Allowable output High current sink (total)	Total of all output pins	Σ -IoH	-	-	25	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 19-3. In particular, when driving a Darlington transistor pair directly, be sure to insert a current-limiting resistor in the output path. See figure 19-2.

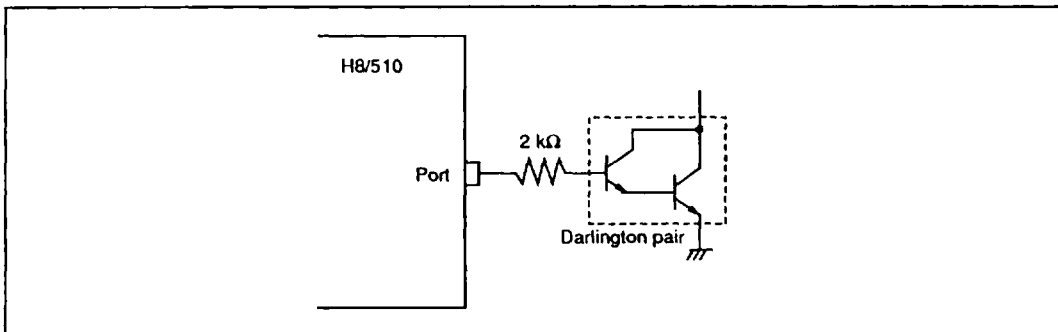


Figure 19-2 Example of Circuit for Driving a Darlington Transistor Pair

19.2.2 AC Characteristics

The AC characteristics of the H8/510 chip are listed in three tables. Bus timing parameters are given in table 20-4, control signal timing parameters in table 20-5, and timing parameters of the on-chip supporting modules in table 20-6.

Table 19-4 Bus Timing

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $\phi = 0.5$ to 10 MHz , $V_{SS} = 0\text{ V}$
 $T_a = -20$ to $+75^\circ\text{C}$ (Regular Specifications)
 $T_a = -40$ to $+85^\circ\text{C}$ (Wide-Range Specifications)

Item	Symbol	6 MHz		8 MHz		10 MHz		Unit	Measurement Conditions
		Min	Max	Min	Max	Min	Max		
Clock cycle time	t_{cyc}	166.7	2000	125	2000	100	2000	ns	See figures
Clock pulse width Low	t_{CL}	65	–	45	–	40	–	ns	19-4 and 19-5
Clock pulse width High	t_{CH}	65	–	45	–	40	–	ns	
Clock rise time	t_{Cr}	–	15	–	15	–	10	ns	
Clock fall time	t_{Cf}	–	15	–	15	–	10	ns	
Address delay time	t_{AD}	–	50	–	40	–	30	ns	
Address hold time	t_{AH1}	30	–	25	–	15	–	ns	
Read strobe delay time 1	t_{RDD1}	–	50	–	40	–	30	ns	
Read strobe delay time 2	t_{RDD2}	–	50	–	40	–	40	ns	
Read strobe width High 1	t_{ASH1}	110	–	85	–	70	–	ns	
Read strobe width High 2	t_{ASH2}	110	–	85	–	70	–	ns	
Write strobe delay time 1	t_{WRD1}	–	50	–	40	–	30	ns	
Write strobe delay time 2	t_{WRD2}	–	50	–	40	–	30	ns	
Write strobe delay time 3	t_{WRD3}	–	50	–	40	–	30	ns	
Write data strobe pulse width 1	t_{WRW1}	150	–	110	–	90	–	ns	
Write data strobe pulse width 2	t_{WRW2}	200	–	150	–	120	–	ns	
Address setup time 1	t_{AS1}	25	–	20	–	15	–	ns	
Address setup time 2	t_{AS2}	25	–	20	–	15	–	ns	
Address setup time 3	t_{AS3}	105	–	80	–	65	–	ns	
Read data setup time	t_{RDS}	40	–	30	–	20	–	ns	
Read data hold time	t_{RDH}	0	–	0	–	0	–	ns	
Read data access time 1	t_{ACC1}	–	160	–	125	–	100	ns	
Read data access time 2	t_{ACC2}	–	300	–	230	–	180	ns	
Read data access time 3	t_{ACC3}	–	81.7	–	60	–	55	ns	
Read data access time 4	t_{ACC4}	–	230	–	165	–	135	ns	
Write data delay time	t_{WDD}	–	70	–	60	–	50	ns	
Write data setup time	t_{WDS}	30	–	15	–	10	–	ns	
Write data hold time	t_{WDH}	30	–	25	–	20	–	ns	
Wait setup time	t_{WTS}	40	–	40	–	40	–	ns	See figure 19-6
Wait hold time	t_{WTH}	10	–	10	–	10	–	ns	
Bus request setup time	t_{BRQS}	40	–	40	–	40	–	ns	See figure 19-11
Bus acknowledge delay time 1	t_{BACD1}	–	70	–	60	–	50	ns	
Bus acknowledge delay time 2	t_{BACD2}	–	70	–	60	–	50	ns	
Bus floating delay time	t_{BZD}	–	t_{BACD1}	–	t_{BACD1}	–	t_{BACD1}	ns	

Table 19-4 Bus Timing (cont)

Item	Symbol	6 MHz		8 MHz		10 MHz		Unit	Measurement Conditions
		Min	Max	Min	Max	Min	Max		
E clock delay time	tED	–	20	–	15	–	15	ns	See figure 19-12
E clock rise time	tER	–	15	–	15	–	15	ns	
E clock fall time	tEF	–	15	–	15	–	15	ns	
Read data hold time (E clock sync)	tRDHE	0	–	0	–	0	–	ns	See figure 19-7
Write data hold time (E clock sync)	tWDHE	50	–	40	–	30	–	ns	

Conditions: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $\phi = 0.5\text{ to }5.0\text{ MHz}$, $V_{SS} = 0\text{ V}$

$T_a = -20\text{ to }+75^\circ\text{C}$ (Regular Specifications)

Item	Symbol	5 MHz		Unit	Measurement Conditions
		Min	Max		
Clock cycle time	t _{cy}	200	2000	ns	See figures 19-4 and 19-5
Clock pulse width Low	t _{CL}	60	–	ns	
Clock pulse width High	t _{CH}	60	–	ns	
Clock rise time	t _{Cr}	–	25	ns	
Clock fall time	t _{Cf}	–	25	ns	
Address delay time	t _{AD}	–	80	ns	
Address hold time (read)	t _{AH1}	5	–	ns	
Address hold time (write)	t _{AH2}	20	–	ns	
Read strobe delay time 1	t _{RDD1}	–	80	ns	
Read strobe delay time 2	t _{RDD2}	–	120	ns	
Write strobe delay time 1	t _{WRD1}	–	80	ns	
Write strobe delay time 2	t _{WRD2}	–	80	ns	
Write strobe delay time 3	t _{WRD3}	–	80	ns	
Write data strobe pulse width1	t _{WRW1}	150	–	ns	
Write data strobe pulse width2	t _{WRW2}	220	–	ns	
Address setup time 1	t _{AS1}	30	–	ns	
Address setup time 2	t _{AS2}	30	–	ns	
Address setup time 3	t _{AS3}	130	–	ns	
Read data setup time	t _{RDS}	50	–	ns	
Read data hold time	t _{RDH}	0	–	ns	
Read data access time 1	t _{ACC1}	–	180	ns	
Read data access time 2	t _{ACC2}	–	350	ns	
Write data delay time	t _{WDD}	–	120	ns	
Write data setup time	t _{WDS}	10	–	ns	
Write data hold time	t _{WDH}	40	–	ns	

Table 19-4 Bus Timing (cont)

Item	Symbol	5 MHz		Unit	Measurement Conditions
		Min	Max		
Wait setup time	tWTS	60	–	ns	See figure 19-6
Wait hold time	tWTH	20	–	ns	
Bus request setup time	tBRQS	80	–	ns	See figure 19-11
Bus acknowledge delay time 1	tBACD1	–	80	ns	
Bus acknowledge delay time 2	tBACD2	–	80	ns	
Bus floating delay time	tBZD	–	tBACD1	ns	
E clock delay time	tED	–	50	ns	See figure 19-12
E clock rise time	tER	–	25	ns	
E clock fall time	tEF	–	25	ns	
Read data hold time (E clock sync)	tRDHE	30	–	ns	See figure 19-7
Write data hold time (E clock sync)	tWDHE	40	–	ns	

Table 19-5 Control Signal Timing

Conditions: VCC = 5.0 V ±10%, AVCC = 5.0 V ±10%, ϕ = 0.5 to 10 MHz, VSS = 0 V

Ta = –20 to +75°C (Regular Specifications)

Ta = –40 to +85°C (Wide-Range Specifications)

Item	Symbol	6 MHz		8 MHz		10 MHz		Unit	Measurement Conditions
		Min	Max	Min	Max	Min	Max		
$\overline{\text{RES}}$ setup time	tRESS	200	–	200	–	200	–	ns	See figure 19-8
$\overline{\text{RES}}$ pulse width	tRESW	6.0	–	6.0	–	6.0	–	t _{cy}	
$\overline{\text{RES}}$ output delay time	tRESO	–	100	–	100	–	100	ns	See figure 19-8
$\overline{\text{RES}}$ output pulse width	tRESOW	132	–	132	–	132	–	t _{cy}	
NMI setup time	tNMIS	150	–	150	–	150	–	ns	See figure 19-10
NMI hold time	tNMIH	10	–	10	–	10	–	ns	
$\overline{\text{IRQ0}}$ setup time	tIRQ0S	50	–	50	–	50	–	ns	
$\overline{\text{IRQ1}}$ setup time	tIRQ1S	50	–	50	–	50	–	ns	
$\overline{\text{IRQ1}}$ hold time	tIRQ1H	10	–	10	–	10	–	ns	
NMI pulse width (for recovery from software standby mode)	tNMIW	200	–	200	–	200	–	ns	
Crystal oscillator settling time (reset)	tOSC1	20	–	20	–	20	–	ms	See figure 19-11
Crystal oscillator settling time (software standby)	tOSC2	10	–	10	–	10	–	ms	See figure 18-1

Table 19-5 Control Signal Timing (cont)

Conditions: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $\phi = 0.5\text{ to }5.0\text{ MHz}$, $V_{SS} = 0\text{ V}$
 $T_a = -20\text{ to }+75^\circ\text{C}$ (Regular Specifications)

Item	Symbol	5 MHz		Unit	Measurement Conditions
		Min	Max		
$\overline{\text{RES}}$ setup time	tRESS	300	–	ns	See figure 19-8
$\overline{\text{RES}}$ pulse width	tRESW	6.0	–	tcyc	
$\overline{\text{RES}}$ output delay time	tRESO	–	150	ns	See figure 19-8
$\overline{\text{RES}}$ output pulse width	tRESOW	132	–	tcyc	
NMI setup time	tNMIS	300	–	ns	See figure 19-10
NMI hold time	tNMIH	10	–	ns	
$\overline{\text{IRQ0}}$ setup time	tIRQ0S	100	–	ns	
$\overline{\text{IRQ1}}$ setup time	tIRQ1S	100	–	ns	
$\overline{\text{IRQ1}}$ hold time	tIRQ1H	10	–	ns	
NMI pulse width (for recovery from software standby mode)	tNMIW	200	–	ns	
Crystal oscillator settling time (reset)	tOSC1	20	–	ms	See figure 19-13
Crystal oscillator settling time (software standby)	tOSC2	10	–	ms	See figure 18-1

Table 19-6 Timing Conditions of On-Chip Supporting Modules

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $\phi = 0.5$ to 10 MHz , $V_{SS} = 0\text{ V}$
 $T_a = -20$ to $+75^\circ\text{C}$ (Regular Specifications)
 $T_a = -40$ to $+85^\circ\text{C}$ (Wide-Range Specifications)

Item	Symbol	6 MHz		8 MHz		10 MHz		Unit	Measurement Conditions		
		Min	Max	Min	Max	Min	Max				
FRT	Timer output delay time	IFTOD	–	100	–	100	–	100	ns	See figure 19-15	
	Timer input setup time	IFTIS	50	–	50	–	50	–	ns		
	Timer clock input setup time	IFTCS	50	–	50	–	50	–	ns	See figure 19-16	
	Timer clock pulse width	IFTCW	1.5	–	1.5	–	1.5	–	t_{cyc}		
TMR	Timer output delay time	tMOD	–	100	–	100	–	100	ns	See figure 19-17	
	Timer clock input setup time	tMCS	50	–	50	–	50	–	ns	See figure 19-18	
	Timer clock pulse width	tMCW	1.5	–	1.5	–	1.5	–	t_{cyc}		
	Timer reset input setup time	tMRS	50	–	50	–	50	–	ns	See figure 19-19	
SCI	Input clock cycle	(Async)	t_{Scyc}	2	–	2	–	2	–	t_{cyc}	See figure 19-20
		(Sync)		4	–	4	–	4	–	t_{cyc}	
	Input clock pulse width	tSCKW	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}		
	Transmit data delay time (Sync)	tTXD	–	100	–	100	–	100	ns	See figure 19-21	
	Receive data setup time (Sync)	tRXS	100	–	100	–	100	–	ns		
	Receive data hold time (Sync)	tRXH	100	–	100	–	100	–	ns		
Port	Output data delay time	tPWD	–	100	–	100	–	100	ns	See figure 19-14	
	Input data setup time	tPRS	50	–	50	–	50	–	ns		
	Input data hold time	tPRH	50	–	50	–	50	–	ns		
RFSH	Refresh output delay time 1	tRFD1	–	50	–	45	–	40	ns	See figure 19-22	
	Refresh output delay time 2	tRFD2	–	50	–	45	–	40	ns		

Table 19-6 Timing Conditions of On-Chip Supporting Modules (cont)

Conditions: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $\phi = 0.5\text{ to }5.0\text{ MHz}$, $V_{SS} = 0\text{ V}$

$T_a = -20\text{ to }+75^\circ\text{C}$ (Regular Specifications)

$T_a = -40\text{ to }+85^\circ\text{C}$ (Wide-Range Specifications)

Item	Symbol	5 MHz		Unit	Measurement Conditions	
		Min	Max			
FRT	Timer output delay time	tFTOD	–	150	ns	See figure 19-15
	Timer input setup time	tFTIS	80	–	ns	
	Timer clock input setup time	tFTCS	80	–	ns	See figure 19-16
	Timer clock pulse width	tFTCW	1.5	–	t _{cyc}	
TMR	Timer output delay time	tTMOD	–	150	ns	See figure 19-17
	Timer clock input setup time	tTMCS	80	–	ns	See figure 19-18
	Timer clock pulse width	tTMCW	1.5	–	t _{cyc}	
	Timer reset input setup time	tTMRS	80	–	ns	See figure 19-19
SCI	Input clock cycle	(Async) tScyc	2	–	t _{cyc}	See figure 19-20
		(Sync)	4	–	t _{cyc}	
	Input clock pulse width	tSCKW	0.4	0.6	t _{SCKW}	
	Transmit data delay time	(Sync) tTXD	–	200	ns	See figure 19-21
	Receive data setup time	(Sync) tRXS	150	–	ns	
	Receive data hold time	(Sync) tRXH	150	–	ns	
Port	Output data delay time	tPWD	–	150	ns	See figure 19-14
	Input data setup time	tPRS	80	–	ns	
	Input data hold time	tPRH	80	–	ns	
RFSH	Refresh output delay time 1	tRFD1	–	80	ns	See figure 19-22
	Refresh output delay time 2	tRFD2	–	80	ns	

• Measurement Conditions for AC Characteristics

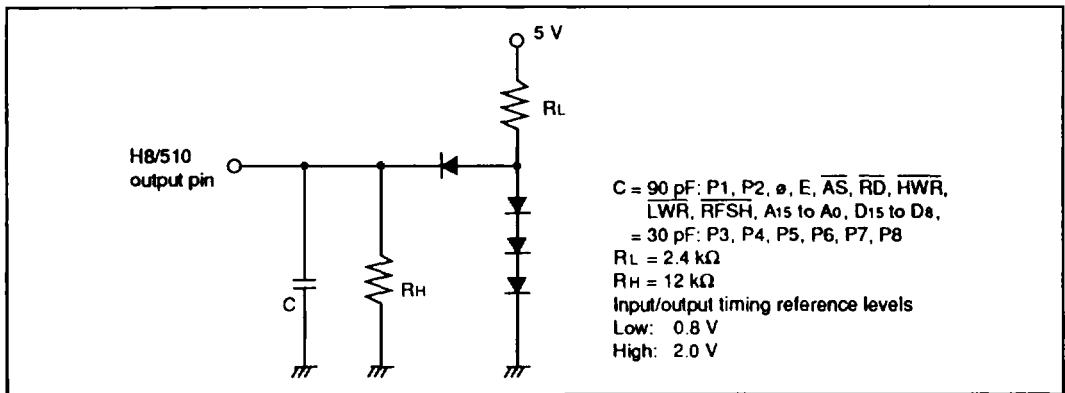


Figure 19-3 Output Load Circuit

19.2.3 A/D Converter Characteristics

Table 19-7 lists the characteristics of the on-chip A/D converter.

Table 19-7 A/D Converter Characteristics

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0\text{ V}$,

$T_a = -20\text{ to }+75^\circ\text{C}$ (Regular Specifications)

$T_a = -40\text{ to }+85^\circ\text{C}$ (Wide-Range Specifications)

Item	6 MHz			8 MHz			10 MHz			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time	—	—	22.33	—	—	16.75	—	—	13.4	μs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal-source impedance	—	—	10	—	—	10	—	—	10	k Ω
Nonlinearity error	—	—	± 3	—	—	± 3	—	—	± 3	LSB
Offset error	—	—	± 2	—	—	± 2	—	—	± 2	LSB
Full-scale error	—	—	± 2	—	—	± 2	—	—	± 2	LSB
Quantizing error	—	—	$\pm 1/2$	—	—	$\pm 1/2$	—	—	$\pm 1/2$	LSB
Absolute accuracy	—	—	± 4	—	—	± 4	—	—	± 4	LSB

Conditions: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20\text{ to }+75^\circ\text{C}$ (Regular Specifications)

$AV_{CC} = 5.0\text{ V} \pm 10\%$

Item	5 MHz			Unit
	Min	Typ	Max	
Resolution	10	10	10	Bits
Conversion time	—	—	26.8	μs
Analog input capacitance	—	—	20	pF
Allowable signal-source impedance	—	—	10	k Ω
Nonlinearity error	—	—	± 3	LSB
Offset error	—	—	± 2	LSB
Full-scale error	—	—	± 2	LSB
Quantizing error	—	—	$\pm 1/2$	LSB
Absolute accuracy	—	—	± 4	LSB

19.3 MCU Operational Timing

This section provides the following timing charts:

19.3.1 Bus timing	Figures 19-4 to 19-7
19.3.2 Control Signal Timing	Figures 19-8 to 19-11
19.3.3 Clock Timing	Figures 19-12 and 19-13
19.3.4 I/O Port Timing	Figure 19-14
19.3.5 16-Bit Free-Running Timer Timing	Figures 19-15 and 19-16
19.3.6 8-Bit Timer Timing	Figures 19-17 to 19-19
19.3.7 Serial Communication Interface Timing	Figures 19-20 and 19-21
19.3.8 Refresh Timing	Figures 19-22 and 19-23

19.3.1 Bus Timing

1. Basic Bus Cycle (Two-State Mode)

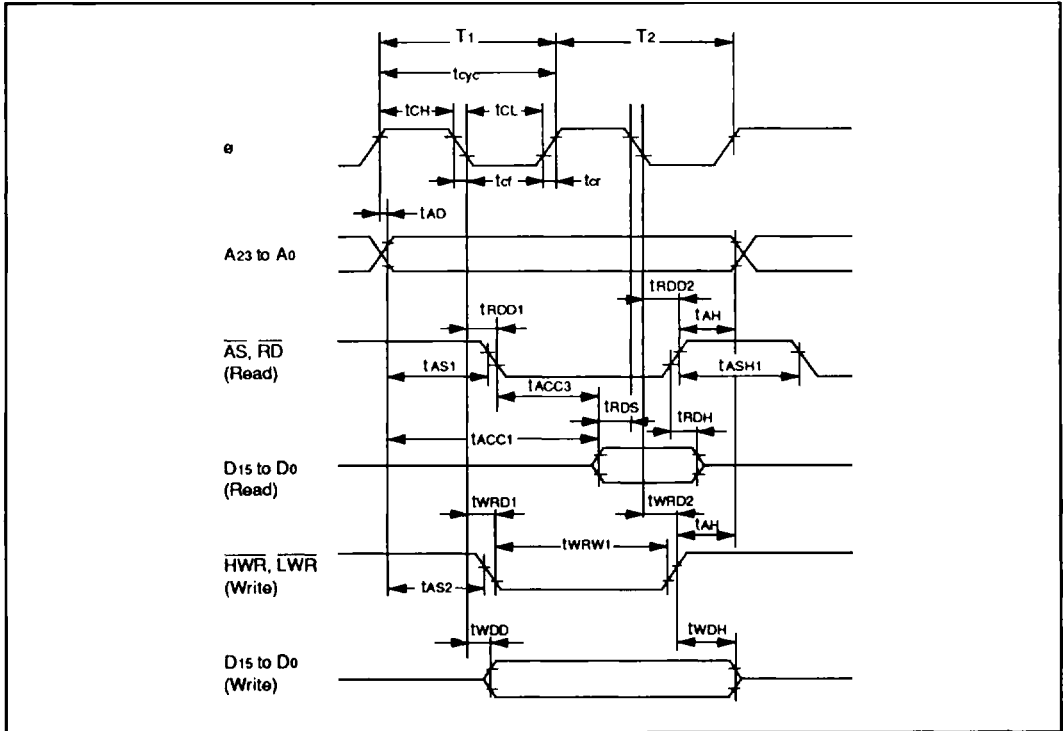


Figure 19-4 Basic Bus Cycle (Two-State Mode)

2. Basic Bus Cycle (Three-State Mode)

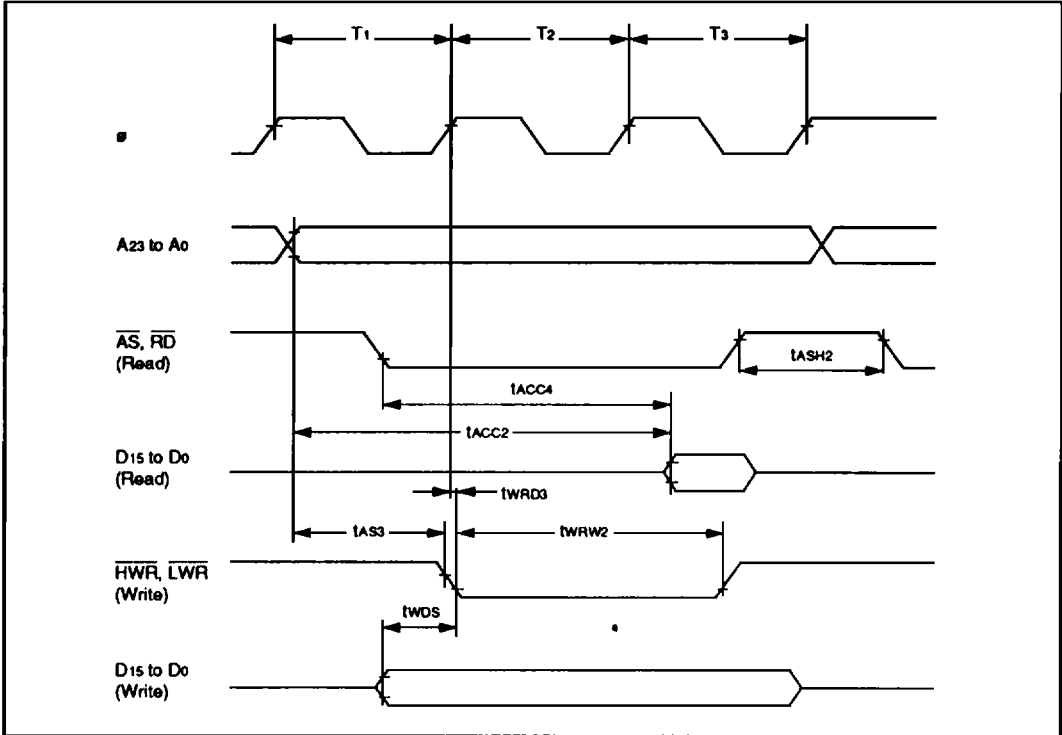


Figure 19-5 Basic Bus Cycle (Three-State Mode)

3. Basic Bus Cycle (Three-State Mode with One Wait State)

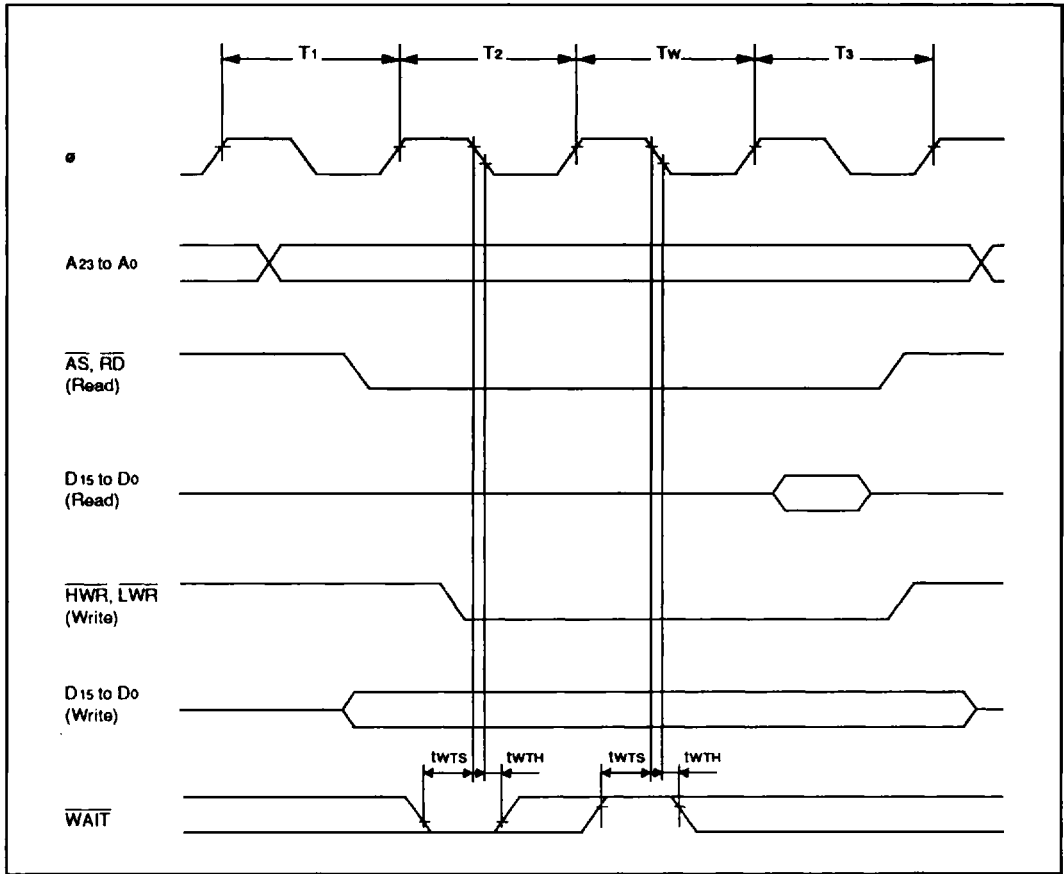


Figure 19-6 Basic Bus Cycle (Three-State Mode with One Wait State)

4. Bus Cycle Synchronized with E Clock

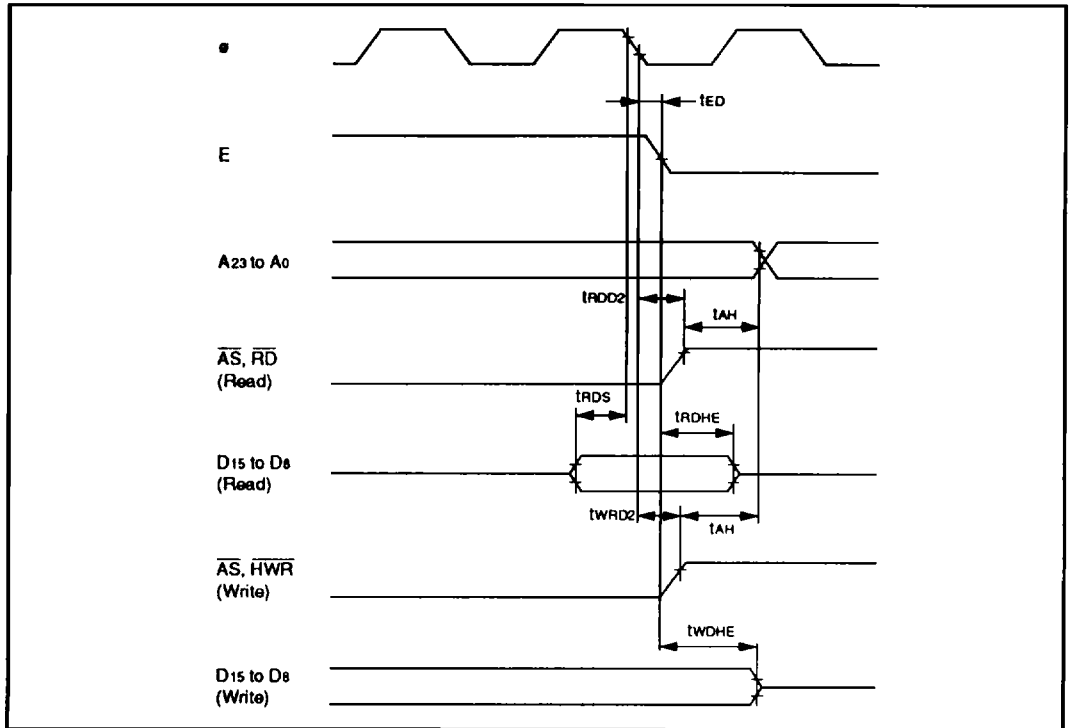


Figure 19-7 Bus Cycle Synchronized with E Clock

19.3.2 Control Signal Timing

1. Reset Input Timing

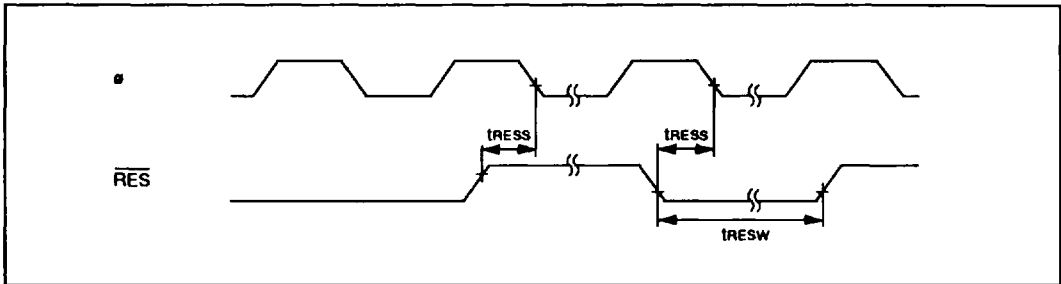


Figure 19-8 Reset Input Timing

2. Reset Output Timing

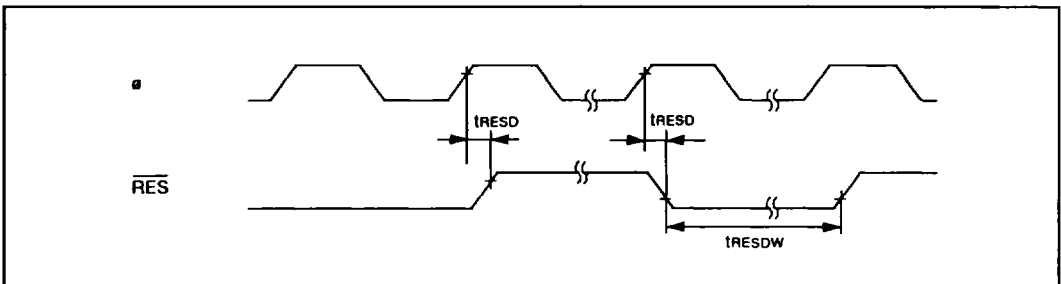


Figure 19-9 Reset Output Timing

3. Interrupt Input Timing

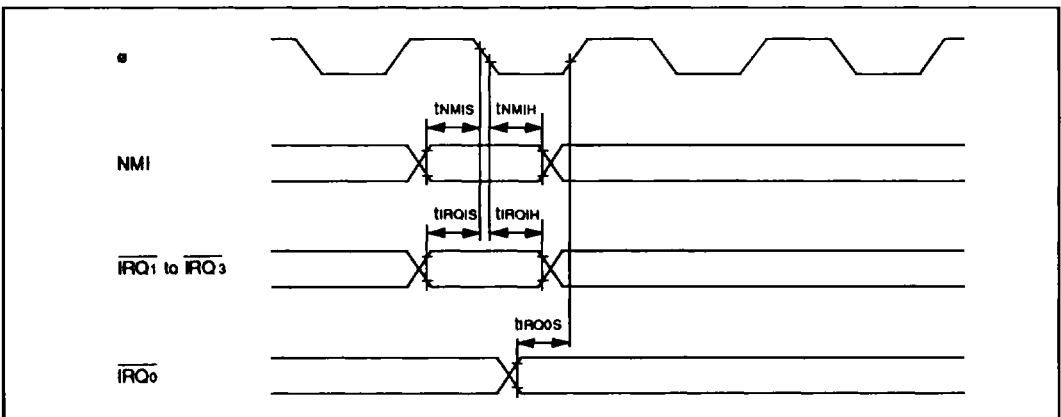


Figure 19-10 Interrupt Input Timing

4. Bus Release State Timing

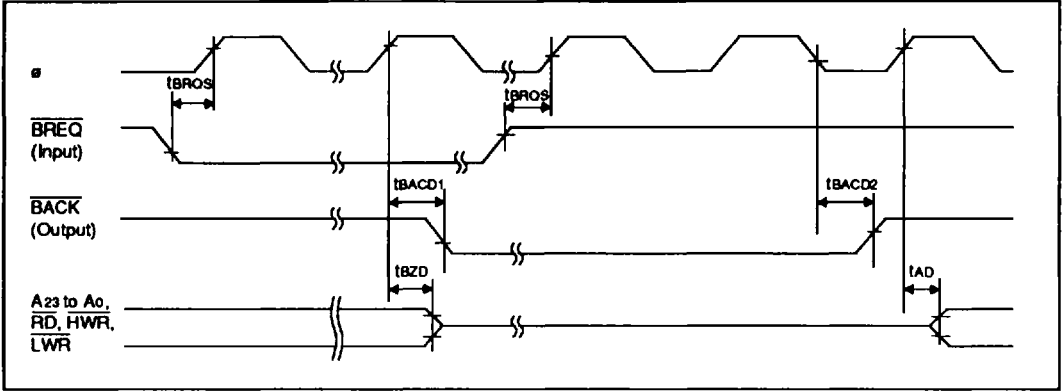


Figure 19-11 Bus Release State Timing

19.3.3 Clock Timing

1. E Clock Timing

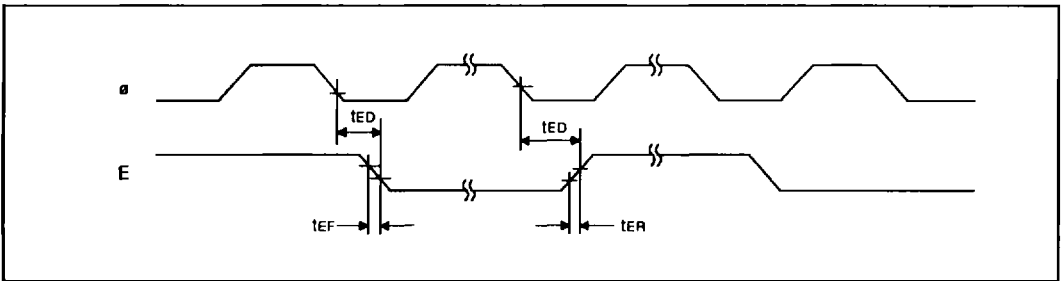


Figure 19-12 E Clock Timing

2. Clock Oscillator Stabilization Timing

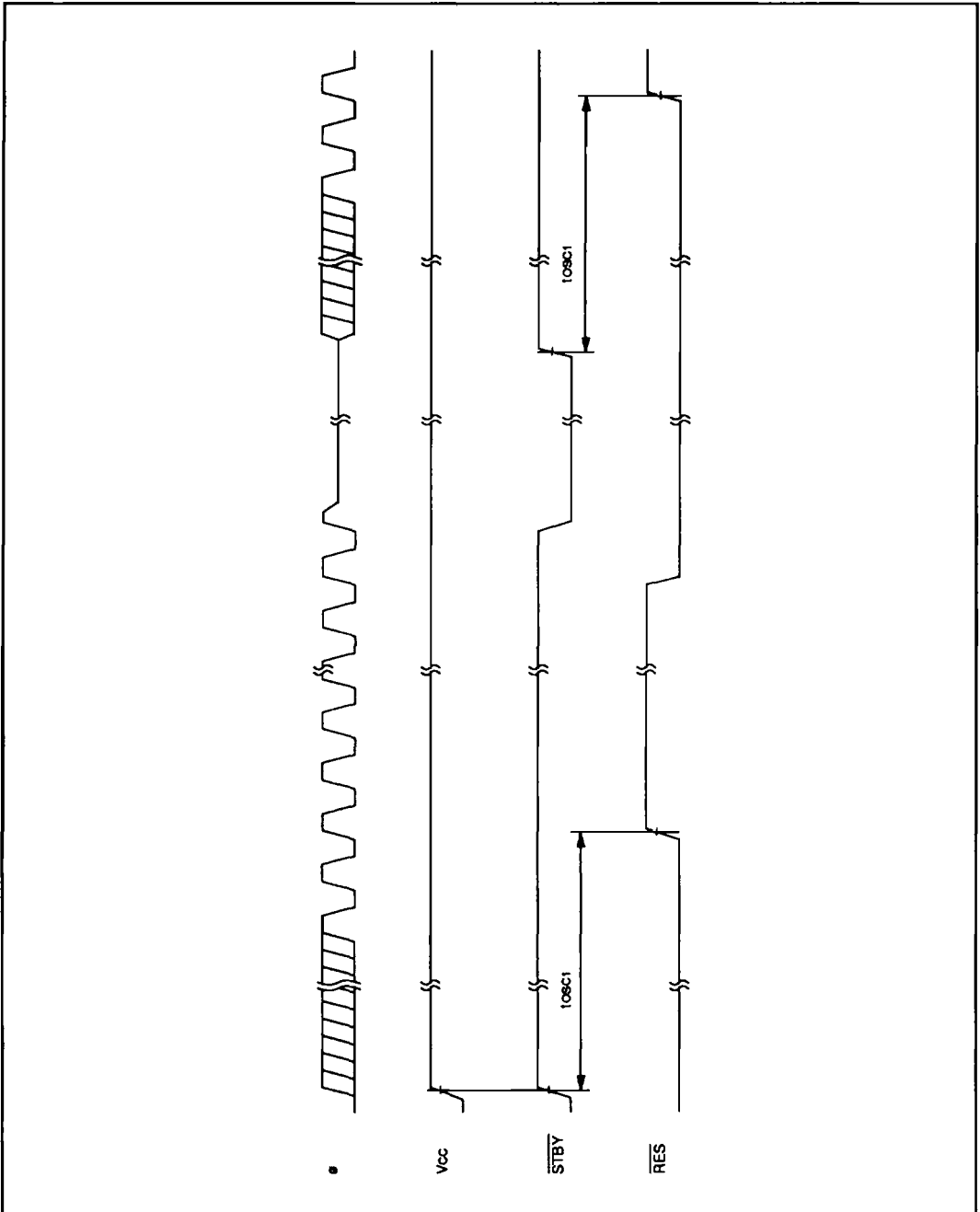


Figure 19-13 Clock Oscillator Stabilization Timing

19.3.4 I/O Port Timing

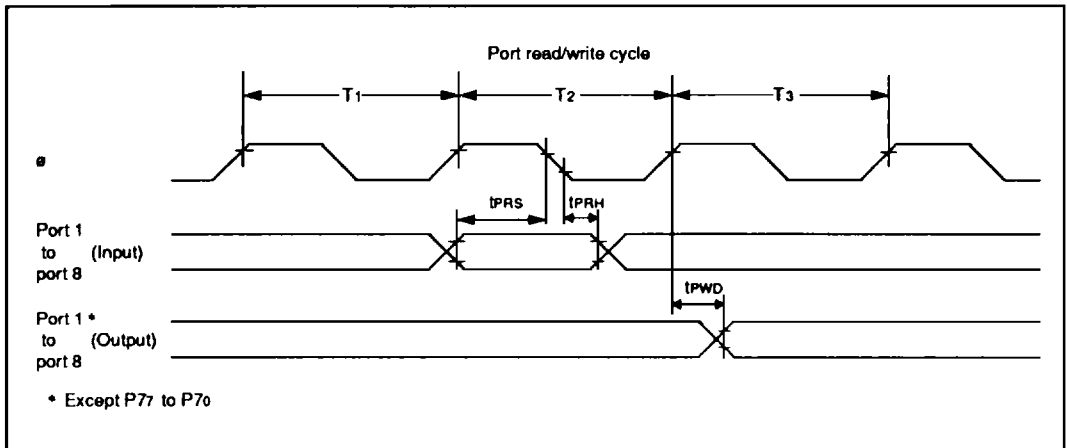


Figure 19-14 I/O Port Input/Output Timing

19.3.5 16-Bit Free-Running Timer Timing

1. Free-Running Timer Input/Output Timing

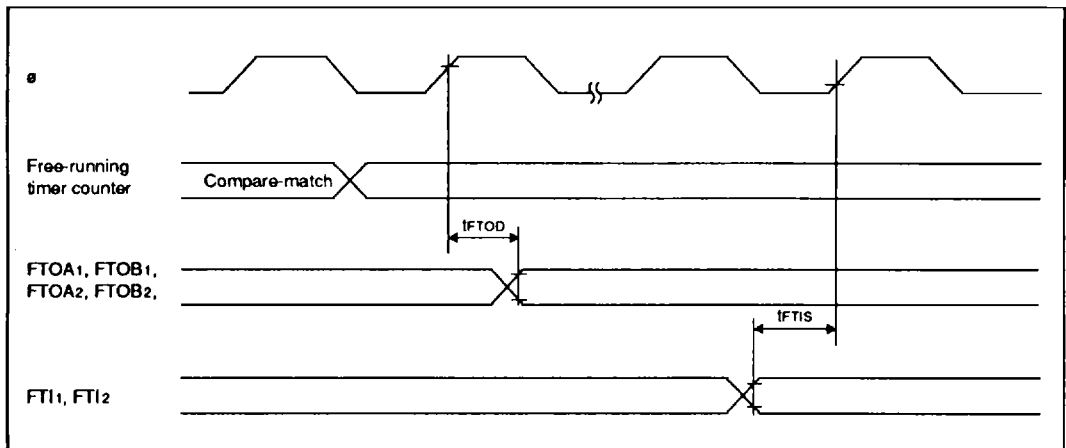


Figure 19-15 Free-Running Timer Input/Output Timing

2. External Clock Input Timing for Free-Running Timers

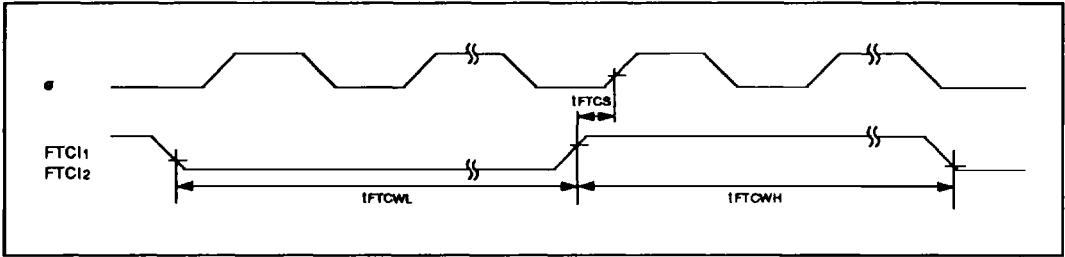


Figure 19-16 External Clock Input Timing for Free-Running Timers

19.3.6 8-Bit Timer Timing

1. 8-Bit Timer Output Timing

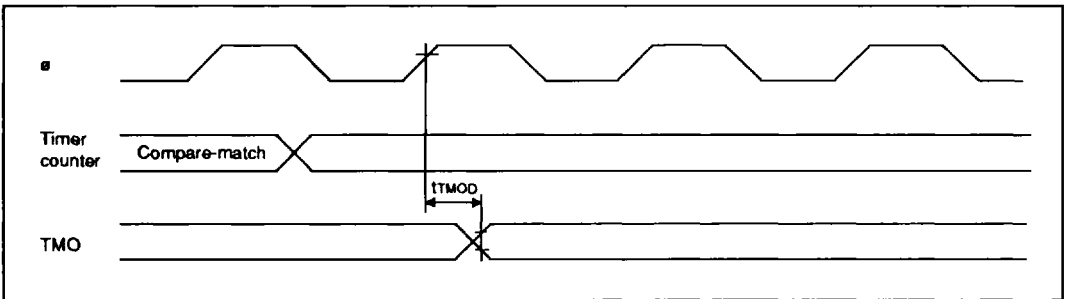


Figure 19-17 8-Bit Timer Output Timing

2. 8-Bit Timer Clock Input Timing

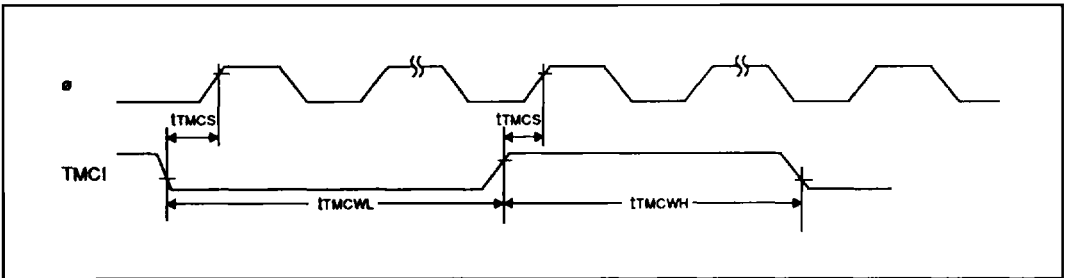


Figure 19-18 8-Bit Timer Clock Input Timing

3. 8-Bit Timer Reset Input Timing

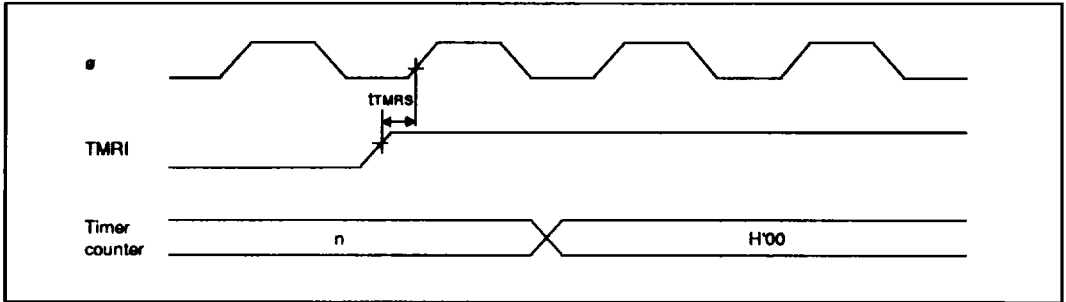


Figure 19-19 8-Bit Timer Reset Input Timing

19.3.7 Serial Communication Interface Timing

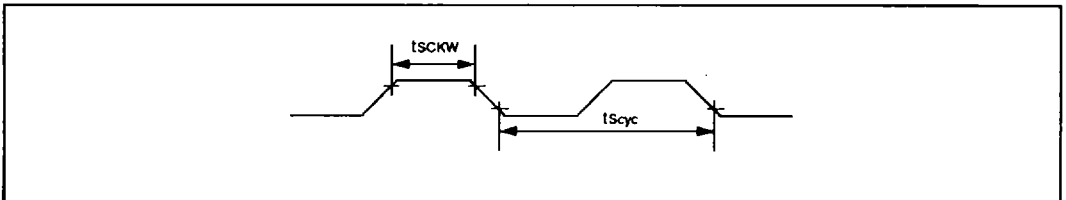


Figure 19-20 SCI Input Clock Timing

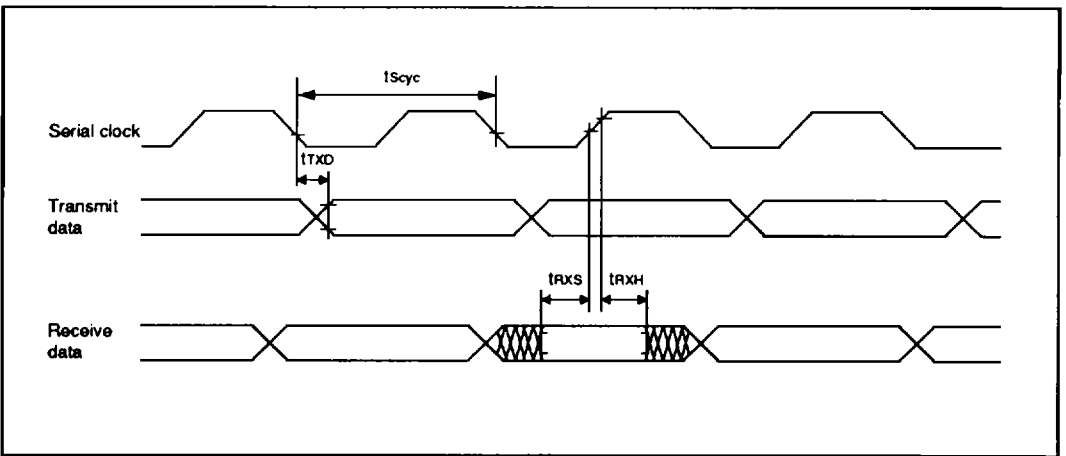


Figure 19-21 SCI Input/Output Timing (Synchronous Mode)

19.3.8 Refresh Timing

1. Basic Refresh Bus Cycle

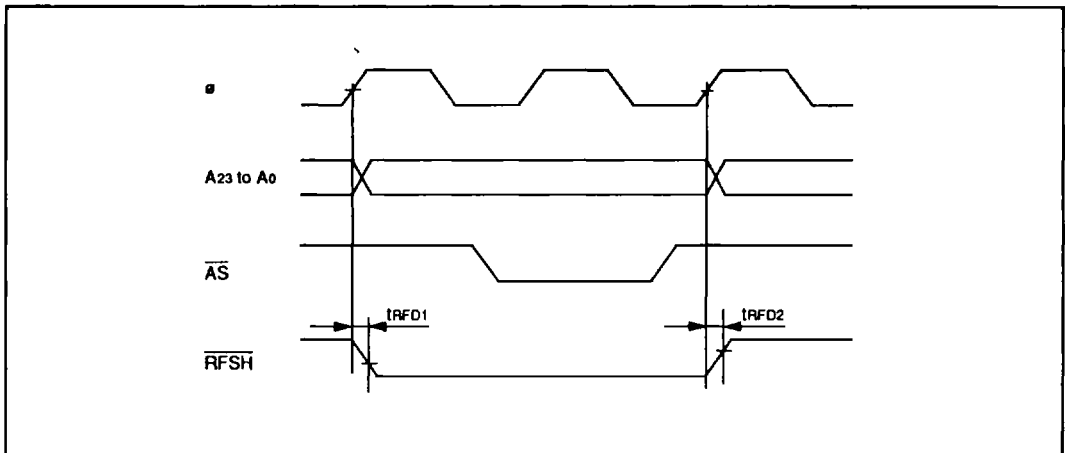


Figure 19-22 Basic Refresh Bus Cycle

2. Refresh Timing (Wait Cycle)

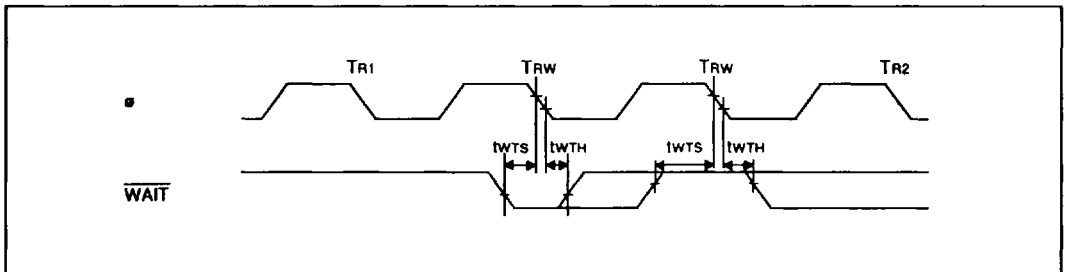


Figure 19-23 Refresh Timing (Wait Cycle)