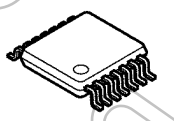
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MP97FT, TC7MP97FK
TC7MP98FT, TC7MP98FK

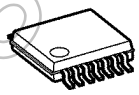
Low Voltage Triple Configurable Multiple Function Gate with 3.6 V Tolerant Inputs and Outputs

TC7MP97FT,TC7MP98FT



TSSOP14-P-0044-0.65A

TC7MP97FK,TC7MP98FK



VSSOP14-P-0030-0.50

Weight:
TSSOP14-P-0044-0.65A : 0.06 g(typ)
VSSOP14-P-0030-0.50 : 0.02 g(typ)

The TC7MP97,98 is a high performance CMOS multiple Function Gate which is guaranteed to operate from 1.2-V to 3.6-V. Designed for use in 1.5 V, 1.8 V, 2.5 V or 3.3 V systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

It independently consists of three circuits for Multiple Function Gate.

The output state is determined by seven patterns of 3-inputs.

The user can choose the functions of Multiplexer, AND, OR, NAND, Schmitt Inverter, and Schmitt Buffer.

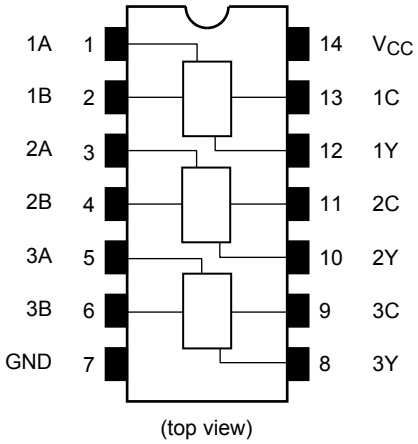
All inputs are equipped with protection circuits against static discharge.

Features

- Low-voltage operation : V_{CC} = 1.2 to 3.6 V
- High-speed operation : t_{pd} = 8.5 ns (max) (V_{CC} = 3.0 to 3.6 V)
  : t_{pd} = 12.0 ns (max) (V_{CC} = 2.3 to 2.7 V)
- Output current : |IOH|/IOL = ±8 mA (min) (V_{CC} = 3.0 V)
  : |IOH|/I_{OL} = ±4 mA (min) (V_{CC} = 2.3 V)
  : |IOH|/I_{OL} = ±1.5 mA (min) (V_{CC} = 1.65 V)
- Latch-up performance : -300 mA
- ESD performance : Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Package : VSSOP14 (US14),TSSOP14
- Power-down protection is provided on all inputs and outputs

Start of commercial production
2005-10

Pin Assignment (top view)



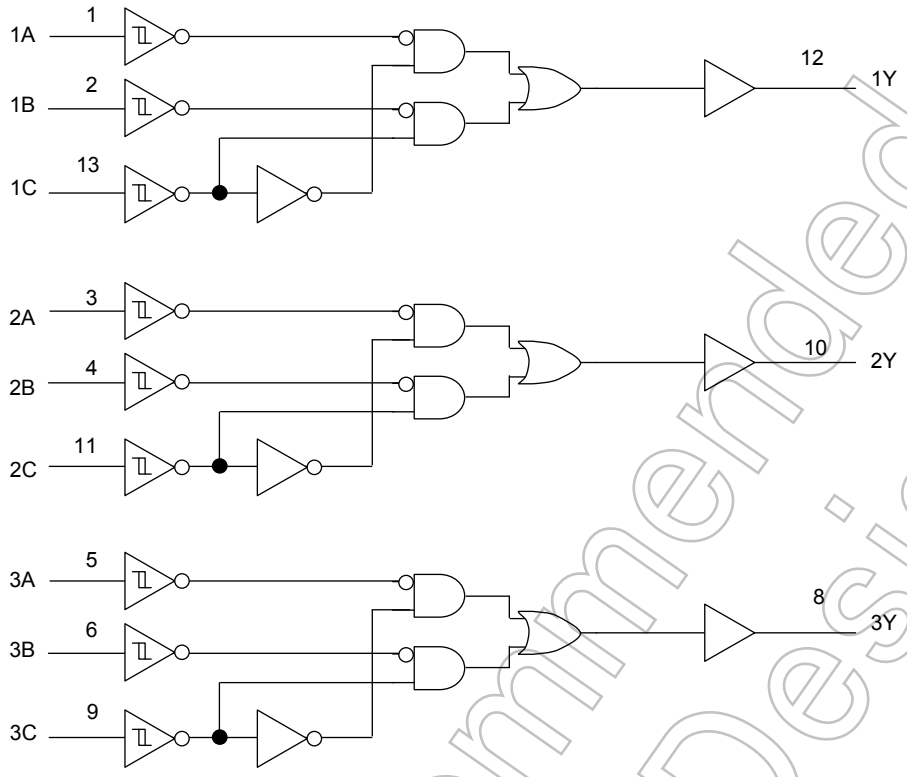
(top view)

Truth Table

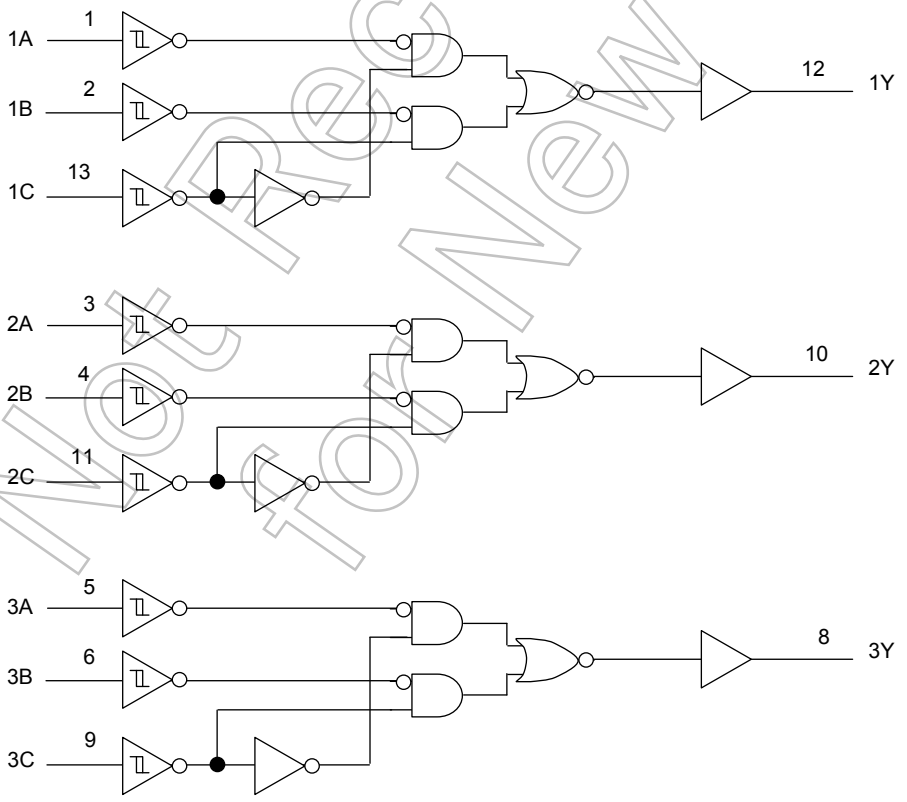
INPUTS			OUTPUT	
			TC7MP97	TC7MP98
A	B	C	Y	Y
L	L	L	L	H
L	L	H	L	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	H
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

System Diagram

TC7MP97

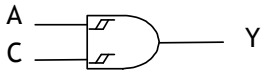
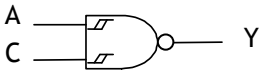


TC7MP98



Logic configrations(1/2)

<table>
<tr><th>Function</th><th>Input Condition</th><th>TC7MP97 Logic symbol</th><th>TC7MP98 Logic symbol</th><th>FUNCTION TABLE</th></tr>
<tr>
<td>MP97
AND

MP98
NAND</td>
<td>A=INPUT
B=L-Level
C=INPUT
Y=OUTPUT</td>
<td>  </td>
<td>  </td>
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<tr><th>97</th><th>98</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>H</td><td>L</td></tr>
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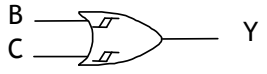
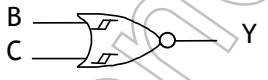
</td>
</tr>
<tr>
<td>MP97
OR

MP98
NOR</td>
<td>A=H-Level
B=INPUT
C=INPUT
Y=OUTPUT</td>
<td>  </td>
<td>  </td>
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<tr><td>H</td><td>L</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>H</td><td>L</td></tr>
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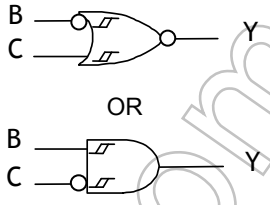
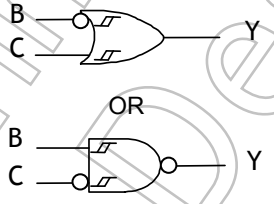
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td></tr>
</table>
</td>
</tr>
<tr>
<td>MP97
Schmitt INV+NOR
or
Schmitt INV+AND

MP98
Schmitt INV+OR
or
Schmitt INV+NAND</td>
<td>A=L-Level
B=INPUT
C=INPUT
Y=OUTPUT</td>
<td>  </td>
<td>  </td>
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<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
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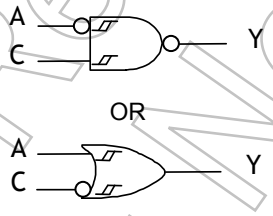
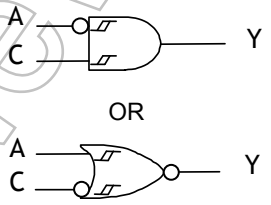
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>H</td></tr>
</table>
</td>
</tr>
<tr>
<td>MP97
Schmitt INV+NAND
or
Schmitt INV+OR

MP98
Schmitt INV+AND
or
Schmitt INV+NOR</td>
<td>A=INPUT
B=H-Level
C=INPUT
Y=OUTPUT</td>
<td>  </td>
<td>  </td>
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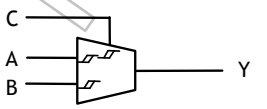
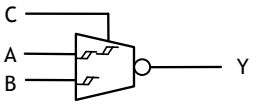
<tr><td>H</td><td>H</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td></tr>
</table>
</td>
</tr>
<tr>
<td>MP97
2 to 1 Selector

MP98
2 to 1 Selector+INV</td>
<td>A=INPUT
B=INPUT
C=Select
Y=OUTPUT</td>
<td>  </td>
<td>  </td>
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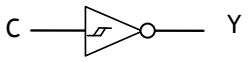
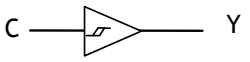
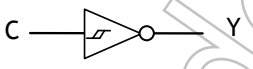
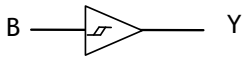
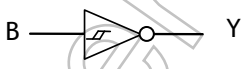
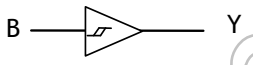
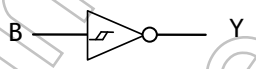
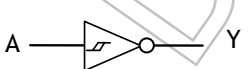
Logic configrations(2/2)

Function	Input Condition	TC7MP97 Logic symbol	TC7MP98 Logic symbol	FUNCTION TABLE
MP97 Schmitt INV MP98 Schmitt Buffer	A=L-Level B=H-Level C=INPUT Y=OUTPUT			A B C | Y (97 98) L H L | H L L H H | L H
MP97 Schmitt Buffer MP98 Schmitt INV	A=H-Level B=L-Level C=INPUT Y=OUTPUT			A B C | Y (97 98) H L L | L H H L H | H L
MP97 Schmitt Buffer MP98 Schmitt INV	A=L-Level B=INPUT C=L-Level Y=OUTPUT			A B C | Y (97 98) L L L | L H L H L | H L
MP97 Schmitt Buffer MP98 Schmitt INV	A=H-Level B=INPUT C=L-Level Y=OUTPUT			A B C | Y (97 98) H L L | L H H H L | H L
MP97 Schmitt Buffer MP98 Schmitt INV	A=INPUT B=L-Level C=H-Level Y=OUTPUT			A B C | Y (97 98) L L H | L H H L H | H L

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5 to 4.6	V
DC input voltage	V_{IN}	-0.5 to 4.6	V
DC output voltage	V_{OUT}	-0.5 to 4.6 (Note 2)	V
		-0.5 to V_{CC} + 0.5 (Note 3)	
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	±20 (Note 4)	mA
DC output current	I_{OUT}	±25	mA
Power dissipation	P_D	180	mW
DC V_{CC}/ground current	I_{CC}/I_{GND}	±25	mA
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: V_{CC} = 0 V

Note 3: High or Low state. I_{OUT} absolute ratiingmust be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	1.2 to 3.6	V
Input voltage	V_{IN}	−0.3 to 3.6	V
Output voltage	V_{OUT}	0 to 3.6 (Note 2)	V
		0 to V_{CC} (Note 3)	
Output current	I_{OH}/I_{OL}	±8.0 (Note 4)	mA
		±4.0 (Note 5)	
		±1.5 (Note 6)	
Operating temperature	T_{opr}	−40 to 85	°C

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 2: V_{CC} = 0 V

Note 3: High or low state

Note 4: V_{CC} = 3.0 to 3.6 V

Note 5: V_{CC} = 2.3 to 2.7 V

Note 6: V_{CC} = 1.65 to 1.8 V

Electrical Characteristics

DC Characteristics (Ta = –40 to 85°C)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_P	—		1.2		1.10	V
					1.4		1.20	
					1.65		1.35	
					2.3		1.70	
					3.0		2.00	
					3.6		2.20	
	L-level	V_N	—		1.2	0.10		V
					1.4	0.20		
					1.65	0.30		
					2.3	0.50		
					3.0	0.70		
					3.6	0.80		
Hysteresis voltage		V_H	—		1.2	0.2	0.9	V
					1.4	0.2	0.9	
					1.65	0.2	0.95	
					2.3	0.3	1.0	
					3.0	0.3	1.2	
					3.6	0.3	1.2	
Output voltage	H-level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –100 μA	1.2 to 1.3	V_{CC} - 0.1	—	V
				I_{OH} = –500 μA	1.4 to 1.6	V_{CC} - 0.2	—	
				I_{OH} = –1.5 mA	1.65 to 1.95	V_{CC} - 0.3	—	
				I_{OH} = –4.0 mA	2.3 to 2.7	V_{CC} - 0.4	—	
				I_{OH} = –8.0 mA	3.0 to 3.6	2.40	—	
	L-level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 100 μA	1.2 to 1.3	—	0.10	
				I_{OL} = 500 μA	1.4 to 1.6	—	0.20	
				I_{OL} = 3.0 mA	1.65 to 1.95	—	0.25	
				I_{OL} = 4.0 mA	2.3 to 2.7	—	0.40	
				I_{OL} = 8.0 mA	3.0 to 3.6	—	0.40	
Input leakage current		I_{IN}	V_{IN} = 0 to 3.6 V		1.2 to 3.6	—	±5.0	μA
Power-off leakage current		I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	$V_{IN} = V_{CC}$ or GND		1.2 to 3.6	—	20.0	μA
			$V_{CC} \leq V_{IN} \leq 3.6$ V		1.2 to 3.6	—	±20.0	
Increase in I_{CC} per input		ΔI_{CC}	$V_{IH} = V_{CC} - 0.6$ V		2.7 to 3.6	—	750	

AC Characteristics (Ta = –40 to 85°C, input: $t_r = t_f = 3.0$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Propagation delay time (A, B,C-Y)	t_{pLH} t_{pHL}	Figure 1, Figure 2 CL = 10pF、R_L = 1MΩ	1.8± 0.15	1.0	21.0	ns
			2.5 ± 0.2	0.8	10.0	
			3.3 ± 0.3	0.6	7.0	
	t_{pLH} t_{pHL}	Figure 1, Figure 2 CL = 15pF、R_L = 1MΩ	1.8± 0.15	1.0	23.0	ns
			2.5 ± 0.2	0.8	11.0	
			3.3 ± 0.3	0.6	7.7	
	t_{pLH} t_{pHL}	Figure 1, Figure 2 CL = 30pF、R_L = 1MΩ	1.8± 0.15	1.0	27.0	ns
			2.5 ± 0.2	0.8	12.0	
			3.3 ± 0.3	0.6	8.5	

Dynamic Switching Characteristics (Ta = 25°C, input: $t_r = t_f = 3.0$ ns, $C_L = 30$ pF)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note)	1.8	0.25	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note)	2.5	0.6	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note)	3.3	0.8	
Quiet output minimum dynamic V_{OL}	V_{OLV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note)	1.8	–0.25	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note)	2.5	–0.6	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note)	3.3	–0.8	
Quiet output minimum dynamic V_{OH}	V_{OHV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note)	1.8	1.5	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note)	2.5	1.9	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note)	3.3	2.2	

Note: Parameter guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	1.8, 2.5, 3.3	6	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz (Note)	1.8, 2.5, 3.3	30	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

AC Test Circuit

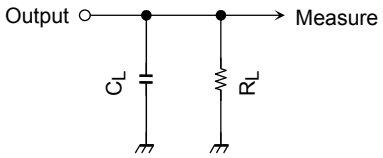


Figure 1

AC Waveform

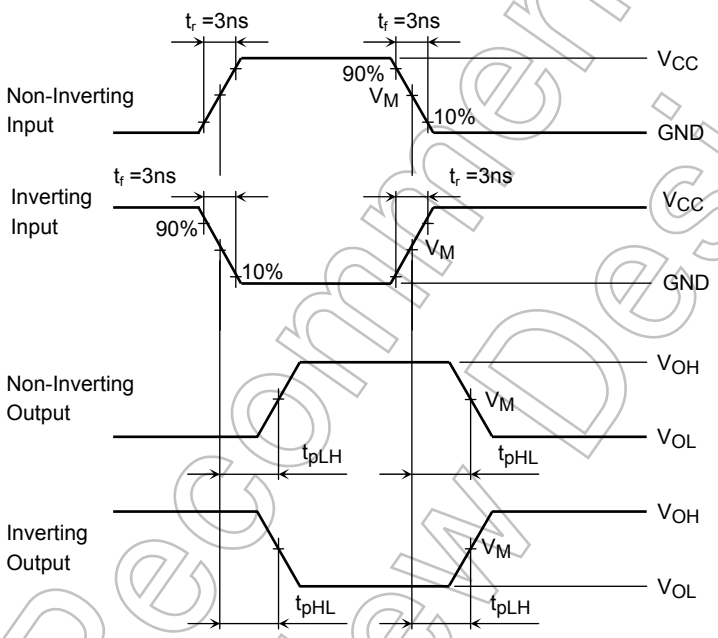
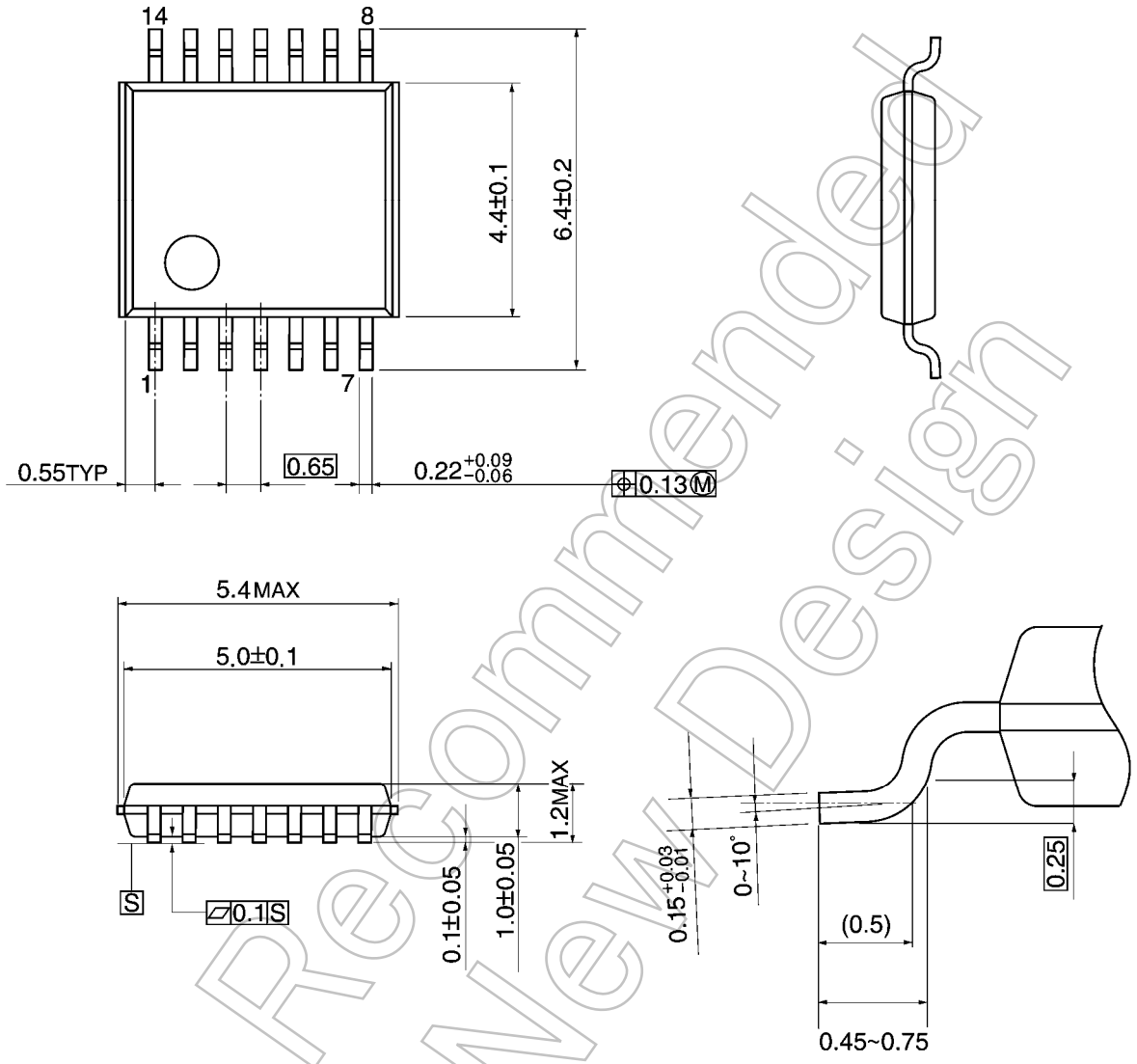


Figure 2 t_{pLH}, t_{pHL}

Symbol	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V± 0.15 V
V_{IN}	V_{CC}	V_{CC}	V_{CC}
V_M	1.5 V	V_{CC}/2	V_{CC}/2

Package Dimensions

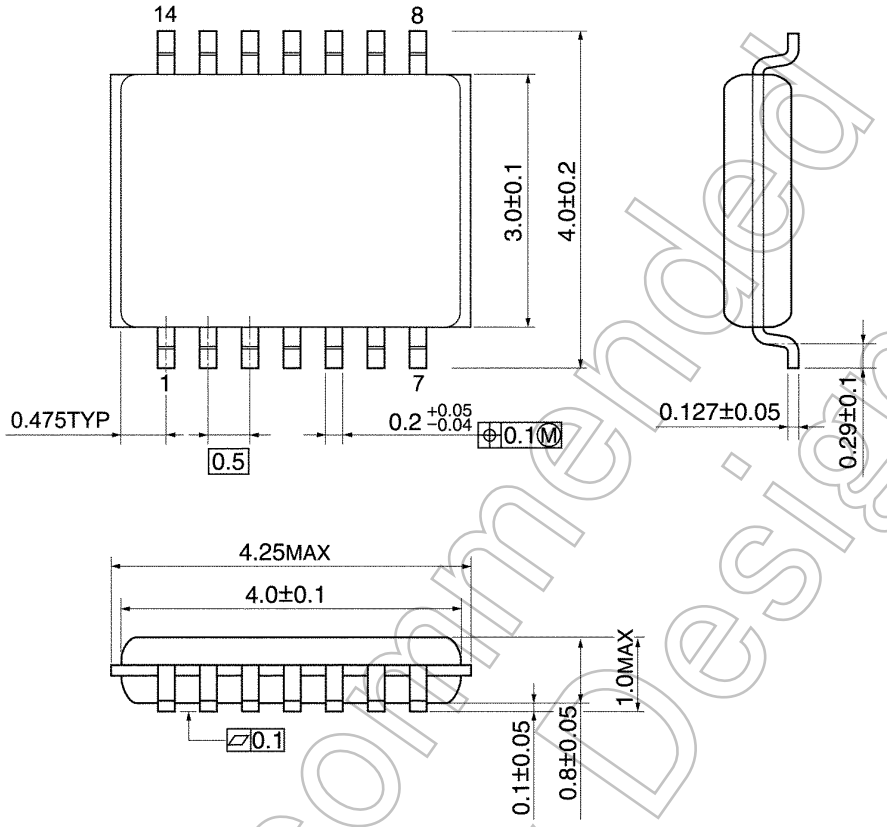
TSSOP14-P-0044-0.65A Unit: mm



Weight: 0.06 g (typ.)

Package Dimensions

VSSOP14-P-0030-0.50 Unit: mm



Weight: 0.02 g (typ.)

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