

# Am4055/5055 • Am4056/5056 • Am4057/5057

## Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers

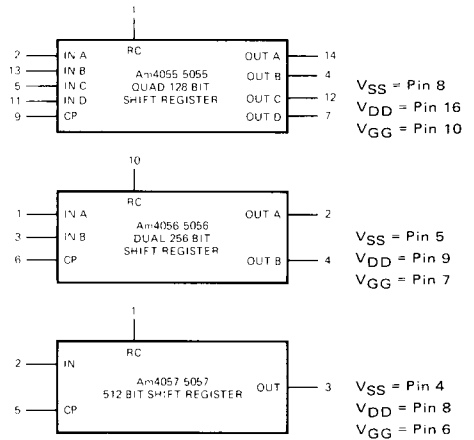
### Distinctive Characteristics

- Internal recirculate
- Single TTL compatible clock
- Operation guaranteed from DC to 1.5MHz
- 100% reliability assurance testing in compliance with MIL-STD-883

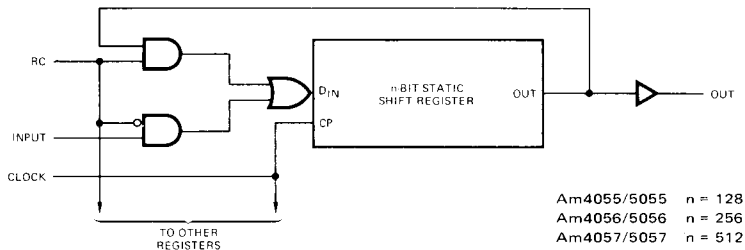
### FUNCTIONAL DESCRIPTION

These devices are a family of static P-channel MOS shift registers in three configurations. The Am4055/5055 is a quad 128-bit register; the Am4056/5056 is a dual 256-bit register; and the Am4057/5057 is a single 512-bit register. All three devices include on chip recirculate. The registers are all clocked by a single low-level clock input. Because the registers are static, the clock may be stopped indefinitely in the LOW state without loss of data. Each of the registers has a single data input; data on the input is written into the register on the HIGH-to-LOW clock edge. A single recirculate control (RC) on each chip determines whether the registers on that chip are to write data in from the data inputs or recirculate the data appearing on the output. If RC is LOW, new data is written in; if RC is HIGH then the data on the output will be written back into the register input on the next clock pulse.

### LOGIC SYMBOLS



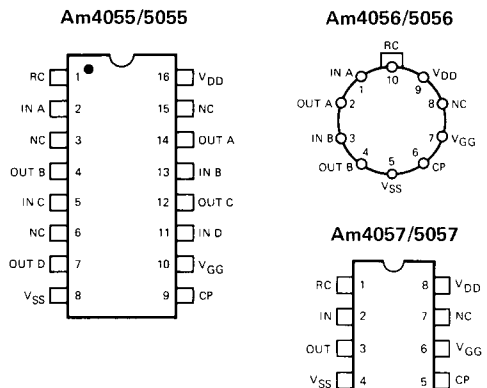
### LOGIC BLOCK DIAGRAM (One Register Shown)



### ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +70°C	MM5055N
16-Pin Hermetic DIP	0°C to +70°C	MM5055D
16-Pin Hermetic DIP	-55°C to +125°C	MM4055D
TO-100 Can	0°C to +70°C	MM5056H
TO-100 Can	-55°C to +125°C	MM4056H
8-Pin Molded DIP	0°C to +70°C	MM5057N
8-Pin Hermetic DIP	0°C to +70°C	MM5057D
8-Pin Hermetic DIP	-55°C to +125°C	MM4057D

### CONNECTION DIAGRAMS



**MAXIMUM RATINGS** (Above which the useful life may be impaired)

Storage Temperature	-65°C to +160°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V <sub>DD</sub> Supply Voltage	V <sub>SS</sub> -10V to V <sub>SS</sub> +0.3V
V <sub>GG</sub> Supply Voltage	V <sub>SS</sub> -20V to V <sub>SS</sub> +0.3V
DC Input Voltage	V <sub>SS</sub> -20V to V <sub>SS</sub> +0.3V

**OPERATING RANGE**

Part Number	Ambient Temperature	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>GG</sub>
Am4055 Am4056 Am4057	-55°C to +125°C	5.0V ±5%	0V	-12V ±5%
Am5055 Am5056 Am5057	0°C to +70°C	5.0V ±5%	0V	-12V ±5%

**ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE** (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Typ. (Note 1)			Units
			Min.	Max.	Units	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.5mA	2.4			Volts
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 1.6mA		0.4		Volts
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	4055/6/7 5055/6/7	V <sub>SS</sub> -1.0 V <sub>SS</sub> -1.5	V <sub>SS</sub> +0.3 V <sub>SS</sub> +0.3	Volts
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		V <sub>SS</sub> -18.5	V <sub>SS</sub> -4.2	Volts
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = -10.0V, all other pins GND, T <sub>A</sub> = 25°C		0.01	0.5	μA
I <sub>DD</sub>	V <sub>DD</sub> Power Supply Current	T <sub>A</sub> = 25°C, t <sub>φpwH</sub> = 160 ns	f ≤ 2.2MHz f ≤ 10KHz	15.0 13.0	20.0 18.0	mA
I <sub>GG</sub>	V <sub>GG</sub> Power Supply Current	Data = 1010. . . output open	f ≤ 1.6MHz	10.5	15.5	
			f ≤ 2.2MHz	13.0	19.0	
			f ≤ 10KHz	6.5	9.0	

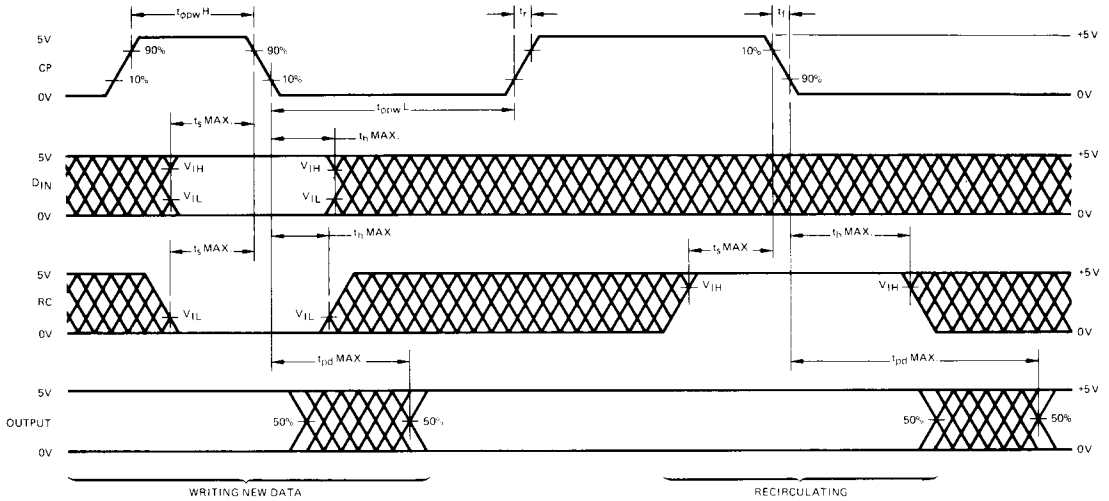
Note: 1. Typical Limits are at V<sub>SS</sub> = 5.0V, V<sub>GG</sub> = -12V, 25°C ambient.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE** (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Am4055/6/7			Am5055/6/7			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
f	Clock Frequency		0		1.0	0		1.5	MHz
t <sub>φpwH</sub>	Clock HIGH Time		0.4		1.0	0.23		100	μs
t <sub>φpwL</sub>	Clock LOW Time		0.4		∞	0.3		∞	μs
t <sub>r</sub> , t <sub>f</sub>	Clock Rise and Fall Times				200			200	ns
t <sub>s</sub>	Set-up Time, D or RC Inputs (see definitions)	t <sub>r</sub> = t <sub>f</sub> ≤ 10ns			260			110	ns
t <sub>h</sub>	Hold Time, D or RC Inputs (see definitions)	t <sub>r</sub> = t <sub>f</sub> ≤ 10ns			120			40	ns
t <sub>pd</sub>	Delay, Clock to Output LOW or HIGH	R <sub>L</sub> = 4k, C <sub>L</sub> = 10pF		350	700		250	345	ns
C <sub>in</sub>	Capacitance, Data and RC Inputs (Note 2)	f = 1MHz, V <sub>IN</sub> = V <sub>SS</sub>		4	7		4	7	pF
C <sub>φ</sub>	Capacitance, Clock Input (Note 2)	f = 1MHz, V <sub>IN</sub> = V <sub>SS</sub>			14			14	pF

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.  
3. At any temperature, t<sub>pd</sub> min. is always much greater than t<sub>h</sub> (D) max.

### TIMING DIAGRAM

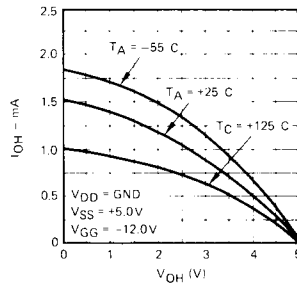


#### KEY TO TIMING DIAGRAM

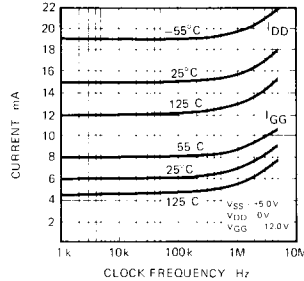
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

### PERFORMANCE CURVES

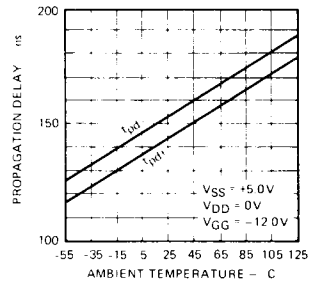
Typical Data Output  
HIGH Current  
Versus Data Output Voltage



Typical Power-Supply Currents  
Versus Frequency



Typical Propagation Delay  
Versus Ambient Temperature



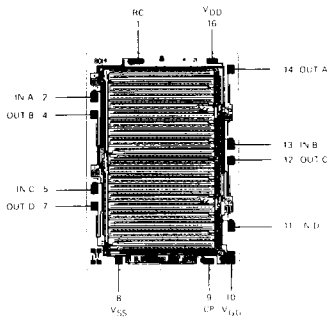
### DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

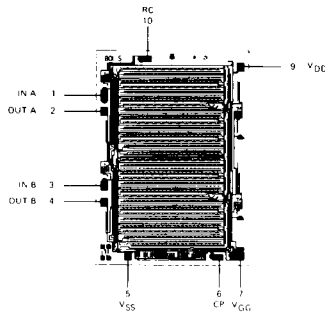
**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

**Metallization and Pad Layouts**

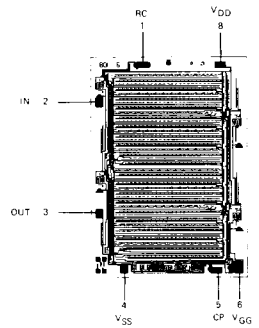
**Am4055/5055**



**Am4056/5056**



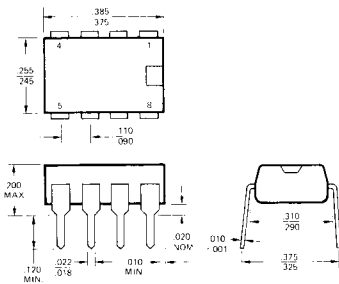
**Am4047/5057**



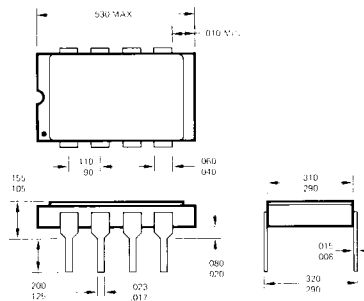
DIE SIZE 0.101" X 0.140"

**PHYSICAL DIMENSIONS  
Top Views**

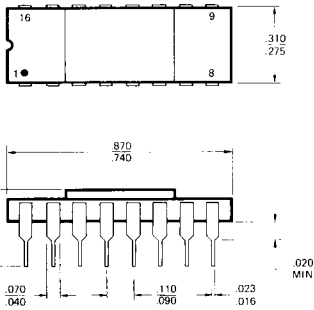
**8-Pin Molded DIP**



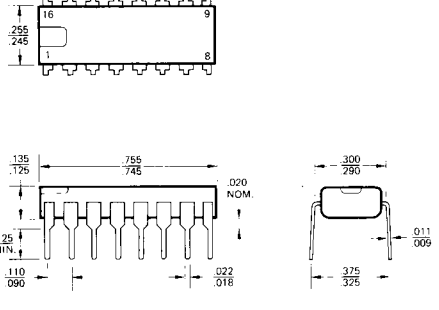
**8-Pin Hermetic DIP**



**16-Pin Side Brazed DIP**



**16-Pin Molded DIP**



**TO-100 Can**

