mosaic

Mosaic Semiconductor Inc.

PUMA 2U4000

PUMA 2U4000-12/15

Issue 1.2 : July 1993

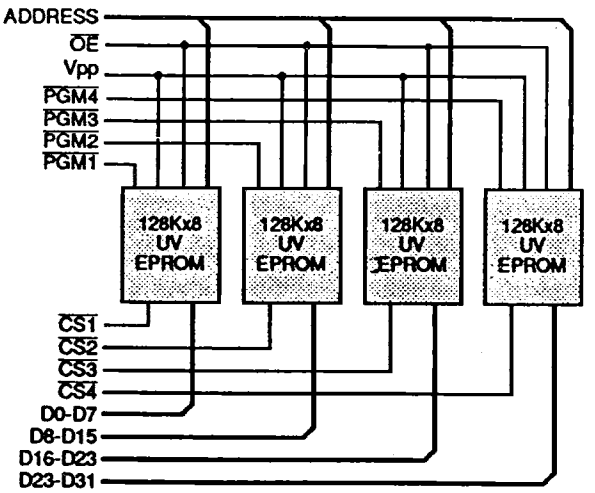
ADVANCE PRODUCT INFORMATION

4,194,304 bit CMOS High Speed UV EPROM

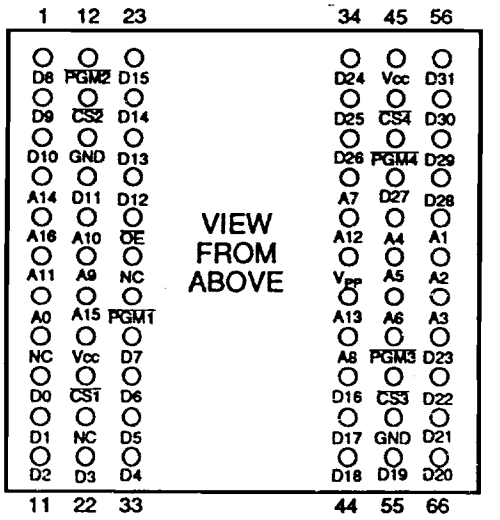
Features

Fast Access times of 120/150 ns
Pin grid array gives 2:1 improvement over DIL.
Package Suitable for Thermal Ladder Applications.
On board decoupling capacitors.
Configurable as 8 / 16 / 32 bit wide.
Operating Power 182 / 341 / 660 mW (max)
Standby Power 440 µW (max)
V_{PP} Voltage of 12.5±0.3V.
Complete Device Programming in 14 seconds (typ)
May be screened in accordance with MIL-STD-883.

Block Diagram



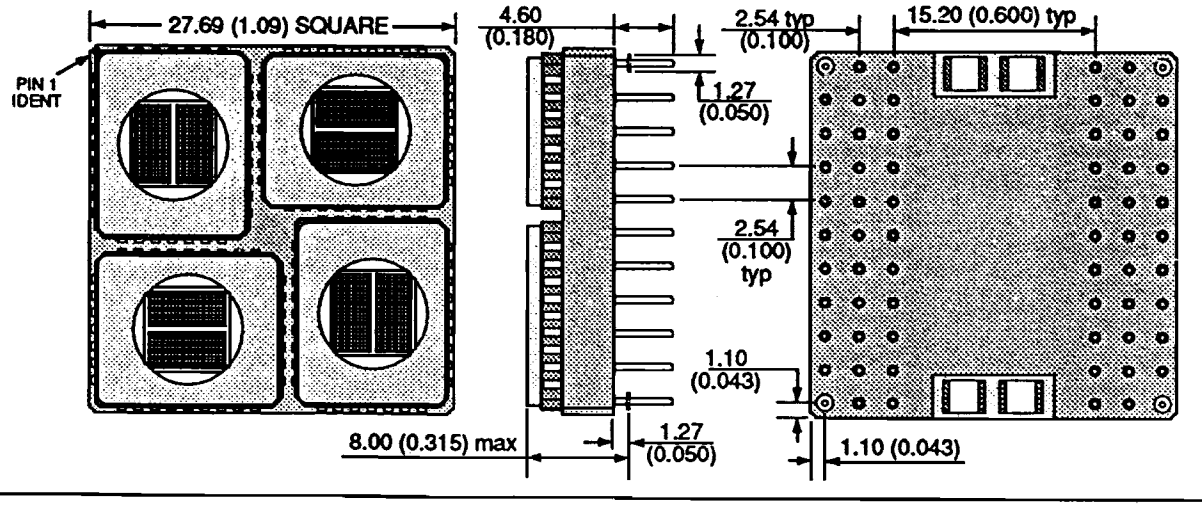
Pin Definition



Pin Functions

A0 - A16	Address Inputs
D0 - D31	Data Inputs/Outputs
$\overline{CS1\text{-}4}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{PGM1\text{-}4}$	Program Enable
NC	No Connect
V_{PP}	Programming Voltage
V_{CC}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



Absolute Maximum Ratings (1)

Voltage on pins V_{PP} and A_9 (2)	V_{TPP}	-0.6V to +13.5	V
Voltage on pin V_{CC}	V_{TCC}	-0.6V to +7.0	V
Voltage on any other pins (2)	V_T	-0.6V to +7.0	V
Power Dissipation	P_T	2	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) Pulse width -1.0V for less than 50 ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.75	5.0	6.25	V
DC Program Voltage	V_{PP}	12.2	12.5	12.8	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+1(2)	V
Input Low Voltage	V_{IL}	-0.3(1)	-	0.8	V
Operating Temperature	T_A	0	-	70	°C (2U4000)
	T_{AI}	-40	-	85	°C (2U4000I)
	T_{AM}	-55	-	125	°C (2U4000M, MB)

Notes (1) Pulse width -1.0V for less than 50 ns.
(2) V_{CC}+1.5V for pulse width ≤20 ns. If V_{IH} is over the specified max. value, Read operation cannot be guaranteed.

Capacitance (V_{CC}=5V±5%, T_A=25°C)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*	
Input Capacitance	Address, $\overline{OE}$	C_{IN1}	V_{IN}=0V	-	40	pF	Note: These parameters are calculated and not measured.
	$\overline{PGM1-4}$, $\overline{CS1-4}$	C_{IN2}	V_{IN}=0V	-	10	pF	
I/O Capacitance	32 Bit Mode	$C_{I/O}$	$V_{I/O}$=0V	-	15	pF	

Operating Modes

This table shows the inputs required to control the operating modes of the EPROMs on the PUMA 2U4000.

Mode		$\overline{CS}$	$\overline{OE}$	$\overline{PGM}$	*A0*	*A9*	*Vpp*	*Vcc*	*Outputs*
Read		0	0	1	X	X	5V	5V	Data out
Output Disable		0	1	1	X	X	5V	5V	Floating
Standby		1	X	X	X	X	5V	5V	Floating
Program		0	1	0	X	X	12.5V	6V	Data in
Program Verify		0	0	1	X	X	12.5V	6V	Data out
Page Data Latch		1	0	1	X	X	12.5V	6V	Data in
Page Program		1	1	0	X	X	12.5V	6V	Floating
Program Inhibit		0	0	0	X	X	12.5V	6V	Floating
		0	1	1	X	X	12.5V	6V	
		1	0	0	X	X	12.5V	6V	
		1	1	1	X	X	12.5V	6V	
Identifier (NOTE 1)	Manufacturer	0	0	1	0	12V	X	5/6V	07_{HEX}
	Device Code	0	0	1	1	12V	X	5/6V	38_{HEX}

1 = V_{IH}
0 = V_{IL}
X = Don't Care

Notes (1) A1 - A8 = A10 - A16 = V_{IL}
(2) $\overline{CS}$ is accessed through $\overline{CS1-4}$, and $\overline{PGM}$ is accessed through $\overline{PGM1-4}$. For correct operation, $\overline{CS1-4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation. $\overline{PGM1-4}$ must also be operated in the same manner.

READ OPERATION

DC Electrical Characteristics (T_A=-55 to +125°C, V_{CC}=5V±5%, V_{PP}=V_{CC})

Parameter		*Symbol*	*Test Condition*	*min*	*typ*[2]	*max*	*Unit*
Input Leakage Current	Address, $\overline{OE}$	I_{LI1}	V_{IN}=0V to V_{CC}	-	-	8	µA
	Other Pins	I_{LI}	V_{IN}=0V to V_{CC}	-	-	2	µA
Output Leakage Current	32 bit	I_{OUT}	V_{OUT}=5.25V	-	-	2	µA
V_{PP} Leakage Current		I_{PP}	V_{PP}=5V	-	4	80	µA
Operating Supply Current	32 bit	I_{CC}	$\overline{CS}$[1]=V_{IL}, I_{OUT}=0 mA	-	-	120	mA
Average Supply Current	32 bit	I_{CC32}	f=10MHz, I_{OUT}=0mA	-	-	200	mA
	16 bit	I_{CC16}	As Above	-	-	102	mA
	8 bit	I_{CC8}	As Above	-	-	53	mA
Standby Supply Current	TTL	I_{SB}	$\overline{CS}$[1]= V_{IH}, I_{OUT}=0mA	-	-	4	mA
	CMOS	I_{SB1}	$\overline{CS}$[1]=V_{CC}-0.3V, 0.2V≥V_{IN}≥V_{CC}-0.2V	-	4	400	µA
Output LowVoltage		V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
Output HighVoltage		V_{OH}	I_{OH}=-1.0 mA	2.4	-	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1-4}$. These inputs must be operated simultaneoulsy for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) Typical figures measured at 25°C.

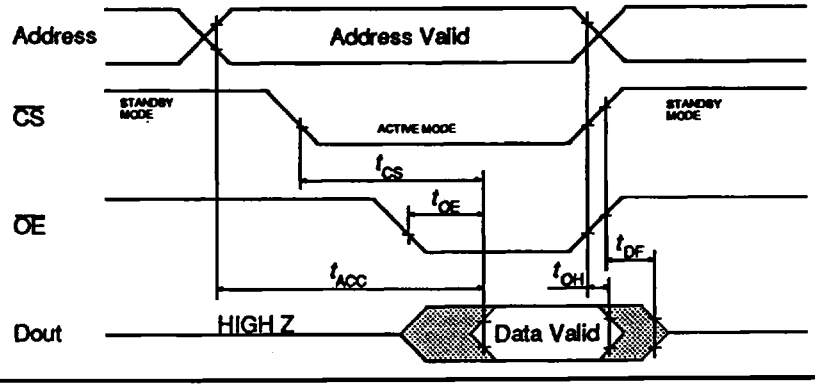
(3) **CAUTION:** the PUMA 2U4000 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.

AC Characteristics

Parameter	*Symbol*	*-12*		*-15*		*Unit*
		min	*max*	*min*	*max*	
Address to Output Delay	t_{ACC}	-	120	-	150	ns
Chip Select to Output Delay	t_{CS}	-	120	-	150	ns
Output Enable to Output Delay	t_{OE}	-	60	-	70	ns
OE or CS High to Output Float [1]	t_{DF}	0	50	0	60	ns
Output Hold from Address, CS or OE	t_{OH}	0	-	0	-	ns

Notes (1) t_{DF} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. This parameter is sampled and not 100% tested.

Read Cycle Timing Waveform



AC Test Conditions

*Input pulse levels: GND to 3.0V
*Input rise and fall times: 5 ns
*Input and Output timing reference levels: 1.5V
*Output load: 1 TTL gate + 100pF
*V_{CC}=5V±10%
*Module is tested in 32 bit mode.

PROGRAMMING OPERATION (The following information is provided for design purposes only.)

DC Electrical Characteristics (T_A= 25°C ±5°C, V_{CC}= 6.0V±0.25V, V_{PP} = 12.5V ±0.3V)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*[2]	*max*	*Unit*
V_{CC} Program Supply Current	32 bit	I_{CCP32}	Programming in operation	-	-	120	mA
	16 bit	I_{CCP32}	As Above	-	-	60	mA
	8 bit	I_{CCP32}	As Above	-	-	30	mA
V_{PP} Program Supply Current	32 bit	I_{PPB32}	Single Byte Programming	-	-	160	mA
	16 bit	I_{PPB16}	As Above	-	-	80	mA
	8 bit	I_{PPB8}	As Above	-	-	40	mA
	32 bit	I_{PPP32}	Page Mode Programming	-	-	200	mA
	16 bit	I_{PPP16}	As Above	-	-	100	mA
	8 bit	I_{PPP8}	As Above	-	-	50	mA
Identifier Select Voltage		V_H		11.5	12.0	12.5	V
Programming Voltage		V_{PP}		12.2	12.5	12.8	V
Supply Voltage		V_{CCP}		5.75	6.0	6.25	V
Output Low Voltage during verify		V_{OL}	I_{OL}=2.1 mA	-	-	0.45	V
Output High Voltage during verify		V_{oh}	I_{OH}=-400 µA	2.4	-	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1\text{-}4}$. These inputs must be operated simultaneoulsy for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) V_{CC} must be applied before V_{PP} and removed after V_{PP}.

(3) V_{PP} must not exceed 13.5V including overshoot.

(4) The transitions V_{IL} to 12.5V or 12.5V to V_{IL} are not allowed while $\overline{CS}$ = Low.

(5) When programming the PUMA 2U4000, a 0.1µF capacitor is required across V_{PP} and GND to suppress noise transients which may damage the device.

(6) **CAUTION:** The PUMA 2U4000 must not be removed from or inserted into a socket while V_{PP} or V_{CC} are applied.

AC Characteristics

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Address Setup Time	t_{AS}	2	-	-	µs
Output Enable Setup Time	t_{OES}	2	-	-	µs
Output Enable Hold Time	t_{OEH}	2	-	-	µs
Data Setup Time	t_{DS}	2	-	-	µs
Address Hold Time	t_{AH}	0	-	-	µs
	t_{AHL}	2	-	-	µs
Data Hold Time	t_{DH}	2	-	-	µs
Output Enable High to Output Float Delay [1]	t_{DF}	0	-	130	ns
V_{PP} Setup Time	t_{VPS}	2	-	-	µs
V_{CC} Setup Time	t_{VCS}	2	-	-	µs
Program Initial Program Pulse Width[2]	t_{PW}	0.19	0.2	0.21	ms
Program Overprogram Pulse Width [3]	t_{OPW}	0.19	-	5.25	ms
Data Valid from Output Enable	t_{OE}	0	-	150	ns
Program Setup Time	t_{PGMS}	2	-	-	µs
Chip Select Setup Time	t_{CES}	2	-	-	µs
Chip Select Hold Time	t_{CSH}	2	-	-	µs
Output Enable Pulse Width during Data Latch	t_{LW}	1	-	-	µs

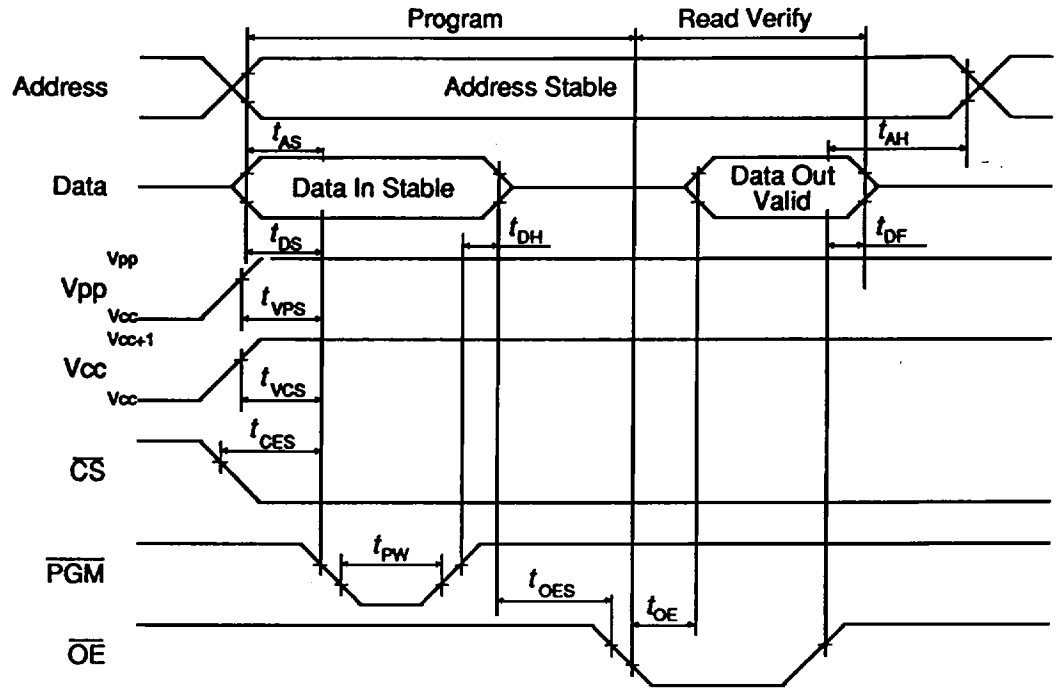
Notes (1) Defines the time at which the output achieves the open circuit condition and is no longer driven.

(2) Initial program pulse width tolerance is 0.2 ms± 5%.

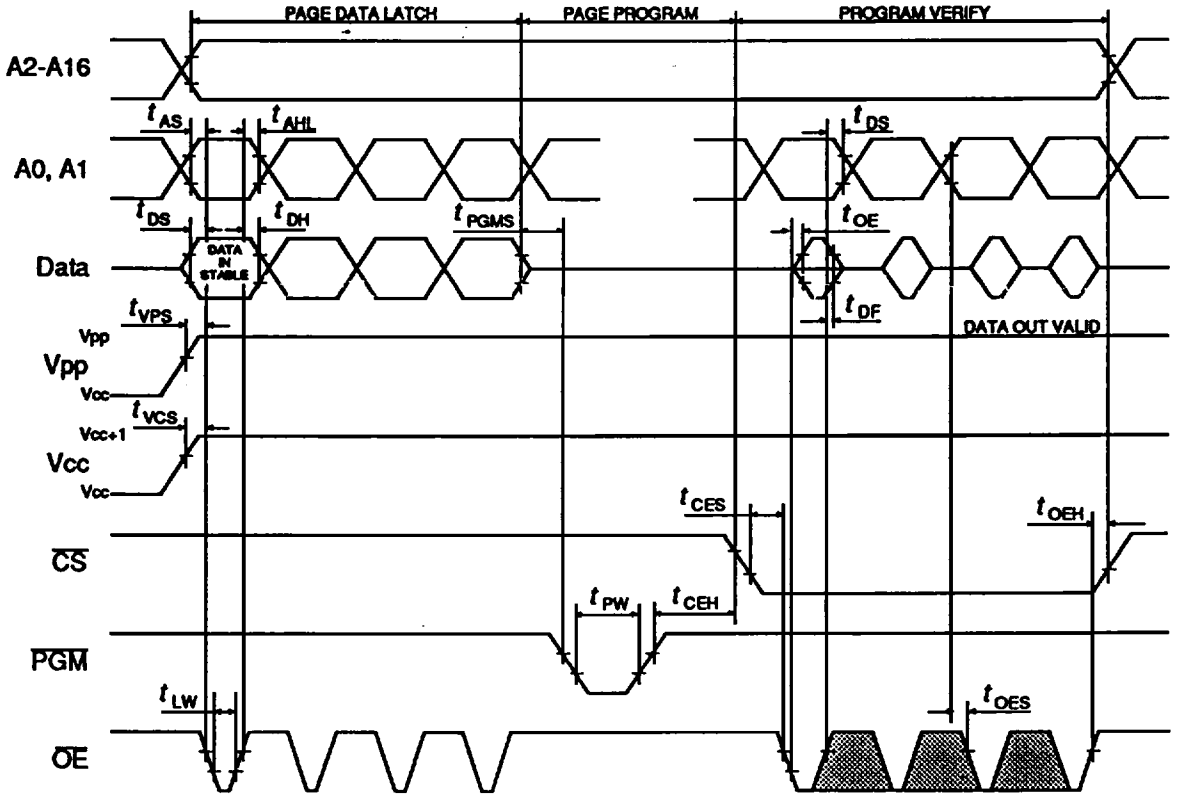
(3) Length of this pulse may vary as a function of the iteration counter value n.

Programming Cycle Timing Waveforms

Single Byte Programming



Page Mode Programming



High Performance Programming Algorithm

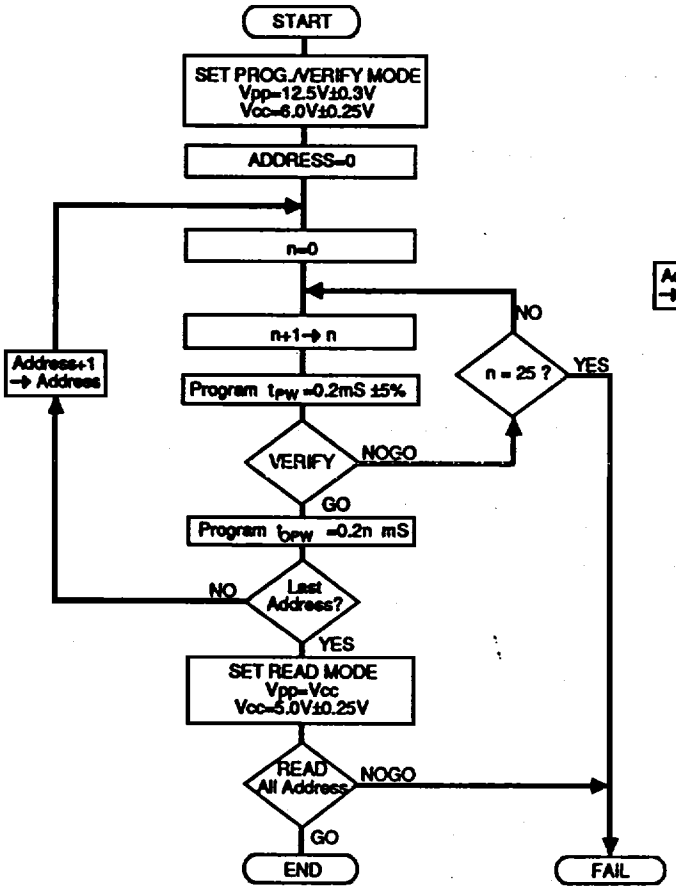
The PUMA 2U4000 can be programmed using either of the alogorithms shown below. These allow faster programming times without stressing the device or causing deterioration in Data Retention Time. Two methods are described here, Single Byte and Page Mode; see the Truth Table on page 2 for selction of these modes.

A,though each flow chart specifically refers to a single EPROM, all four devices on the PUMA can be programmed simultaneously in 32 bit mode, in pairs in 16 bit mode or singly in 8 bit mode.

Note that the parts used on this module are Hitachi 27C101A; this information, together with the device identifier code, should allow the correct programming alogorithm to be selected automatically.

Single Byte

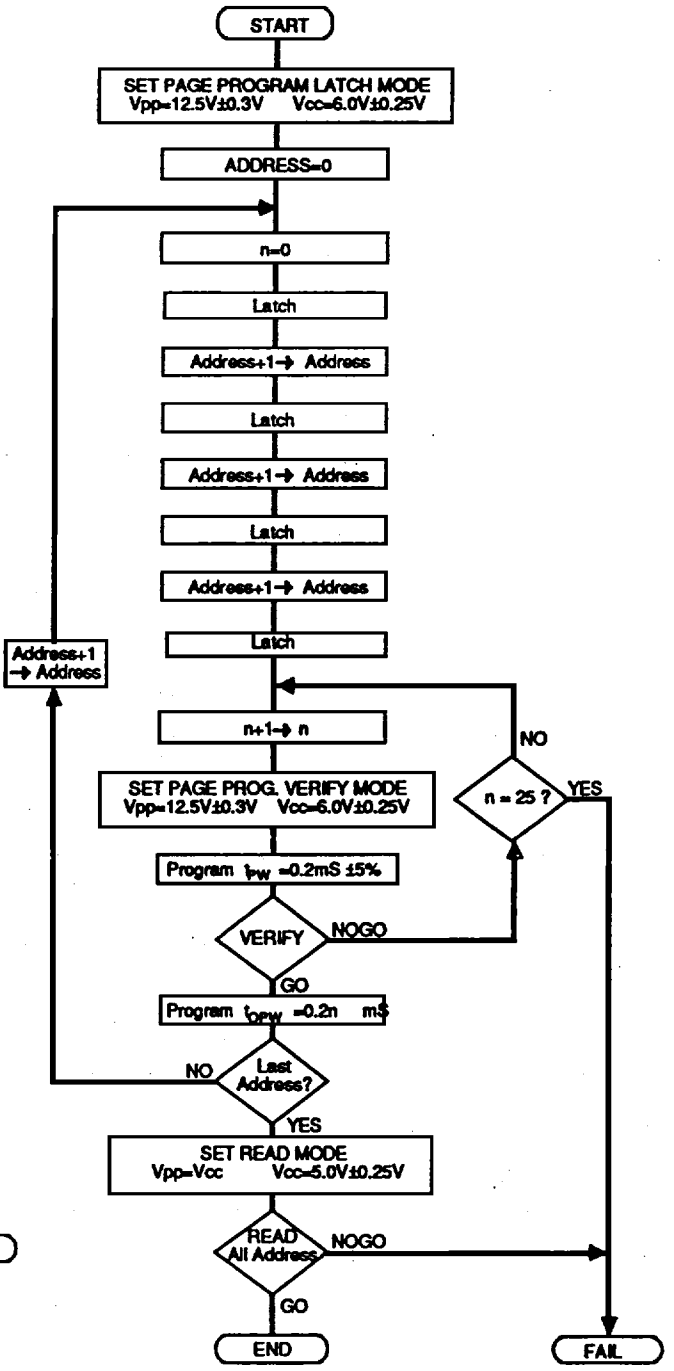
When the Program logic conditions are satisfied, the location is designated by A0 - A16, and the data to be programmed is applied 8 bits in parallel on D0 - D7. In this state, Byte programming is completed when $\overline{PGM}$ is at a low level.



NOTE: THE ALGORITHMS SHOWN HERE MUST BE USED TO ENSURE CORRECT PROGRAMMING OF THE PUMA 2U4000. THIS MAXIMISES THE DATA RETENTION TIME OF THE DEVICE AND DOES NOT STRESS THE MEMORY CELLS.

Page Mode

Page Mode allows up to 16 bytes of data to be simultaneously programmed. The destination address for a Page Programming operation must reside on the same page i.e. A2 - A16 must not change. When the logic conditions in the Truth Table are satisfied, Page Mode Programming is activated. The four locations in the same page are designated by A0 - A1, and the data is applied in parallel on D0 - D7. In this state the data latch (4 bytes) is completed, and the data is programmed when $\overline{OE}$ is high. Programming is completed when $\overline{PGM}$ is low.



PROGRAMMING NOTES

Upon delivery, or after each erasure, the MUM8128W has all 1,048,576 bits in the ONE or HIGH state. ZEROs are loaded into the devices through the procedure of programming.

This mode is entered when 12.5V is applied to the V_{PP} pin, V_{CC} is raised to 6.0V, $\overline{CS}$ and $\overline{PGM}$ are at V_{IL} and $\overline{OE}$ is at V_{IH}, as shown on the Table on page 2. Data may be applied in 8, 16 or 32 bits in parallel depending on how $\overline{CS1\text{-}4}$ and $\overline{PGM1\text{-}4}$ are controlled.

The algorithms reduce programming time by using 200µs pulses followed by byte verification to determine if the byte has been successfully programmed. If the data does not verify, up to 25 such pulses (n) can be applied, after which, if verification fails, programming stops. This proccess is repeated for each memory location within the PUMA 2U4000. After successful programming each memory location is given an over-program pulse of n times 0.2 ms duration to ensure that all bits have an adequate margin.

The algorithms program at V_{CC}=6.0V in order to ensure that each EPROM bit is programmed to a sufficiently high threshold voltage. After programming is complete, all bytes are compared with the original data with V_{CC}=5.0V±5%.

In order to overcome the voltage drop caused by the inductive effects of the printed circuit board on which the PUMA 2U4000 module is used, it is recommended that a 4.7µF electrolytic capacitor is used between V_{CC} and GND for every two PUMA modules. This capacitor should be placed close to the point where the power supply is routed to the UV EPROM array.

DEVICE IDENTIFIER MODE

The device identifier mode allows the reading out of a binary code from an EPROM which identify its manufacturer and specific type. It is intended to be used to automatically match the device to be programmed with the correct algorithm. This mode operates over the 25°C±5°C temperature range.

In order to activate this mode 12.0V±0.5V must be placed onto address line A9, after which two identifier bytes may be read by toggling A0 from V_{IL} to V_{IH}. All other address lines are held at V_{IL} during this sequence.

The manufacturer code is accessed with A0=V_{IL} and the device code with A0=V_{IH}; the values for these codes are given in the Operating Mode Table on page 2. Note that all identifiers for manufacturer and device codes will possess odd parity, with D7 defined as the parity bit.

ERASE

Complete erasure of the PUMA 2U4000 is performed by exposure to an ultraviolet light source giving a dosage of 15WS/cm². This dosage can be obtained by using an ultraviolet lamp with a wavelength of 2537 Å at a minimum intensity of 12,000µW/cm², for approximately 15 - 20 minutes. The MUM8128W should be directly under and about 1 inch from the light source.

Note that sunlight and fluorescent light may contain sufficient ultraviolet light to erase the programmed information. Although erasure times will be much longer at these levels, the transparent lids on this module should be covered with an opaque label to realise maximum system reliability.

Ordering Information

PUMA 2U4000MB-12

Speed	12	= 120 ns
	15	= 150 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Screened in accordance with MIL-STD 883C
Memory Type	U4000	= 128K x 32 UV EPROM (configurable as 256K x 16 or 512K x 8)

Note: For more information regarding screening flows contact Mosaic Semiconductor Inc. for a 'Screening Flow Applications note.'

mosaic
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