PARADIGM

256K Static RAM 64K x 4-Bit with Separate I/O

T-46-23-10

PDM41251S/L
PDM41252S/L

Features

- Separate data input and output pins
- High speed access times
  Com'l: 15, 20, 25, 35 and 45ns
  Mil : 20, 25, 35, 45, and 55ns
- Low power operation
  - PDM41258S
    Active: 400mW (typ.)
    Standby: 400 µW (typ.)
  - PDM41258L
    Active: 350mW (typ.)
    Standby: 100 µW (typ.)
- PDM41251: output track inputs during write mode
- PDM41252: high impedance outputs during write mode
- TTL compatible inputs and outputs
- Military product MIL-STD-883, Rev. C
- Packages
  Plastic dip - P
  Cerdip - D, Plastic SOJ - SO,
  Ceramic LCC - L28.

Description

The PDM41251 and PDM41252 are high performance CMOS static RAMs organized as 65,536 x 4 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing to this device is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW.

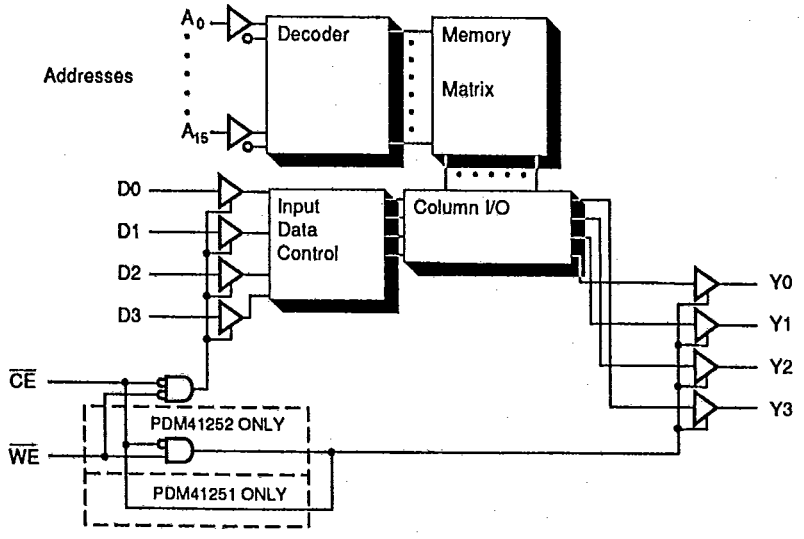
The PDM41251/2 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM41251 and PDM41252 each comes in two versions, the standard power version PDM41251S andPDM41252S and a low power version the PDM41251L and PDM41252L. The two versions are functionally the same and only differ in their power consumption.

The Paradigm 41 (static ram) family of products are functionally equivalent to manufacturers products meeting JEDEC standards. These products are manufactured and quality controlled in the U.S.A.

The PDM41251and PDM41252 are available in a 28-pin 300 mil DIP. The PDM41251 and PDM41252 are also available in a 28-pin LCC and a 28-pin SOJ for surface mount applications.

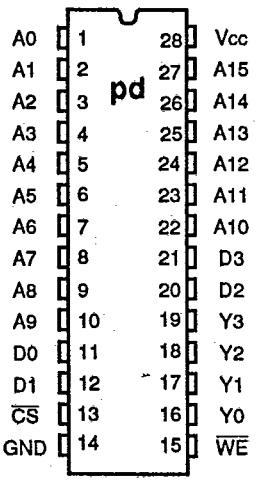
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Rev. C, making the PDM41251 and PDM41252 ideally suited for military temperature applications.

Functional Block Diagram

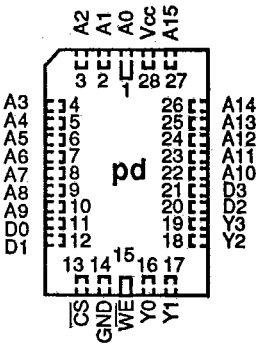


Pin Configuration

300 DIP
300 SOJ



LCC



PDM41251S/L
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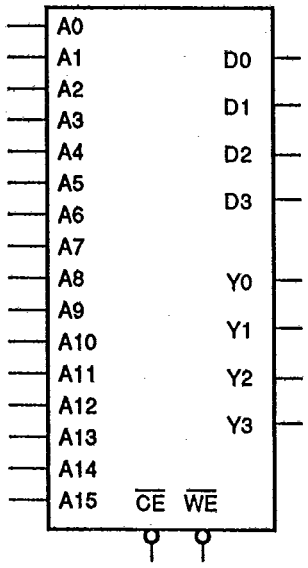
Logic Symbol



Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	OV	5.0V ± 10%
Commercial	0°C to +70°C	OV	5.0V ± 10%

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	--	5.5	V
V_{IL}	Input High Voltage	-0.5(1)	--	0.8	V

NOTE: 1. V_{IL}(min) = -3.0V for pulse width less than 20ns.

Absolute Maximum Ratings (1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	- 0.5 to + 7.0	- 0.5 to + 7.0	V
T_A	Operating Temperature	0 to + 70	- 55 to + 125	°C
T_{BIAS}	Temperature Under Bias	- 55 to + 125	- 65 to + 135	°C
T_{STG}	Storage Temperature	- 55 to + 125	- 65 to + 150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions		PDM41251S PDM41252S Min.	PDM41251S PDM41252S Max.	PDM41251L PDM41252L Min.	PDM41251L PDM41252L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	Vcc = MAX., V_{IN} = GND to Vcc	MIL.	--	10	--	5	µA
			Com'l.	--	5	--	2	
$\|I_{LO}\|$	Output Leakage Current	Vcc = MAX.	MIL.	--	10	--	5	µA
		$\overline{CE}$ = V_{IH}, V_{OUT} = GND to Vcc	Com'l.	--	5	--	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, Vcc = Min.		--	0.4	--	0.4	V
		I_{OL} = 10mA, Vcc = Min.		--	0.5	--	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, Vcc = Min.		2.4	--	2.4	--	V

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DC Electrical Characteristics[1] (V_{CC} = 5.0V ± 10%, V_{LC} ≤0.2V, V_{HC} ≥Vcc - 0.2)

Symbol	Parameter	Power	Function	15,[4] 20 Com'l.	20 MIL.	25, 30, 35, 45, 55 ns[5] Com'l.	MIL.	Unit
I_{CC}	Dynamic Operating Current $\overline{CE}$ = V_{IL}, Outputs Open, V_{CC} = Max., f=f MAX[3]	S	Read	180	180	160	160	mA
			Write[2]	180	180	160	160	
		L	Read	160	160	140	140	mA
			Write[2]	160	160	140	140	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CE}$ ≥V_{IH}, V_{CC} = Max., Outputs Open f=f MAX[3]	S	—	60	60	60	60	mA
		L	—	50	50	50	50	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CE}$ ≥ V_{HC}, V_{CC}= Max., f=0[3] V_{IN} ≥V_{HC} or ≤ V_{LC}	S	—	30	30	30	30	mA
		L	—	10	10	10	10	mA

NOTES:
1. All values are maximum guaranteed values.
2. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that in most systems the ratio of read cycles to write cycles is extremely high. When comparing these figures to those on other data sheets, we recommend that the read cycle data is used (especially where "Average" current consumption figures are specified).
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. This speed grade is available in Commercial grade product only.
5. This speed grade is available in Military grade product only.

Capacitance[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = OV	10	pf
C_{OUT}	Output Capacitance	V_{OUT} = OV	10	pf

NOTE 1: This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input pulse levels	GND to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

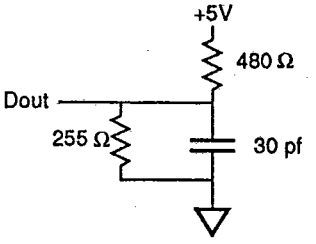

Fig. 1 Output Load Equivalent

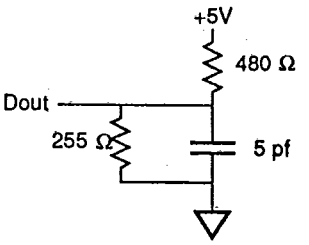

Fig. 2 Output Load Equivalent (for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE})

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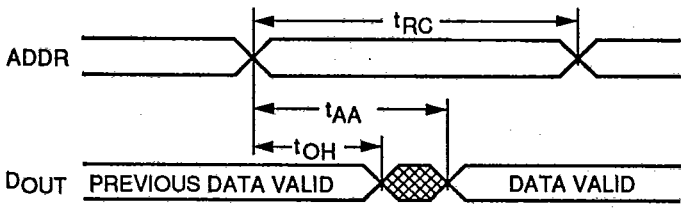
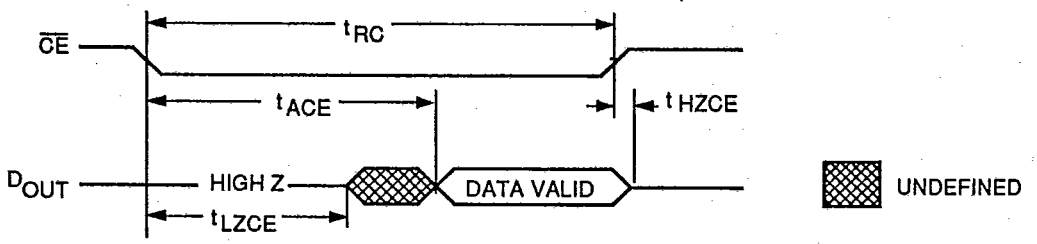
Read Cycle No. 1 (6, 7)



Read Cycle No. 2 (3, 6, 8)



AC Electrical Characteristics Vcc = 5V ± 10%, All Temperature Ranges

Description		-15 (9)		-20		-25		-35		-45		-55 (10)		
READ Cycle	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
READ cycle time	t_{RC}	15		20		25		35		45		55		ns
Address access time	t_{AA}		15		20		25		35		45		55	ns
Chip enable access time	t_{ACE}		15		20		25		35		45		55	ns
Output hold from address change	t_{OH}	3		3		5		5		5		5		ns
Chip enable to output in low Z (4)	t_{LZCE}	5		5		5		5		5		5		ns
Chip disable to output in high Z (2, 3, 4)	t_{HZCE}		10		10		15		20		20		25	ns
Chip enable to power up time (4)	t_{PU}	0		0		0		0		0		0		ns
Chip disable to power down time (4)	t_{PD}		15		20		25		35		45		55	ns

PRELIMINARY

NOTE : reference page 6 for all notes on this page

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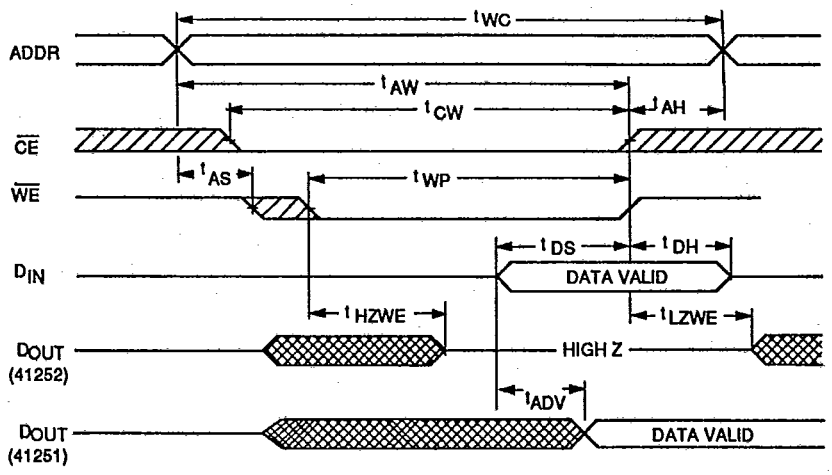
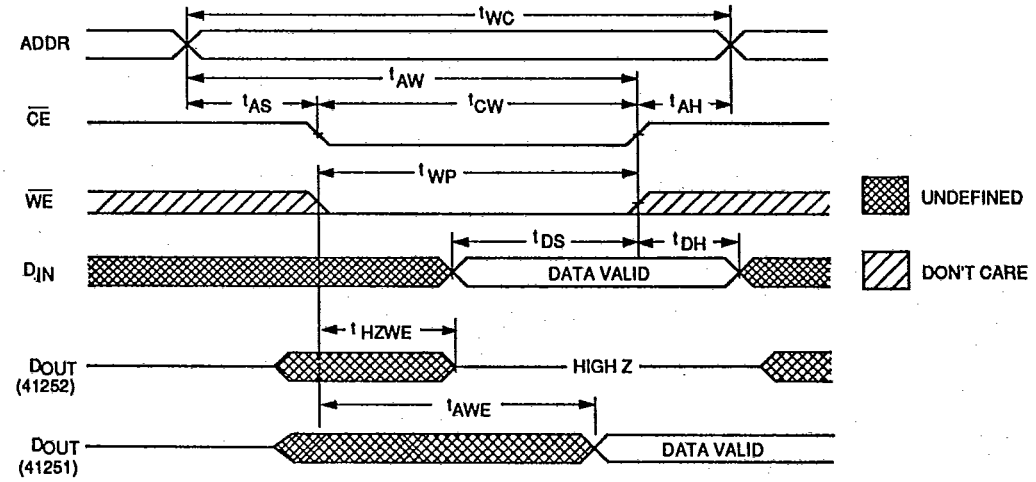
Write Cycle No. 1
(Write Enable Controlled)



Write Cycle No. 2
(Chip Enable Controlled)



AC Electrical Characteristics

Vcc = 5V ± 10%, All Temperature Ranges

Description		-15 (9)		-20		-25		-35		-45		-55 (10)		
WRITE Cycle	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
WRITE cycle time (4)	t_{WC}	15		20		25		35		45		55		ns
Chip enable to end of write (4)	t_{CW}	15		20		20		30		40		50		ns
Address Valid to end of write	t_{AW}	15		20		20		30		40		50		ns
Address set-up time	t_{AS}	0		0		0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns
Write pulse width	t_{WP}	15		20		20		25		30		35		ns
Data set-up time	t_{DS}	10		12		12		15		20		25		ns
Data hold time	t_{DH}	0		0		0		0		0		0		ns
Write disable to output in low Z (4) (41252)	t_{LZWE}	0		0		0		0		0		0		ns
Write enable to output in high Z (4) (41252)	t_{HZWE}		5		8		10		13		20		25	ns
Write enable to data valid (41251)	t_{AWE}	15		20		20		30		35		40		ns
Data valid to output valid (41251)	t_{ADV}	15		20		20		30		35		40		ns

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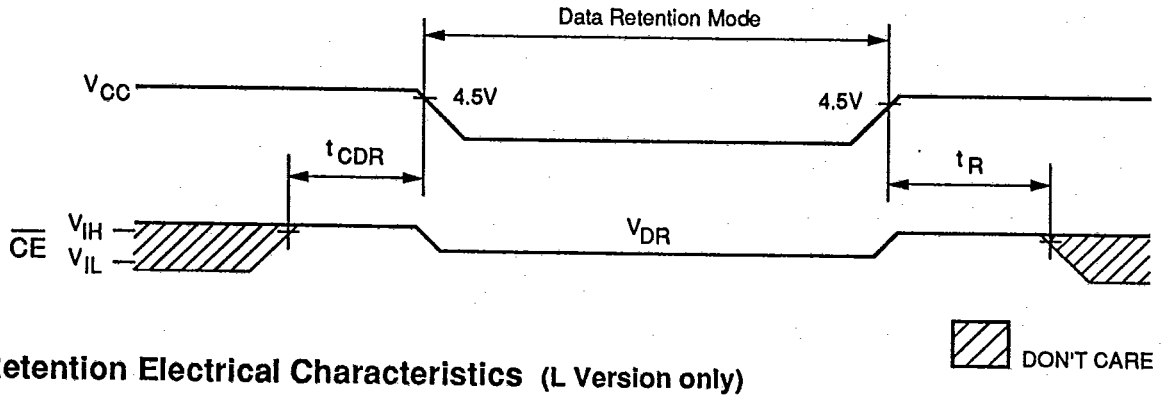
Low V_{CC} Data Retention Waveform



Data Retention Electrical Characteristics (L Version only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max	Unit
V_{DR}	Vcc for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq Vcc - 0.2V$	Vcc = 2V	—	95	500	µA
		$V_{IN} \geq Vcc - 0.2V$ or $\leq 0.2V$	Vcc = 3V	—	350	750	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(4)	Operation Recovery Time			t_{RC}(5)	—	—	ns

NOTES: (For pages 4,5 and 6)

1. Test conditions as specified with the output loading circuit as shown in Fig #1 unless otherwise noted.
2. T_{HZCE} and T_{HZWE} are tested with CL = 5pF as shown in Fig. #2. Transition is measured ±200mV from steady state voltage.
3. At any given temperature and voltage condition, T_{HZCE} is less than T_{LZCE}.
4. This parameter is sampled.
5. t_{RC} = Read cycle time.
6. $\overline{WE}$ is high for a READ cycle.
7. The device is continuously selected. All the Chip Enables are held in their state
8. The address is valid prior to or coincident with the latest occuring Chip Enable.
9. 0°C to +70°C temperature range only.
10. -55°C to +125°C temperature range only.

Truth Table (1) (V_{LC}=0.2V, V_{HC}=V_{CC}-0.2V)

$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	H	Hi-Z	Standby
H	L	D_{OUT}	Read
L	L	D_{IN}	Write (2)
L	L	Hi-Z	Write (3)

NOTE:
1. H = V_{IH}, L = V_{IL}, X = DON'T CARE.
2. For PDM41251 only.
3. For PDM41252 only.

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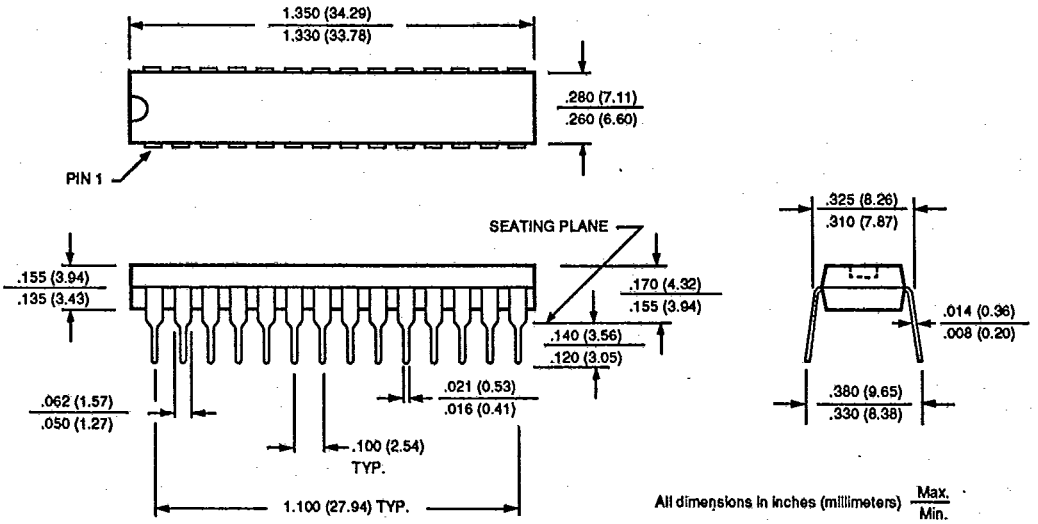
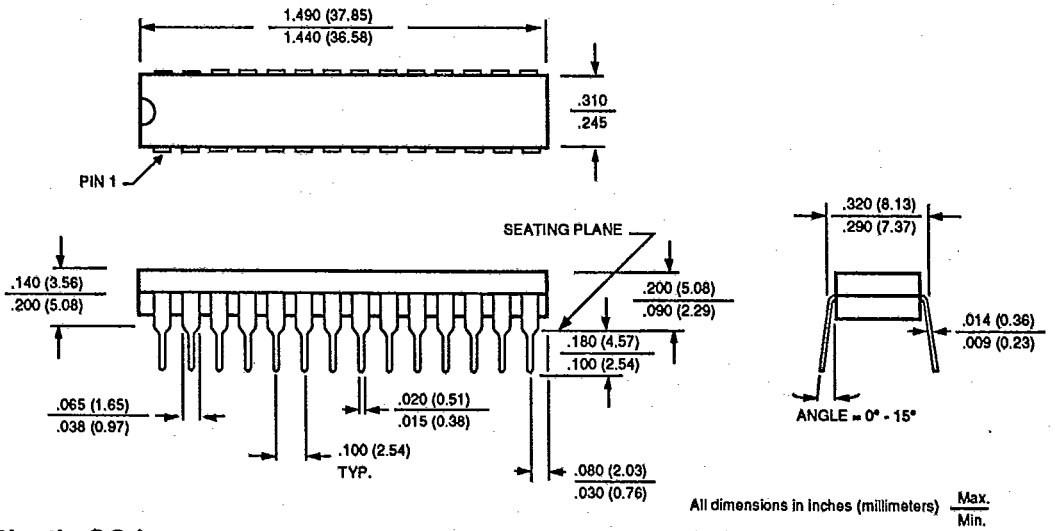
PDM41252S/L

28 Pin Plastic Dip



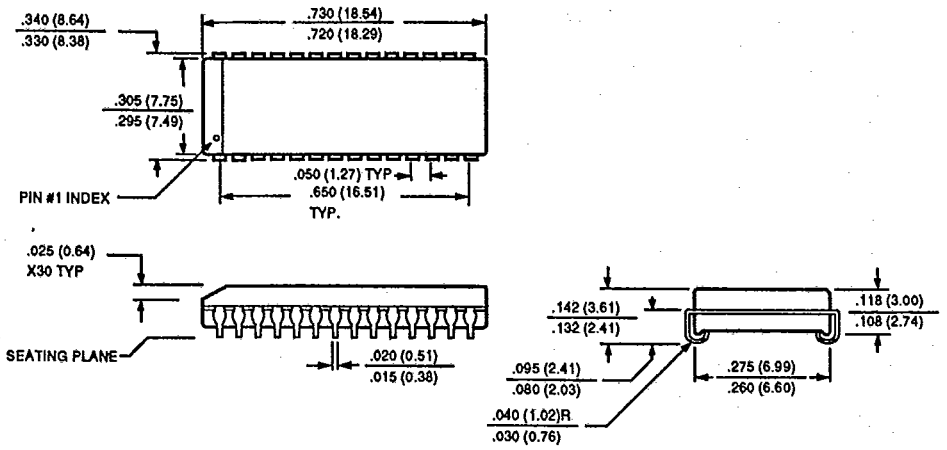
All dimensions in inches (millimeters) Max. / Min.

28 Pin Cerdip



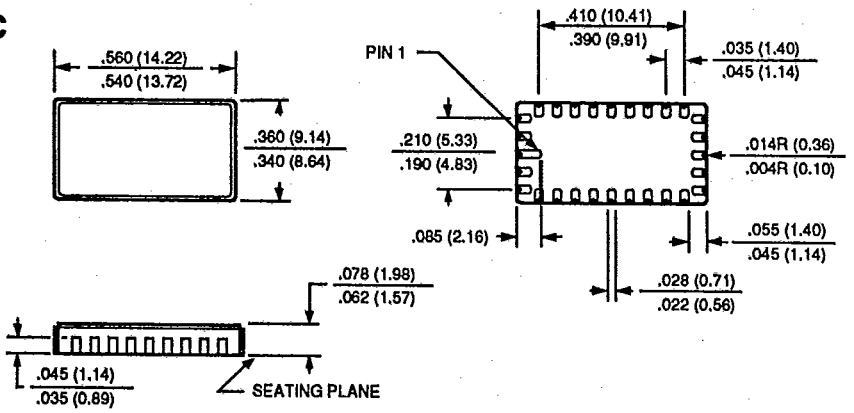
All dimensions in inches (millimeters) Max. / Min.

28 Pin Plastic SOJ



All dimensions in inches (millimeters) Max. / Min

28 Pin LCC



All dimensions in inches (unless noted). All dimensions in inches (millimeters.) Max./Min.

Ordering Information

PDM — Device Type — Power — Speed — Package — Process/Temperature Range

Process/Temperature Range	
Blank	Commercial (0° to +70°C)
M	Military (-55°C to +125°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD 883
Package	
P	300 mil Plastic Dip
D	300 mil Cerdip
L28	350 x 550 LCC
SO	300 mil Plastic SOJ
Speed	
15	Commercial Only
20	
25	
35	
45	
55	Military Only
Power	
S	Standard Power
L	Low Power
Device Type	
41251 41252	256K (64K x 4) Static RAM with separate I/O

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