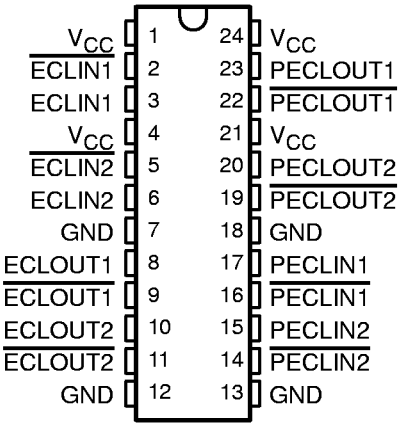
TNETA1545
DUAL DIFFERENTIAL PSEUDO-ECL TO ECL TRANSLATORS AND DUAL DIFFERENTIAL ECL TO PSEUDO-ECL TRANSLATORS

SDNS005B – SEPTEMBER 1993 – REVISED OCTOBER 1995

- **Dual ECL to Pseudo-ECL and Pseudo-ECL to ECL Translators**
- **Single 5-V Power Supply**
- **Advanced BiCMOS Technology**
- **Typical Application: Interface Between an ECL-Level Optical Transmitter and a Pseudo-ECL-Output Level Parallel-to-Serial Converter**
- **Packaged in 24-Pin Plastic Small-Outline Package**

DW PACKAGE
(TOP VIEW)

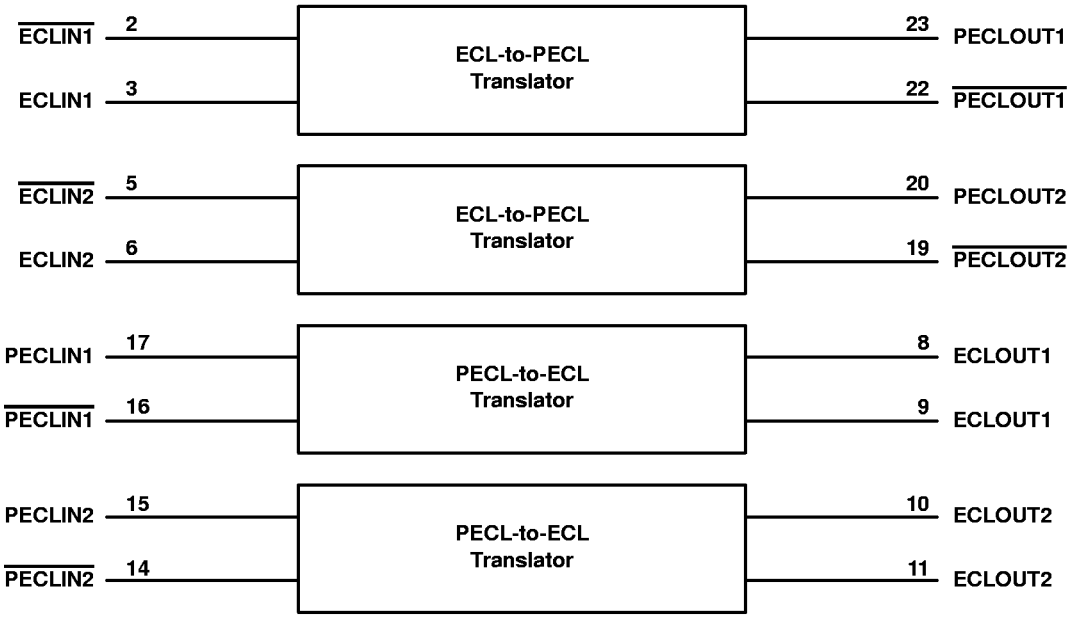


description

The TNETA1545 provides four buffers. Two buffers for two differential ECL-input signals referenced to GND are translated to differential psuedo-ECL (PECL) outputs referenced to 5 V instead of GND.

Two buffers for two differential PECL-input signals referenced to 5 V instead of GND are translated to differential ECL outputs referenced to GND.

functional block diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{ECLIN1}}$, ECLIN1	3, 2	I	ECL-compatible inputs for ECL-to-PECL translator
$\overline{\text{PECLOUT1}}$, PECLOUT1	23, 22	O	PECL-compatible outputs from ECL-to-PECL translator
$\overline{\text{ECLIN2}}$, ECLIN2	6, 5	I	ECL-compatible intpus for ECL-to-PECL translator
$\overline{\text{PECLOUT2}}$, PECLOUT2	20, 19	O	PECL-compatible otuputs from ECL-to-PECL translator
$\overline{\text{PECLIN1}}$, PECLIN1	17, 16	I	PECL-compatible inputs fro PECL-to-ECL translator
$\overline{\text{ECLOUT1}}$, ECLOUT1	8, 9	O	ECL-compatible outputs from PECL-to-ECL translator
$\overline{\text{PECLIN2}}$, PECLIN2	15, 14	I	PECL-compatible inputs for PECL-to-ECL translator
$\overline{\text{ECLOUT2}}$, ECLOUT2	10, 11	O	ECL-compatible outputs from PECL-to-ECL translator
GND	7,12,13,18		Ground (0-V reference)
V_{CC}	1,4,21,24		Supply voltage

absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range: ECL . . . . . −2.5 V to 0 V
PECL . . . . . 0 V to 7 V
Operating free-air temperature range, T_A . . . . . −40° C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	ECL (see Note 2)	−1.165		−0.88	V
		PECL (see Note 2)	V_{CC}−1.165		V_{CC}−0.88	
V_{IL}	Low-level input voltage	ECL (see Note 2)	−1.81		−1.475	V
		PECL (see Note 2)	V_{CC}−1.81		V_{CC}−1.475	
T_A	Operating free-air temperature		−40		85	°C

NOTE 2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	ECLOUT1, $\overline{\text{ECLOUT1}}$, ECLOUT2, $\overline{\text{ECLOUT2}}$	V_{CC} = 4.75 V, See Note 3	–1.025	–0.88	V
		PECLOUT1, $\overline{\text{PECLOUT1}}$, PECLOUT2, $\overline{\text{PECLOUT2}}$	V_{CC} = 4.75 V, See Note 4	V_{CC} –1.025	V_{CC} –0.84	
V_{OL}	Low-level output voltage	ECLOUT1, $\overline{\text{ECLOUT1}}$, ECLOUT2, $\overline{\text{ECLOUT2}}$	V_{CC} = 4.75 V, See Notes 2 and 3	–1.81	–1.62	V
		PECLOUT1, $\overline{\text{PECLOUT1}}$, PECLOUT2, $\overline{\text{PECLOUT2}}$	V_{CC} = 4.75 V, See Note 4	V_{CC} –1.85	V_{CC} –1.62	
I_{IH}	High-level input current	PECLIN1, $\overline{\text{PECLIN1}}$, PECLIN2, $\overline{\text{PECLIN2}}$	V_{CC} = 5.25 V, V_I = 4.45 V		50	µA
		ECLIN1, $\overline{\text{ECLIN1}}$, ECLIN2, $\overline{\text{ECLIN2}}$	V_{CC} = 5.25 V, V_I = –0.88 V		–1.5	mA
I_{IL}	Low-level input current	PECLIN1, $\overline{\text{PECLIN1}}$, PECLIN2, $\overline{\text{PECLIN2}}$	V_{CC} = 5.25 V, V_I = 3.35 V		50	µA
		ECLIN1, $\overline{\text{ECLIN1}}$, ECLIN2, $\overline{\text{ECLIN2}}$	V_{CC} = 5.25 V, V_I = –1.81 V		–2.5	mA
I_{CC}	Supply current		V_{CC} = 5.25 V, See Note 5		75	mA
			V_{CC} = 5.25 V, See Note 6		125	

NOTES: 2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.
3. These outputs are terminated through a 50-Ω resistor to –2 V.
4. These outputs are terminated with a 50-Ω resistor to V_{CC}–2 V.
5. All outputs open
6. ECLOUT1, $\overline{\text{ECLOUT1}}$, ECLOUT2, $\overline{\text{ECLOUT2}}$ terminated with a 50-Ω resistor to –2 V.
PECLOUT1, $\overline{\text{PECLOUT1}}$, PECLOUT2, $\overline{\text{PECLOUT2}}$ terminated with a 50-Ω resistor to V_{CC}–2 V.

switching charactertistics over recommended operating free-air temperature range, V_{CC} = 5 V ±0.25 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			250		MHz
t_{PLH}	ECLIN/$\overline{\text{ECLIN}}$ or PECLIN/$\overline{\text{PECLIN}}$	PECLOUT/$\overline{\text{PECLOUT}}$ or ECLOUT/$\overline{\text{ECLOUT}}$	1.5	4	ns
t_{PHL}	ECLIN/$\overline{\text{ECLIN}}$ or PECLIN/$\overline{\text{PECLIN}}$	PECLOUT/$\overline{\text{PECLOUT}}$ or ECLOUT/$\overline{\text{ECLOUT}}$	1.5	4	ns

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