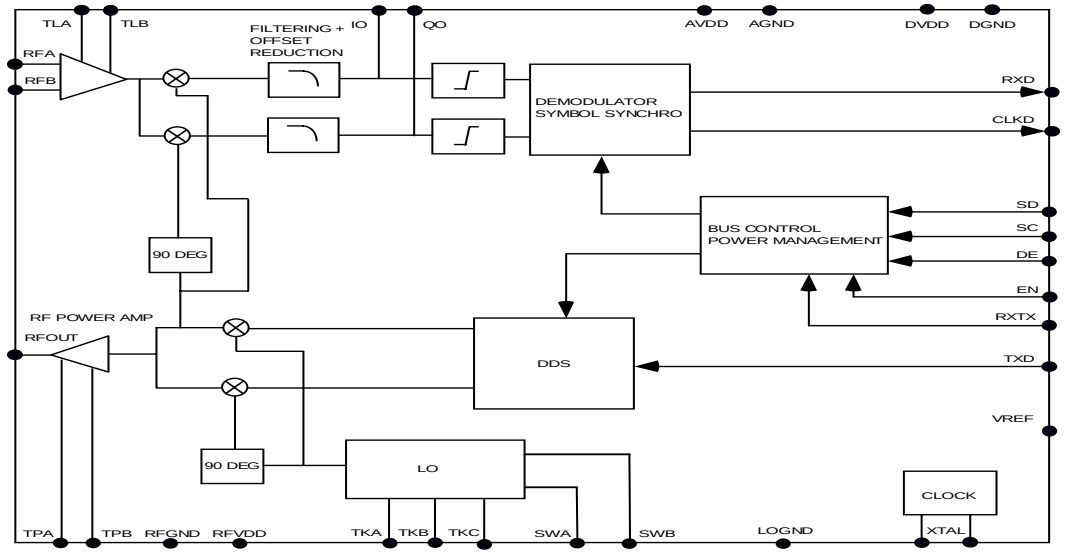


XE1201A 300-500 MHz

Low-Power UHF Transceiver

Features

- very low-power
- half-duplex operation
- data rate up to 64 kbit/s
- high sensitivity
- few external components
- internal bit synchronizer
- 3-wire bus for easy microcontroller interface
- output power programmable via bus

Applications

- telemetry
- RF security systems
- wireless data link
- door openers
- remote control
- wireless sensing

Ordering Information

Part	Temperature range	Pin-package
XE1201AI026TR	-40 to 70° C	TQFP32

General Description

The XE1201A is a half-duplex FSK transceiver for operation in the 433 MHz ISM band (optimized) and in the 300-500 MHz band. The modulation used is the Continuous Phase, 2 level Frequency Shift Keying (CPFSK). The direct conversion (zero IF) receiver architecture enables on-chip channel filtering.

The XE1201A includes a bit synchronizer so that glitch free data with synchronized clock can directly be read by a low cost / low complexity micro-controller. The transmitted power level can also be controlled via the bus. The XE1201A meets the I-ETS300-220 standard and is available in a TQFP32 package.

Quick Reference Data

- supply voltage 2.4 V
- RF sensitivity -109 dBm
- data rate 64 kbits/s
- transmitted power +5 dBm

1. DETAILED PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	EN	Chip enable
2	DE	Bus data enable
3	AVDD	Supply voltage for analog
4	TPA	Power amplifier tank circuit
5	TPB	Power amplifier tank circuit
6	AGND	Ground for analog
7	SC	Bus clock
8	SD	Bus data input
9	LOGND	Ground for local oscillator
10	TKA	Oscillator tank circuit
11	TKB	Oscillator tank circuit
12	TKC	Oscillator tank circuit
13	SWA	SAW resonator
14	SWB	SAW resonator
15	RXTX	Receiver / transmitter enable
16	VREF	Voltage stabilizer decoupling
17	TXD	Data input stream
18	CLKD	Received data clock
19	RXD	Received data output
20	DGND	Ground for digital
21	XTAL	Reference oscillator
22	XTAL	Reference oscillator
23	DVDD	Supply voltage for digital
24	QO	Test pin
25	IO	Test pin
26	RFA	RF input
27	RFB	RF input
28	RFGND	Ground for RF
29	RFOUT	Transmitter output
30	TLA	Low noise amplifier tank circuit
31	TLB	Low noise amplifier tank circuit
32	RFVDD	Supply voltage for RF

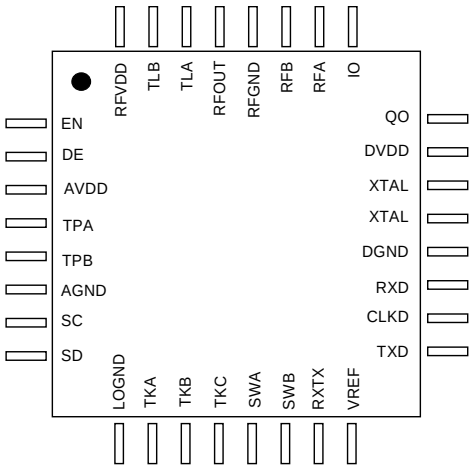


fig. 2: TQFP 32L package

2 ABSOLUTE RATINGS

- supply voltage 2.4 V to 6 V
- storage temperature -55°C to 150°C
- operating temperature -40°C to 70°C

3. ELECTRICAL CHARACTERISTICS

Tamb = 25° C; VDD = 3.0 V; F_{LO} = 433.92 MHz; +/- 125 kHz frequency deviation; 16 kbit/s pseudo random bit sequence unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	Min	Typ	Max	Units
VDD	Operating supply voltage		2.4	3.0	5.5	V
IDDR	Reception supply current		4.5	6	7.5	mA
IDDT	Transmission supply current	- 15 dBm output power		5.5		mA
		- 5 dBm output power		8		mA
		+ 2.5 dBm output power		11		mA
		+ 5 dBm output power		13.5		mA
IDDS	Standby current	Clock running	-	55	65	µA
		Clock stopped	-	0.2	1	µA
FR	Frequency range		300	-	500	MHz
TP	Transmitter output power	C13 = 0 ; C12 = 0		-15		dBm
		C13 = 0 ; C12 = 1		-5		dBm
		C13 = 1 ; C12 = 0		+2		dBm
		C13 = 1 ; C12 = 1		+5		dBm
RFS	RF sensitivity	BER=1%, R*source* = 50Ω				
		8 kbit/s	-106	-109	-	dBm
		16 kbit/s	-104	-107	-	dBm
		64 kbit/s	-99	-102	-	dBm
ZIN	RF input impedance	Parallel real part	-	1	-	kΩ

SYMBOL	PARAMETER	CONDITIONS	Min	Typ	Max	Units
		Parallel capacitive part	-	4	-	pF
ZOUT	RF output impedance	Parallel capacitive part	-	2.4	-	pF
CCR	Co-channel rejection	F*unw* =F*LO* ±125 kHz RF*level* = RFS+3dB	-12	-7	-	dB
BI	Blocking immunity	F*unw* =F*RF* ±1MHz RF*level* = RFS+3dB	39	43	-	dB
ML	Maximum receiver input level	1 channel, BER=1%	0	-	-	dBm
BW	Baseband filter bandwidth	3 dB cutoff frequency	250	330	410	kHz
LOD	Local oscillator drift	-40 < Tamb < +70° C	-	-4	-	ppm/° C
LOS	Local oscillator shift	2.4 V < Vdd < 3.6 V	-	+/-8	+/-15	KHz
TBW	DDS anti-alias filter bandwidth		-	160	-	kHz
FDEV	Frequency deviation	programmable by 3-wire bus	+/-4	-	+/-200	kHz
DR	Data rate	programmable by 3-wire bus	4	-	64	kbit/s
LOL	Digital input/output low level		0	-	0.4	V
HIL	Digital input/output high level		2.6	-	3	V
Tclk	Clock wake-up time	from cold start (see fig. 5)	-	2	3.5	ms
Rwu	Receiver wake-up time	from oscillator running (see fig. 4) bit synchronizer bypassed	-	60	75	µs
Twu	Transmitter wake-up time	from oscillator running (see fig. 4)	-	60	75	µs
Tsu	Data set-up time	(see fig. 3)	125	-	-	ns
Trt	Receive to transmit switching time	(see fig. 4)	-	15	25	µs
Ttr	Transmit to receive switching time	(see fig. 4) bit synchronizer bypassed	-	60	75	µs
Tr	SC bus clock rise time		-	-	50	ns
Tf	SC bus clock fall time		-	-	50	ns
FSC	SC bus clock frequency		-	-	4	MHz

4. HANDLING

All pins withstand the ESD test in accordance with the MIL-STD-883F method 3015.6 (all pins towards substrate), human body model (2000V). The RF output (pin 29) is only protected against negative voltage (no protection device towards VDD).

5. FUNCTIONAL DESCRIPTION

The XE1201A is controlled via the 3-wire serial bus by a microcontroller that addresses the 3 wires (SD - Serial Data, SC - Serial Clock, DE - Data enable) according to the format shown in Figure 3 a bit stream of 16 bits is fed into the internal register (SD - pin8) with the Most Significant Bit (MSB) first and is shifted during the low to high transition of the clock (SC - pin7). This serial programming is enabled by the Data Enable pin (DE - pin2) which must be set to zero before the data transfer. The low to high transition of the Data Enable validates the register filling. Data is retained as long as the supply voltage (Vdd) is present.

6. 3-WIRE BUS DATA FORMAT

The first two bits (D15 and D14) determine the A, B or C register access according to the truth table below (table 1).

D15	D14	REGISTER NAME
0	0	REGISTER A
0	1	REGISTER B
1	0	REGISTER C
1	1	NOT USED

table 1: Register Address

These three registers are filled by the data A13 to A0, B13 to B0 or C13 to C0 according to the value of D15 and D14. Register A is used to set the XE1201A mode (transmission, reception and standby modes) and to select the receiver data rate. Register B is used for central frequency adjustment during transmission. Register C is used for frequency deviation set-up, transmitted power adjustment and other auxiliary functions.

7. "A" REGISTER FORMAT (D15=0, D14=0)

D15	D14	A13	A12	A11	A10	A9	A8
A7	A6	A5	A4	A3	A2	A1	A0

table 2: "A" Register Format

∗ A13 - CONTROL MODE BIT

When set to 0, this bit enables the XE1201A transmit/receive mode and chip enable control to be addressed via the pin15 (RXTX) and pin1 (EN). For further information on this control mode, please refer to RXTX pin and EN pin description on page 7. When set to 1, the transmit/receive mode and chip enable controls are addressed by bit A10 and A11. In this mode, the levels applied on pin 15 and pin 1 have no effect.

∗ A12 - CLOCK CONTROL

This bit is used for XE1201A internal clock start-up. When set to 1, the clock is always running whatever the state of the chip enable bit (A11 when A13=1 or pin1 when A13=0). When set to 0, the clock activity is determined by the chip enable bit (A11).

∗ A11 - CHIP ENABLE

When set to 0, all the blocks of XE1201A are deactivated (except the clock if the bit A12 is set to 1). However, the 3-wire bus can be programmed in disabled mode as long as Vdd is present. This bit replaces the Chip Enable (pin1) when A13=1.

* A10 - TRANSMIT/RECEIVE MODE

When set to 1, the XE1201A is set in receiving mode and in transmitting mode when set to 0. This bit replaces the RXTX (pin15) when A13=1

* A9, A8, A7, A6 – DEMODULATOR AND BIT SYNCHRONIZER BYPASSING

These bits are used in applications where the bit synchronizer is not needed for e.g. decrease the receiver wake-up time

a) The receiver is in normal mode but the demodulator is bypassed. The outputs I and Q of the limiters are available on pin19
(I output) and pin 18 (Q output). Bits A9 to A6 must be set according to table 3 below.

A9	A8	A7	A6
0	1	0	0

table 3: Receiver Mode with Demodulator Bypassed

b) The receiver is in normal mode but the internal bit synchronizer is switched off. Raw data are available at RXD output (pin19). The CLKD (pin18) is meaningless. In this mode, no preamble is required for clock synchronization of the bit synchronizer so that the minimum receiver wake-up time is accessed. Bits A9 to A6 must be set according to table 4.

A9	A8	A7	A6
0	1	0	1

table 4: Receiver Mode with Bit Synchronizer Switched Off

* A5, A4, A3, A2, A1, A0 - RECEIVER DATA RATE

These bits are used to set the bit synchronizer data rate according to the following formula:

$$DR = 65574 \bullet 2^{\left(\frac{-n}{8}\right)} \quad [Hz]$$

Where n is the unsigned decimal value of bits A5 to A0 (A5=MSB).
The inverse function gives the value of n for a wanted data rate DR (in Hz) as showed below:

$$n = ROUND\left(\frac{-8 \bullet \mathrm{Log}\left[\frac{61 \bullet DR}{4 \bullet 10^{6}}\right]}{\mathrm{Log}\ 2}\right)$$

The rate of the data to be transmitted should then be fed accordingly in TXD (pin17).

Note: when the bit synchronizer is bypassed (bits A9,A8,A7,A6), it is not necessary to program the data rate. The data are demodulated accordingly to the incoming data rate.

8. "B" REGISTER FORMAT (D15=0, D14=1)

D15	D14	B13	B12	B11	B10	B9	B8
B7	B6	B5	B4	B3	B2	B1	B0

table 5: "B" register format

* B13, B12, B11, B10, B9, B8, B7 - OFFSET FREQUENCY

These bits can be used to calibrate the oscillator central frequency (e.g. related to SAW resonator initial accuracy). A frequency offset can be added or subtracted to the frequency of the Local Oscillator while transmitting according to the following formula:

$DFC = 3906.25 \bullet n \ [Hz]$

where n is the signed value of bits B13 to B7 (from -64 to +63). Bits B13 to B7 are expressed in 2's complement 7 bits representation. The offset can thus range from
-250000 Hz (1000000) to 246093.75 Hz (0111111).

* B6, B5, B4, B3, B2, B1, B0 – TEST BITS

These bits are for test purpose only. They must be set to zero.

9. "C" REGISTER FORMAT (D15=1, D14=0)

D15	D14	C13	C12	C11	C10	C9	C8
C7	C6	C5	C4	C3	C2	C1	C0

table 6: "C" register format

* C13, C12 - TRANSMITTED OUTPUT POWER

The output power available at RFOUT (pin29) can be adjusted with C13 and C12 according to table 7 below.

C13	C12	OUTPUT POWER
0	0	- 15 dBm
0	1	- 5 dBm
1	0	+ 2.5 dBm
1	1	+ 5 dBm

table 7: transmitter output power control bits

* C11 - DATA INVERSION BIT

The received data stream is inverted when this bit is set to 1.

* C10, C9 - TEST BITS

These bits must always be set to C10=1 and C9=0

* C8 - TRANSMITTED OUTPUT AMPLIFIER ENABLE

When set to 0, this bit disables the transmitter output amplifier whatever the transceiver state is.

* C7 - TRANSMITTED DATA BIT

This bit replaces the TXD (pin17) when bit A13 of register A is set to 1 and thus allows a data transmission via the 3-wire bus.

* C6, C5, C4, C3, C2, C1, C0 - MODULATOR FREQUENCY DEVIATION

These bits are used to adjust the frequency deviation of the modulator according to the following formula:

$FDEV = 3906.25 \bullet n \ [Hz]$

Where n is the unsigned decimal value of bits C6 to C0. The frequency deviation of the transmitter can be theoretically adjusted up to 496093.75 Hz. However, it should be noticed that for proper behavior of the XE1201A demodulator, the frequency deviation must be greater than the data rate (FDEV>DR) and smaller than the baseband filter bandwidth (BW). In addition, the FDEV must be smaller than the DDS anti-alias filter bandwidth (TBW).

10. BUS REGISTERS DEFAULT VALUES

After Vdd is applied, the internal 3-wire bus registers A, B and C are initialized with the values shown in tables 8, 9 and 10 below.

A13	A12	A11	A10	A9	A8	A7
0	0	0	0	0	0	0

A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	0

table 8: register "A" default value

B13	B12	B11	B10	B9	B8	B7
0	0	0	0	0	0	0

B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0

table 9: register "B" default value

C13	C12	C11	C10	C9	C8	C7
0	1	0	1	0	1	0

C6	C5	C4	C3	C2	C1	C0
0	1	0	0	0	0	0

table 10: register "C" default value

After power-up, the XE1201A is in the following initial state: RXTX (pin15) and EN (pin1) control mode, clock stopped, 16 kbits/s data rate, -5 dBm output power and 125 kHz frequency deviation. Ready to transmit or receive.

11. RXTX (PIN15) AND EN (PIN1)

RXTX (receive/transmit) and EN (chip enable) are activated when the control bit (A13) is set to zero. In this mode, the XE1201A can be switched on, switched off and set to the transmit or receive mode with pin 1 (EN) and 15 (RXTX) as explained in table 11 and figure 4.

EN	RXTX	MODE
0	X	CHIP DISABLED
1	0	TRANSMIT MODE
1	1	RECEIVE MODE

table 11: EN and RXTX pins truth table

12. BIT SYNCHRONIZATION IN RECEIVING MODE

The operation is based on an advanced digital PLL controlled by an ALU. Care must be taken while using it, particularly when the receiver is in permanent listening mode (please refer to the XE1201A application information documentation).

The internal demodulator of the XE1201A needs a frame of 20 synchronization bits to ensure proper clock synchronization. The synchronization frame must be a sequence of 0 and 1 sent alternatively.

13. WAKE-UP TIME

The wake-up time depends on the clock state. If the clock is kept running (A12=1), the wake-up time is 75 µs max. If the clock is off, the clock has to be switched on before the wake-up of the rest of the XE1201A as explained in figure 5.

14. TIMING FIGURES

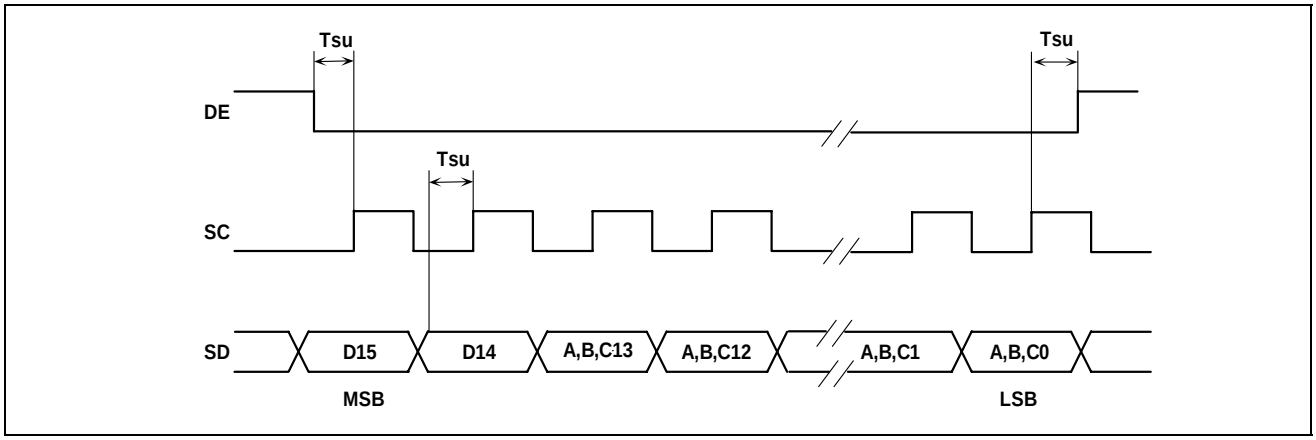


Figure 3: timing diagram for 3-wire bus

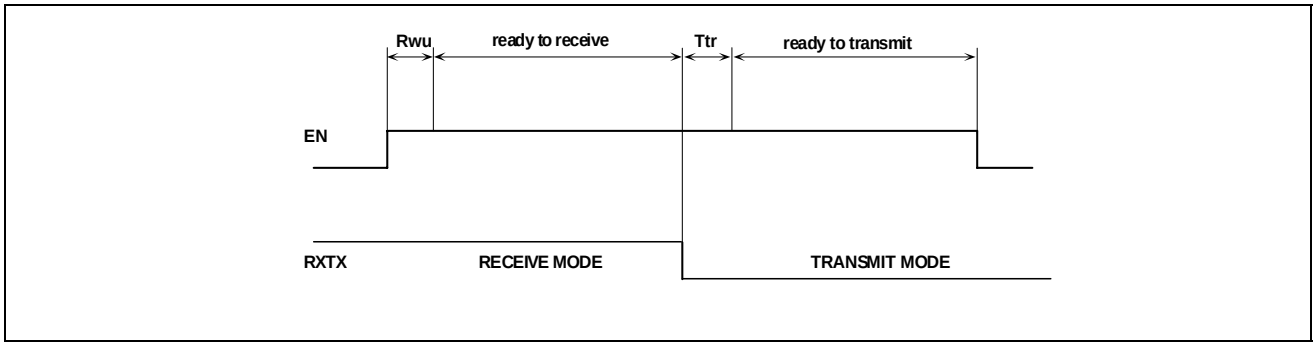


Figure 4: timing diagram for RXTX and EN control pins

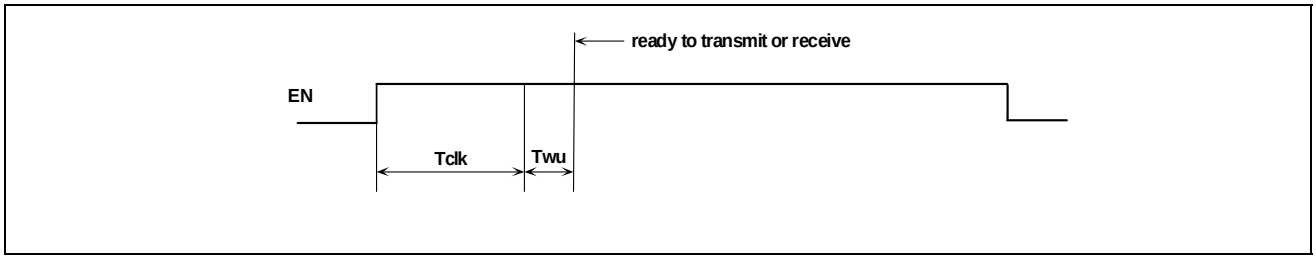


Figure 5: timing diagram for chip wake-up (from cold start)

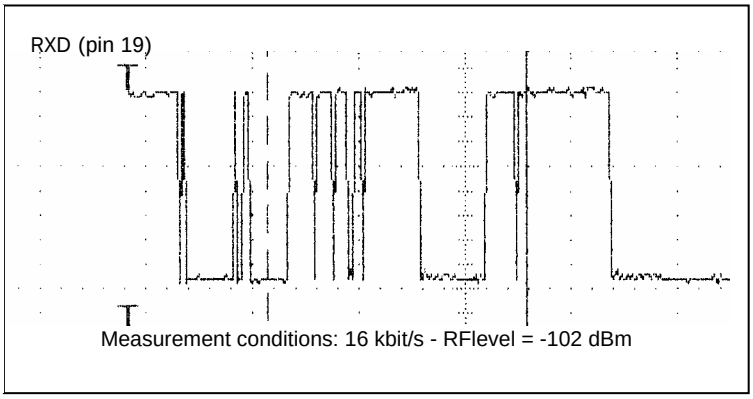


Figure 6: Received data stream with internal bit synchronizer bypassed

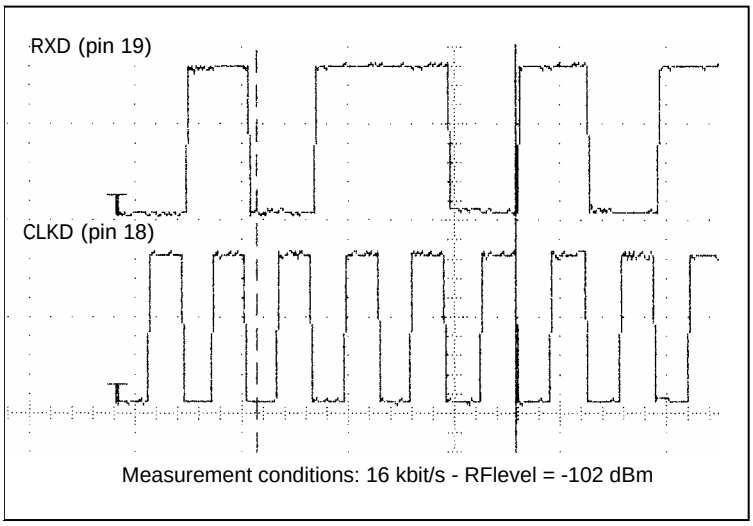
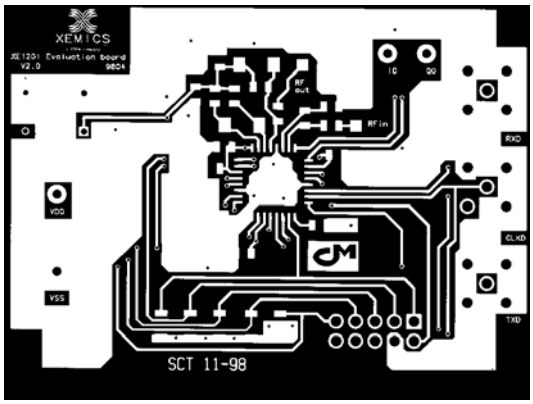
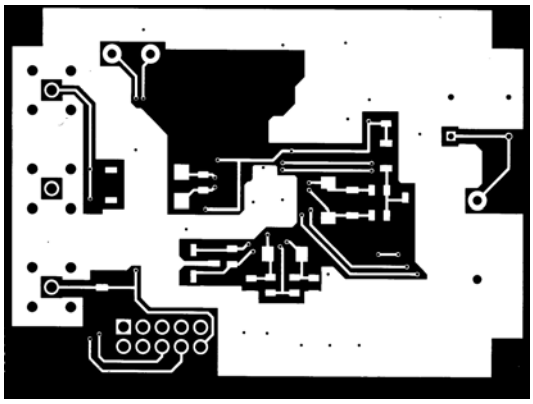


Figure 7: Received data stream with internal bit synchronizer and synchronized data clock output



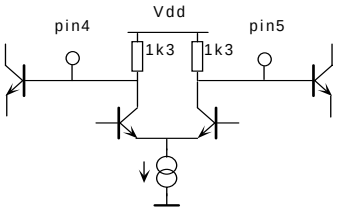
components side (front)



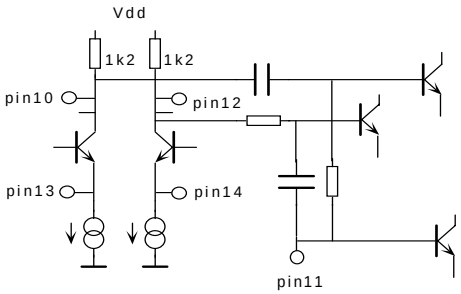
copper side (back)

Figure 8: reference board layout (not actual scale)

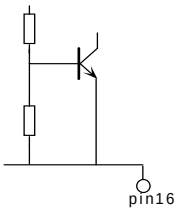
15. ANALOG PIN DESCRIPTION



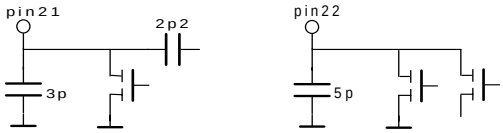
pin4 and 5: power amplifier



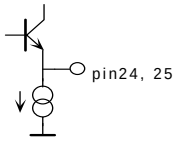
pin10, 11, 12, 13 and 14: oscillator



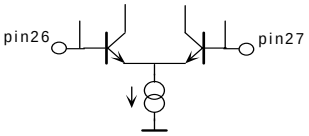
pin16: voltage stabilizer



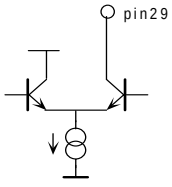
pin21 and 22: clock oscillator



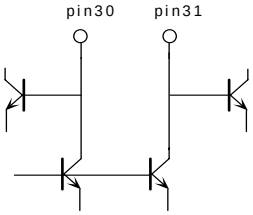
pin24 and 25: I and Q outputs



pin26 and 27: RF amplifier inputs



pin29: transmitter output



pin30 and 31: LNA tank

Figure 9: analog pins description

16. APPLICATION INFORMATION

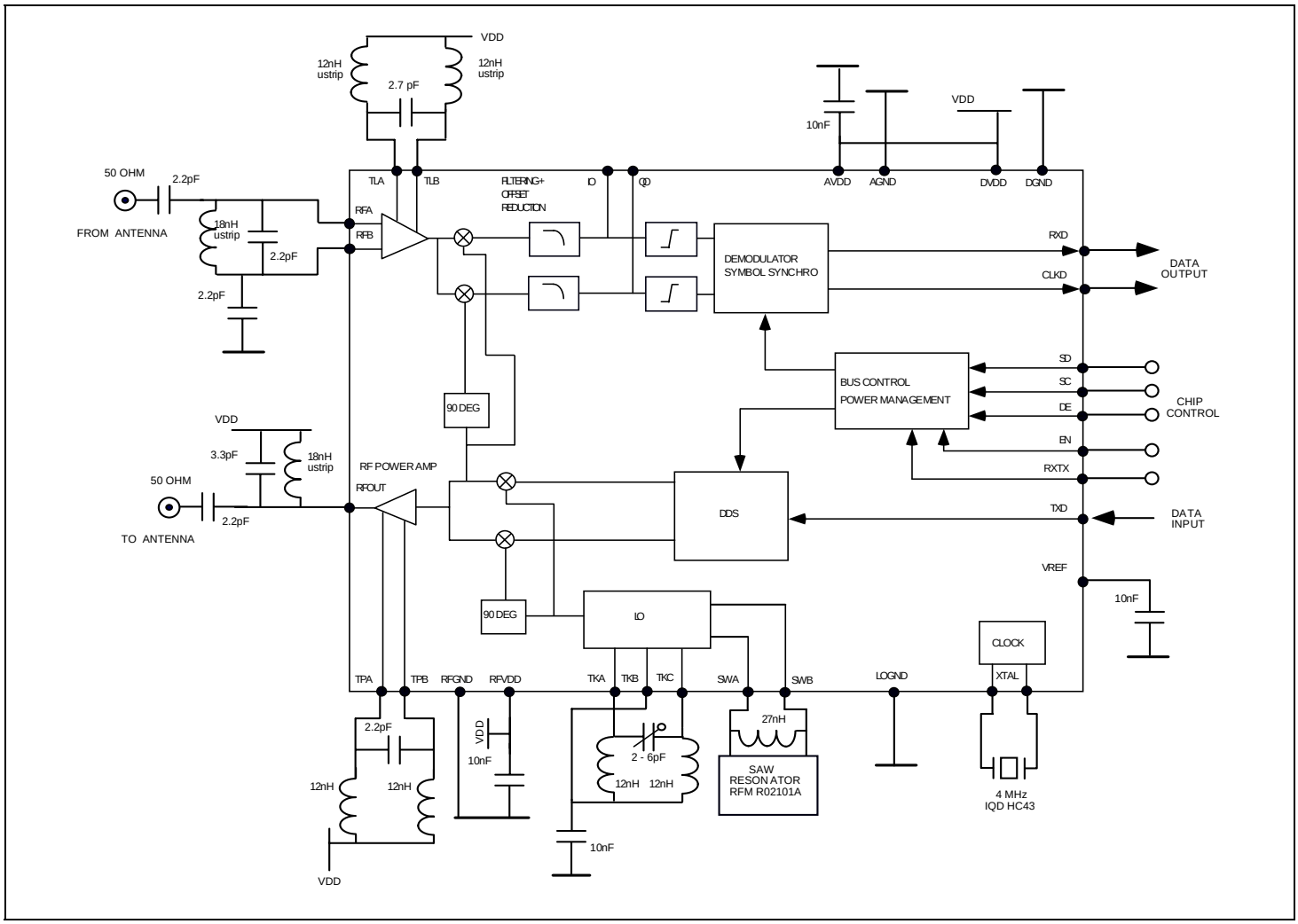
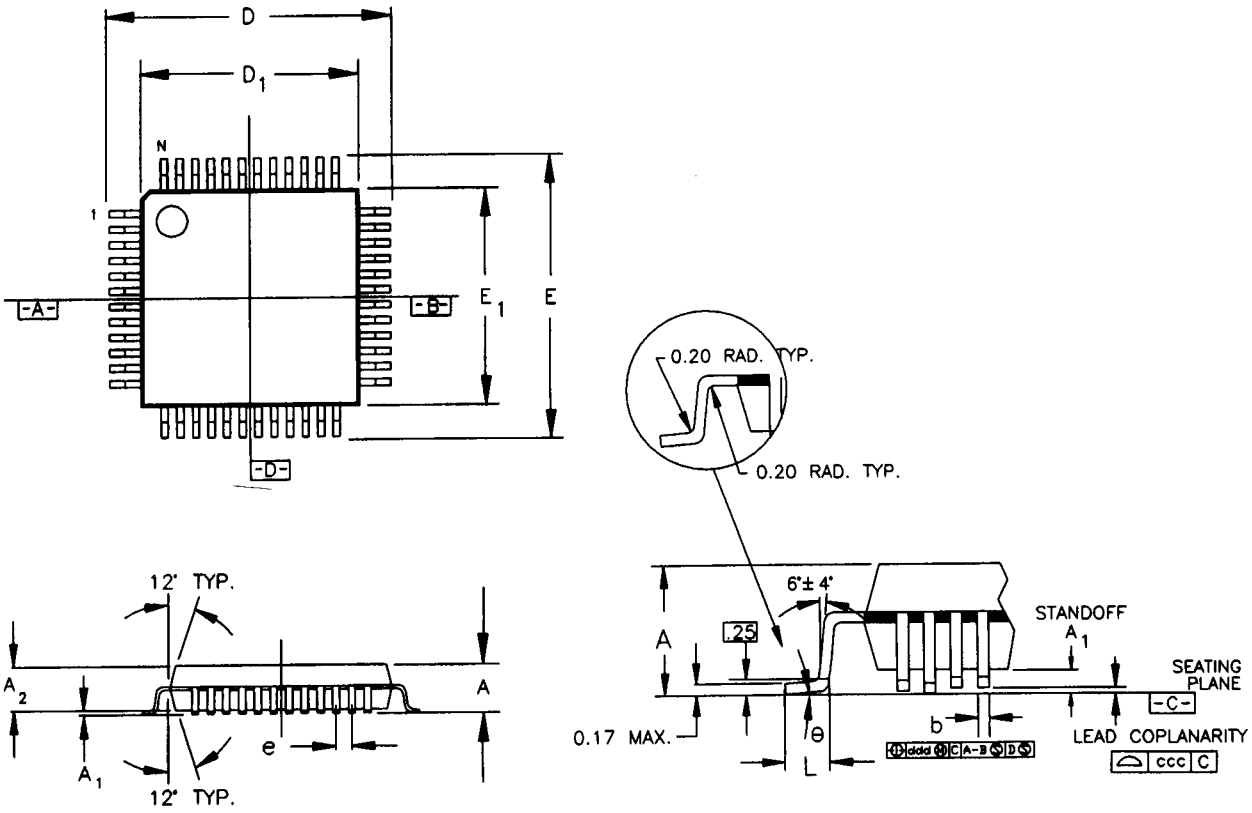


Figure 10: application information

17. MECHANICAL DATA PACKAGE



DIMENSIONS	VALUE	TOLERANCE
Body Thickness	1.00	-
Footprint (Body+)	2.00	-
A	1.20	MAX
A1	0.05 min/0.15 max	-
A2	1.00	±0.05
D	9.00	±0.25
D1	7.00	±0.10
E	9.00	±0.25
E1	7.00	±0.10
L	0.60	+0.15/-0.10
e	0.80	BASIC
b	0.35	±0.05
ccc	0.10	MAX
ddd	0.20	MAX
0	0°-7°	

Package Information for TQFP 32L

Contact Information

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