MICRONAS

DA9316.000

MAS9316

16–BIT DAC, BUFFERED

- ± 0.006% DNL and INL
- No Laser Trimming
- Fast Interface Timing

DESCRIPTION

The MAS9316 is a 16–bit, monolithic CMOS, multiplying digital–to–analog converter (DAC) designed for direct microprocessor interface. Its high relative accuracy and monotonicity is achieved without laser trimming. This is made possible by the use of highly accurate, low TCR thin film resistor process and a 4 MSB to 15 decoding design technique. Hidden errors are eliminated by testing all the 65536 different input codes.

The device offers advantages like high stability over time and temperature and low sensitivity to output amplifier offset combined to excellent performance–to–cost ratio. The fast input data latches are designed as two 8–bit segments providing data storage when latched or transparent operation when unlatched. All digital inputs have high ESD protection up to 2 kV.

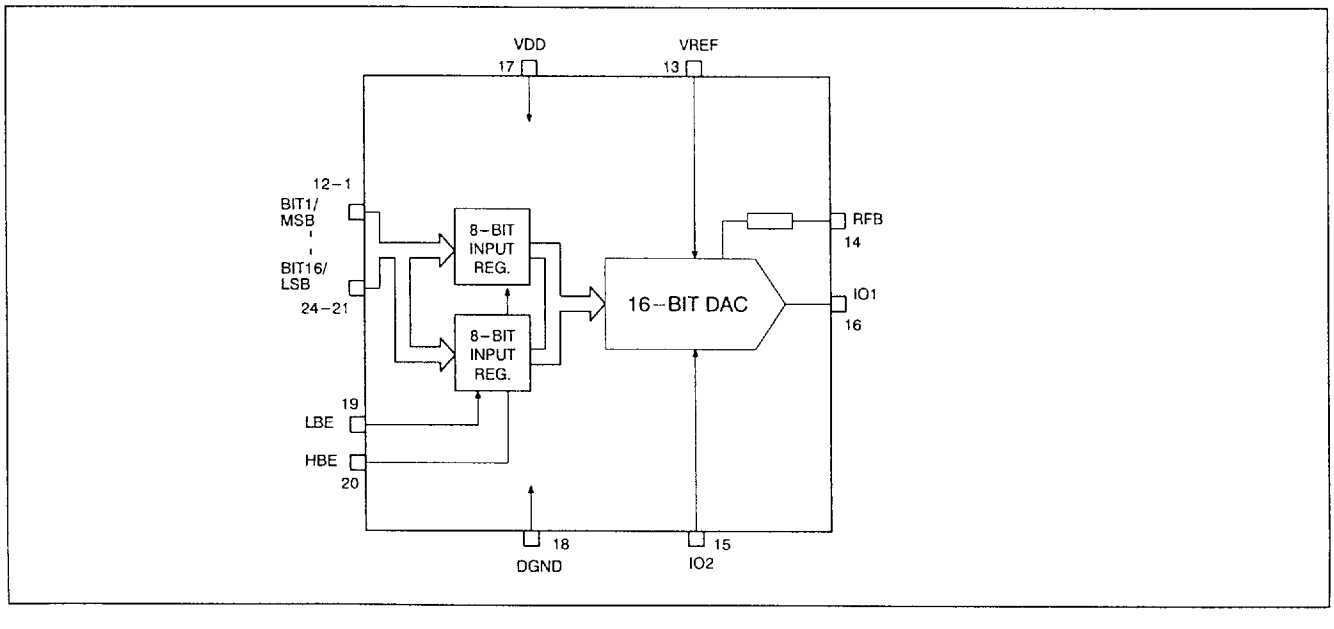
FEATURES

- ± 0.006% DNL and INL
- No Laser Trimming
- Fast Interface Timing
- Linearity TC 0.5 ppm/°C
- 2 kV ESD Protection on Digital Inputs
- 4 MSB's Decoded
- All 65536 Codes Tested
- Monolithic CMOS Replacement for SIPEX DAC 9331–16–4 and SP9316C–4
- 24–pin Cerdip Package

APPLICATION

- Audio Applications
- Instrumentation
- µP Controlled Systems

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

VDD=+15V, VREF=10V, IO1=IO2=DGND=0V, Unipolar unless otherwise specified.

		Ta=+25°C			Tmin–Tmax		
Parameter	Symbol	MIN	TYP	MAX	Limits	Units	Test Conditions/Comments
STATIC PERFORMANCE							
Resolution	N	16			16	Bits	
Integral Nonlinearity[1]	INL		±0.004	±0.006	±0.012	%	Relative accuracy 13 bits
Differential Nonlinearity[2]	DNL		±0.003	±0.006	±0.006	%	Monotonic to 14 bits
Gain error	Gfse		±0.1	±0.2		%	Measured Using Internal Rfb DAC Register Loaded With All 1's
Output Leakage Current at IO1 (pin 16)	Ilkg			10	50	nA	
Offset Error				±0.0005	±0.0025	%	
TEMPERATURE STABILITY							
Gain error TC	TCGFSE		±1.0	±2.0		ppm/°C	
Integral Nonlinearity TC	TCINL		±0.1	±0.5		ppm/°C	
Differential Nonlinearity TC	TCDNL		±0.1	±0.5		ppm/°C	
REFERENCE INPUT							
Input Resistance	Rref	2.5	5	7.5		kΩ	
Voltage Range[3]					±25	V	
DIGITAL INPUTS							Unipolar Coding. Binary
Input High Voltage	VIH	2.4		VDD	2.4	V	Bipolar Coding. Offset Binary
Input Low Voltage	VIL	−0.3		0.8	0.8	V	
Input Current[4]	Iin			±1	±10	µA	
Input Capacitance[3]	Cin			8	8	pF	
SWITCHING CHARACTERISTICS							
Strobe Width	t_{SW}	80	60			ns	HBE and LBE Inputs
Data Setup Time	t_{DS}	80	70			ns	Bit 1 to Bit 16
Data Hold Time	t_{DH}	40	20			ns	Bit 1 to Bit 16
POWER SUPPLY							
Voltage Range	VDD	+5	+15	+16		V	Accuracy guaranteed only at +15V
Supply Current	IDD		2.0	4.0	4.0	mA	All Digital Inputs VIL or VIH
	IDD		0.2	1.0	1.0	mA	All Digital Inputs 0V or 5V
Power Dissipation				60		mW	
TEMPERATURE RANGE		0		+70		°C	

NOTES:
1. Integral Nonlinearity is measured as the arithmetic mean value of magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value of any given input combination.
2. Differential Nonlinearity DNL is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
3. Guaranteed by design but not production tested.
4. Logic inputs are MOS gates. Iin typical is less than 1 nA at 25°C.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are subject to sample testing only. VDD=+15V, VREF=10V, IO1=IO2=DGND=0V except where stated. Output Amp is HOS−050.

		Ta=+25°C			Tmin−Tmax		
Parameter	Symbol	Min	TYP	MAX	Limits	Units	Test Conditions/Comments
PROPAGATION DELAY	t_{PD}		300			ns	IO1 load R=100Ω, Cext=13pF All Data Inputs 0V to VDD or VDD to 0V From 50% digital input change to 90% of final analog output.
CURRENT SETTLING TIME Major Code Transition	ts		1.5			us	Settling to +0.01% FSR (strobed). 0111111111111111 to 1000000000000000 or 1000000000000000 to 0111111111111111
Full Scale Transition			3.0			us	All Data Inputs 0V to VDD or VDD to 0V
OUTPUT CAPACITANCE	Co						
CIO1 (Pin 16)			170			pF	Digital inputs VIH
CIO2 (Pin 15)			30			pF	Digital inputs VIH
CIO1 (Pin 16)			80			pF	Digital inputs VIL
CIO2 (Pin 15)			100			pF	Digital inputs VIL
DIGITAL TO ANALOG GLITCH ENERGY	Q		250			nVs	VREF = 0V; DAC register alternately loaded with all 0's and all 1's
MULTIPLYING FEEDTHROUGH ERROR AT IO1	FT		3.0			mVpp	VREF= 20Vpp; f=10kHz sine wave
			0.3			mVpp	VREF=20Vpp, f=1kHz sine wave
POWER SUPPLY REJECTION RATIO	PSRR		±0.0001	±0.002		%/%	VDD = 14 to16V

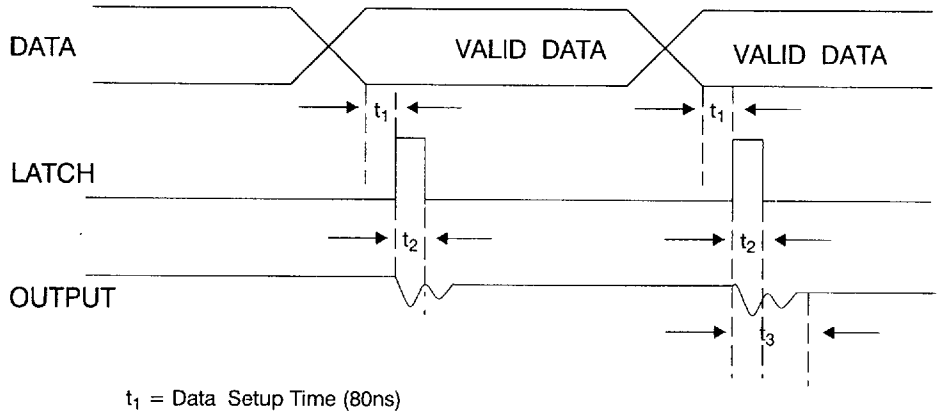
ABSOLUTE MAXIMUM RATINGS

(TA=25°C unless otherwise noted)

VDD to DGND ..... −0.3V, +17V
Digital Input Voltage to DGND ..... −0.3V, VDD +0.3V
VREF or RFB to DGND ..... +/−25V
Output Voltage (Pin 15, Pin 16) ..... −0.3V, VDD+0.3V
Power Dissipation (Any Package) to +75°C ..... 450 mW
Derates above 75°C by ..... 6 mW/°C
Dice Junction Temperature ..... +150°C
Storage Temperature ..... −65°C to +150°C

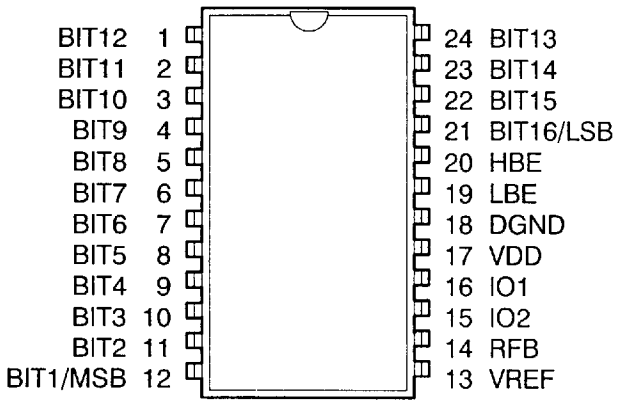
CAUTION:
1. Do not apply voltages higher than VDD or less than GND potential on any terminal other than VREF or RFB.
2. The digital inputs are diode clamp protected against ESD damage. However, permanent damage may occur on unprotected units from high−energy electrostatic fields. Keep units in conductive foam at all time until ready to use.
3. Use proper anti−static handling procedures.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied.

TIMING DIAGRAM



t_1 = Data Setup Time (80ns)
t_2 = Strobe Width (80ns)
t_3 = Settling Time (2µs typical)

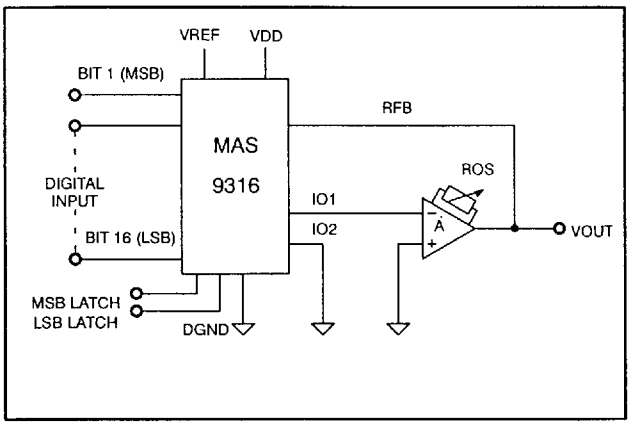
PIN CONFIGURATION

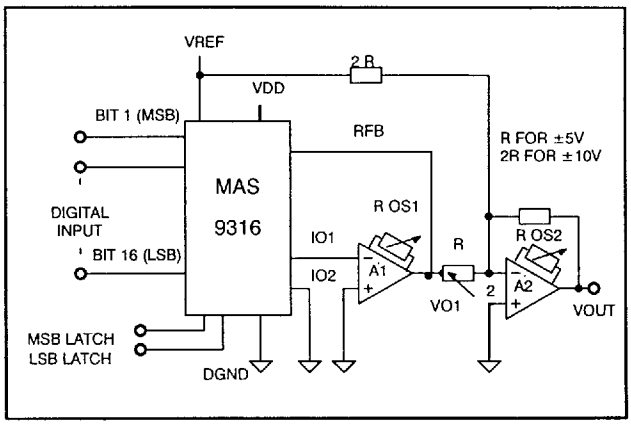


PIN DESCRIPTION

Pin name	Pin No.	I/O	Function
BIT12	1	I	Data BIT12, MSB
BIT11	2	I	Data BIT11
BIT10	3	I	Data BIT10
BIT9	4	I	Data BIT9
BIT8	5	I	Data BIT8
BIT7	6	I	Data BIT7
BIT6	7	I	Data BIT6
BIT5	8	I	Data BIT5
BIT4	9	I	Data BIT4
BIT3	10	I	Data BIT3
BIT2	11	I	Data BIT2
BIT1	12	I	Data BIT1
VREF	13	I	Reference Voltage Input
RFB	14	I	Feedback Resistor
IO2	15	O	Current Output
IO1	16	O	Current Output
VDD	17	P	Positive Power Supply
DGND	18	G	Digital Ground
LBE	19	I	Low Byte Enable
HBE	20	I	High Byte Enable
BIT16	21	I	Data BIT16, LSB
BIT15	22	I	Data BIT15
BIT14	23	I	Data BIT14
BIT13	24	I	Data BIT13

APPLICATION INFORMATION





UNIPOLAR OPERATION, Transfer Characteristics

BINARY INPUT	ANALOG OUTPUT
111 ... 111	$-VREF\ (1-2^{-N})$
100 ... 001	$-VREF(1/2+2^{-N})$
100 ... 000	$-VREF\ /2$
011 ... 111	$-VREF\ (1/2-2^{-N})$
000 ... 001	$-VREF\ (2^{-N})$
000 ... 000	0

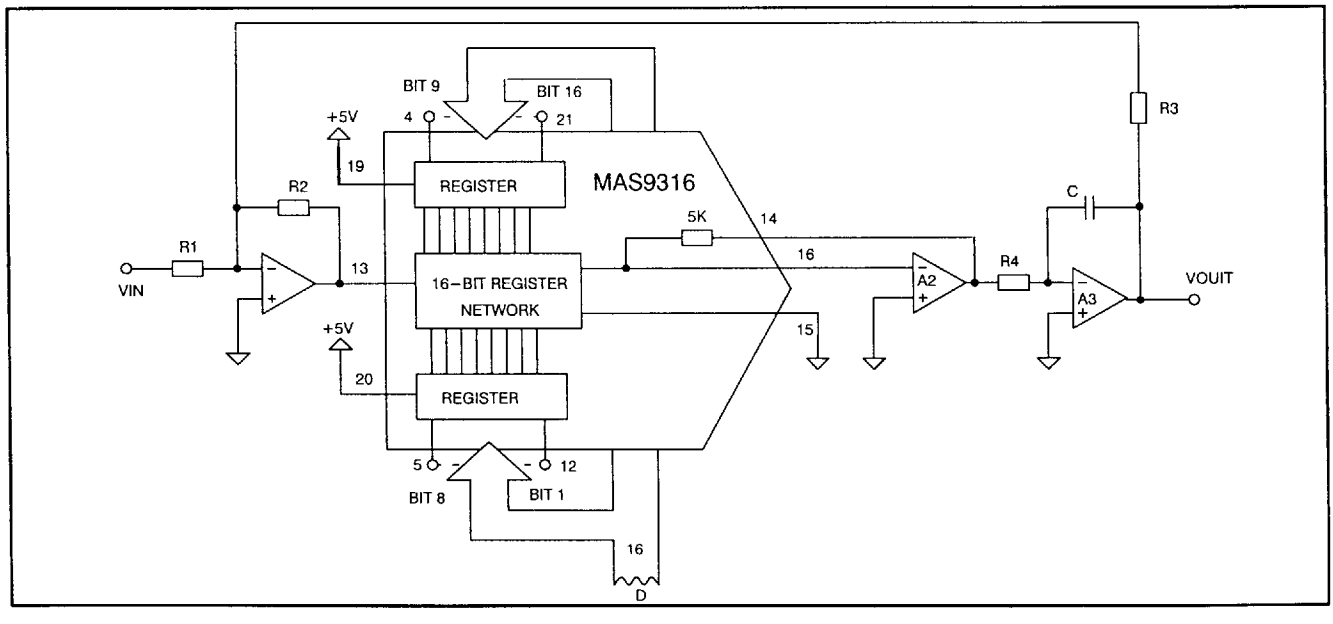
NOTE: To maintain specified linearity, the external amplifier (A) must be nulled. Apply on "all Zeroes" digital input and adjust ROS for VOUT = 0±1mV.

BIPOLAR OPERATION, Transfer Characteristics

OFFSET BINARY INPUT	ANALOG OUTPUT
111 ... 111	$-VREF\ (1-2^{-(N-1)})$
100 ... 001	$-VREF(2^{-(N-1)})$
100 ... 000	0
011 ... 111	$+VREF\ (2^{(N-1)})$
000 ... 001	$+VREF\ (1-2^{(-N-1)})$
000 ... 000	+VREF

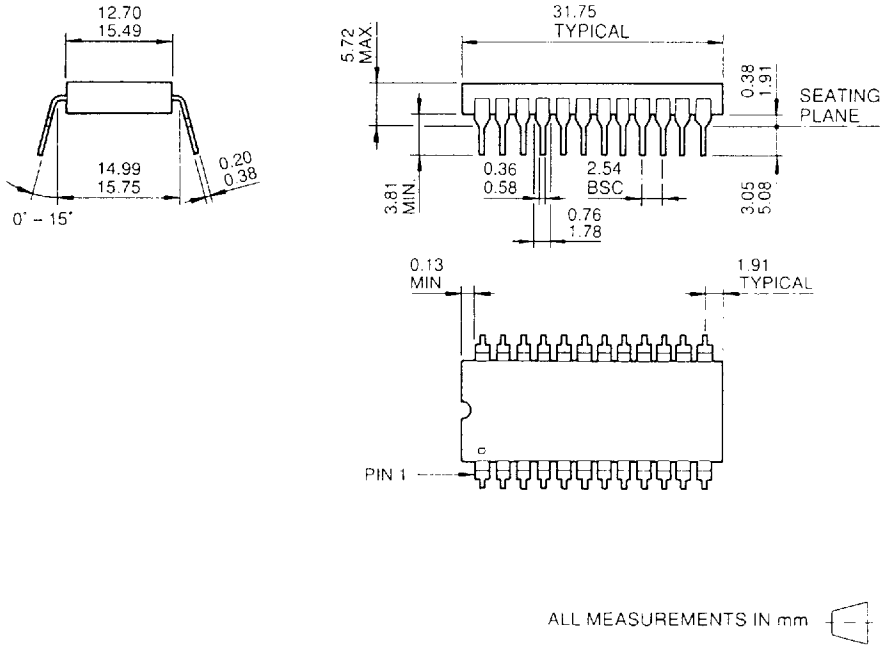
NOTE: To maintain specified linearity, the external amplifier (A_1 and A_2) must be nulled.
With a digital input of 10 ... 0 and VREF set to zero:
a) Set ROS1 for VO1 = 0
b) Set ROS2 for VOUT = 0
c) Set VREF to +10V and adjust R_B for VOUT to be 0 volts.

DIGITALLY CONTROLLED LOW PASS FILTER



PACKAGE OUTLINES

24 LEAD CERDIP OUTLINE (600 MIL BODY)



ALL MEASUREMENTS IN mm

ORDERING INFORMATION

Product code	Product	Package	Comments
MAS9316Q	16–BIT DAC, BUFFERED	24 Pin CERDIP	

LOCAL DISTRIBUTOR

MICRONAS CONTACTS

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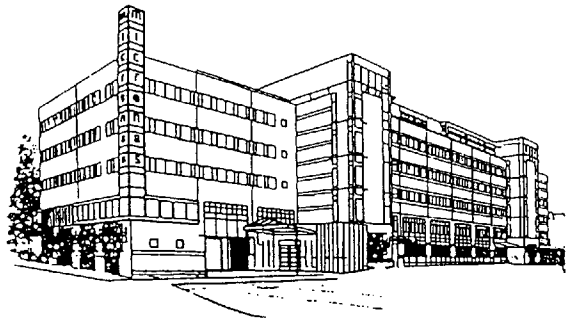

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