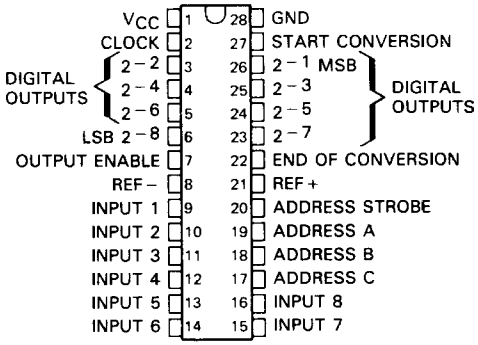
TYPES TL520, TL521, TL522 CMOS ANALOG-TO-DIGITAL CONVERTERS WITH 8-CHANNEL MULTIPLEXERS

D2666, SEPTEMBER 1982—REVISED SEPTEMBER 1983

- **Total Unadjusted Error at 85°C:**
  TL520 . . . ±3/4 LSB MAX
  TL521 . . . ±1 LSB MAX
  TL522 . . . ±1/2 LSB MAX
- **8-Bit Resolution**
- **Built-in 8-Input Analog Multiplexer**
- **Minimum Conversion Time:**
  TL520 . . . 70 μs
  TL521 . . . 100 μs
  TL522 . . . 200 μs
- **Ratiometric Conversion**
- **Guaranteed Monotonicity**
- **No Missing Codes**
- **Easy Interface with Microprocessors**
- **Latched 3-State Outputs**
- **Latched Address Inputs**
- **Single-Supply Operation**
  TL520, TL521 . . . 5 V
  TL522 . . . 3 V
- **Low Power Consumption**
  TL520, TL521 . . . 2.5 mW Typical
  TL522 . . . 0.3 mW Typical

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL520, TL521, and TL522 are monolithic CMOS devices each with an 8-channel multiplexer, and 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to a comparator. The 8-bit A/D converter uses a binary-weighted capacitor array to implement the high-speed, successive-approximation conversion technique.

The comparison and conversion methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs and latched inputs to the multiplexer address decoder. The single 5-volt supply and low power requirements make the TL520 and TL521 especially useful for a wide variety of applications. The 3-volt and low power requirements make the TL522 especially useful for battery and LCD applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

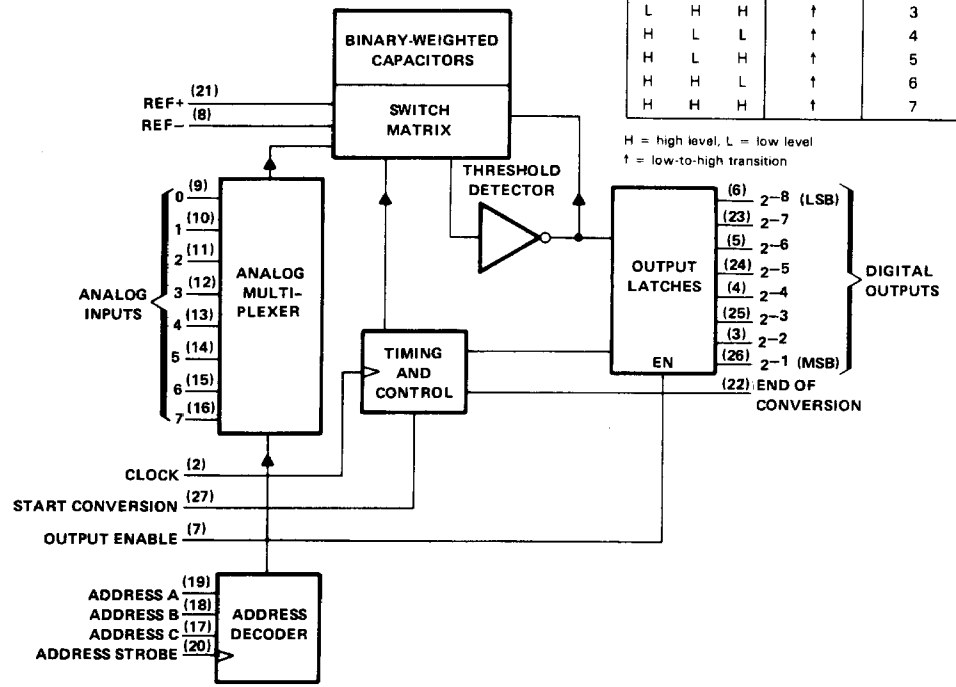
The TL520, TL521, and TL522 are characterized for operation from −40°C to 85°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Positive reference input voltage range, V_{REF+} . . . . . V_{REF-} to V_{CC} + 0.3 V
Negative reference input voltage range, V_{REF-} (see Note 1) . . . . . −0.3 V to V_{REF+}
Input voltage range: all other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Continuous total dissipation at 25°C free-air temperature (see Note 2) . . . . . 1250 mW
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

functional block diagram (positive logic)

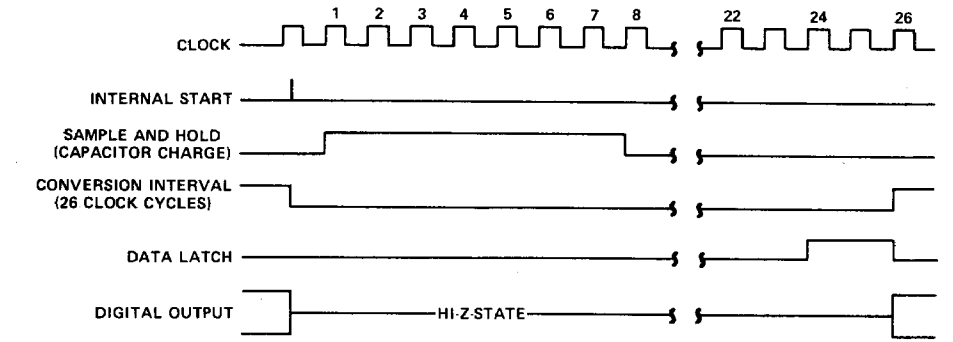


MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition

internal timing sequence



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TL520, TL521 recommended operating conditions

		TL520			TL521			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		3	5	5.5	3	5	5.5	V
Positive reference voltage, V_{REF+}		3		V_{CC}	3		V_{CC}	V
Negative reference voltage, V_{REF-}		0		0.3	0		0.3	V
Supply voltage relative to V_{REF+} ($V_{CC} - V_{REF+}$)		0		1	0		1	V
Analog input voltage (see Note 3)		V_{REF-}		V_{REF+}	V_{REF-}		V_{REF+}	V
High-level control input voltage, V_{IH}	$V_{CC} \geq 4.75$ V	$V_{CC} - 1.5$			$V_{CC} - 1.5$			
Low-level control input voltage, V_{IL}	$V_{CC} \geq 4.75$ V			1.5			1.5	V
Clock frequency, f_{clock}	$V_{REF+} = 5$ V		260	370		200	260	kHz
	$V_{REF+} = 3$ V		100			100		
Conversion time, t_{conv}	$V_{CC} = V_{REF+} = 5$ V	70			100			μs
Duration of start pulse, $t_{w(S)}$		100			100			ns
Duration of address strobe pulse, $t_{w(AS)}$		200			200			ns
Address setup time, t_{su}		50			50			ns
Address hold time, t_h		50			50			ns
Input voltage hold time		8			8			clock periods
Operating free-air temperature, T_A		−40		85	−40		85	°C

TL522 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 4)	T_A = 0°C to 85°C	2.75	3	5.5	V
	T_A = −40°C to 0°C	3		5.5	
Positive reference voltage, V_{REF+} (see Notes 3 and 4)		2.75		V_{CC}	V
Negative reference voltage, V_{REF-} (see Note 3)		0		0.3	V
Supply voltage relative to V_{REF+}, $V_{CC} - V_{REF+}$		0		1	V
Analog input voltage (see Note 3)		V_{REF-}		V_{REF+}	V
High-level control input voltage, V_{IH}		$0.7V_{CC}$			V
Low-level control input voltage, V_{IL}				$0.3V_{CC}$	V
Clock frequency, f_{clock}	$V_{REF+} = 5$ V		100	260	kHz
	$V_{REF+} = 2.75$ V (see Note 4)		100	130	
Conversion time, t_{conv} (see Note 5)		200			us
Duration of start pulse, $t_{w(S)}$		600			ns
Duration of address strobe pulse, $t_{w(AS)}$		600			ns
Address setup time, t_{su}		200			ns
Address hold time, t_h		150			ns
Input voltage hold time		8			clock periods
Operating free-air temperature, T_A (see Note 4)		−40		85	°C

NOTES: 3. Analog input voltage greater than V_{REF+} converts as all highs and less than V_{REF-} converts as all lows.
4. For proper operation of TL522 at free-air temperatures below 0°C, V_{CC} and differential reference voltage ($V_{REF+} - V_{REF-}$) must never be less than 3 volts.
5. Conversion time is a function of clock frequency, with 200 μs corresponding to a maximum clock frequency of 130 kHz.

TL520, TL521 electrical characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V to 5.25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −360 μA	4			V
V_{OL}	Low-level output voltage	I_O = 1.6 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current	V_O = 5 V			1	μA
		V_O = 0			−1	
I_{IH}	High-level control input current	$V_I = V_{CC}$ + 0.3 V			1	μA
I_{IL}	Low-level control input current	V_I = 0			−1	μA
$I_{I(op)}$	Peak analog input current (operating) (see Note 6)	$V_{CC} = V_{REF+}$ = 5 V, V_I = 2.5 V, f_{clock} = 200 kHz, T_A = 25°C		−5	−10	μA
$I_{I(stdby)}$	Analog input current (standby) (see Note 7)	V_{CC} = 5 V, V_I = 5 V, T_A = 25°C		10	200	nA
		V_{CC} = 5 V, V_I = 0, T_A = 25°C		−10	−200	
		V_{CC} = 5 V, V_I = 5 V, T_A = 85°C			1	μA
		V_{CC} = 5 V, V_I = 0, T_A = 85°C			−1	
I_{CC}	Supply current (see Note 8)	REF+ and REF− terminals open, f_{clock} = 200 kHz		10	50	μA
$I_{CC} + I_{REF+}$	Supply current plus reference current (see Note 8)	$V_{CC} = V_{REF+}$ = 5 V, V_{REF-} = 0, f_{clock} = 200 kHz		0.5	1	mA
		$V_{CC} = V_{REF+}$ = 3 V, V_{REF-} = 0, f_{clock} = 100 kHz		0.1		

†All typical characteristics are at V_{CC} = 5 V and T_A = 25°C (unless otherwise specified)

NOTES: 6. $I_{I(op)}$ is measured on a selected channel and decays exponentially during the first clock pulse.
7. $I_{I(stdby)}$ is measured on a selected channel with the clock input at 0 V.
8. Current increases linearly with frequency of the clock at the rate of approximately 10% per 100 kHz.

TL520, TL521 operating characteristics, T_A = 25°C, $V_{CC} = V_{REF+}$ = 5 V, V_{REF-} = 0, f_{clock} = 370 kHz for TL520 and 260 kHz for TL521 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TL520			TL521			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
k_{SVS}	Supply voltage sensitivity	$V_{CC} = V_{REF+}$ = 4.75 V to 5.25 V		0.05			0.05		%/V
	Linearity error (see Note 9)			±0.25			±0.5		LSB
	Origin error (see Note 9)			±0.25			±0.25		LSB
	Total unadjusted error (see Note 9)	T_A = 25°C		±0.25	±0.5		±0.5		LSB
		T_A = −40°C to 85°C			±0.75			±1	
t_{en}	Output enable time	C_L = 50 pF		100	250		100		ns
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ		100	250		100		ns
$t_{d(EOC-L)}$	Delay time, end-of-conversion output		0		100	0		100	ns

‡Typical values for all except supply voltage sensitivity are at V_{CC} = 5 V.

NOTE 9: All errors are measured with reference to an ideal straight-line transfer curve from 9.8 mV to 4.99 V with REF+ = V_{CC}.

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TL522 electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3 V to 5.25 V, f_{clock} = 125 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −1 μA		V_{CC}−0.05			V
		V_{CC} = 2.75 V, T_A = 0°C to 85°C	I_O = −0.1 mA,	2.35			
		I_O = −0.36 mA,	V_{CC} = 5 V				
V_{OL}	Low-level output voltage	I_O = −1 μA				0.05	V
		V_{CC} = 2.75 V, T_A = 0°C to 85°C	I_O = 0.4 mA,			0.4	
		V_{CC} = 5 V,	I_O = 1.6 mA			0.4	
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = 5.25 V,	V_O = 5.5 V			1	μA
			V_O = 0			−1	
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.5 V			1	μA
I_{IL}	Low-level input current	V_I = 0				−1	μA
$I_{I(op)}$	Peak analog input current (operating) (see Note 6)	V_{CC} = V_{REF+} = 3 V, f_{clock} = 125 kHz,	V_I = 1.5 V, T_A = 25°C		−5	−10	μA
$I_{I(stdby)}$	Analog input current (see Note 7)	V_{CC} = 3 V, T_A = 25°C	V_I = 3 V		10	200	nA
			V_I = 0		−10	−200	
		V_{CC} = 3 V, T_A = 85°C	V_I = 3 V			1	μA
			V_I = 0			−1	
I_{CC}	Supply current from V_{CC1}	REF+ and REF− terminals open			10	50	μA
I_{CC} + I_{REF}	Supply current plus reference current (see Note 8)	V_{CC} = V_{REF+} = 5 V, f_{clock} = 200 kHz	V_{REF-} = 0,		0.5		mA
		V_{CC} = V_{REF+} = 3 V, f_{clock} = 125 kHz	V_{REF-} = 0,		0.1	0.2	
C_i	Input capacitance				10		pF
C_o	Output capacitance				10		pF

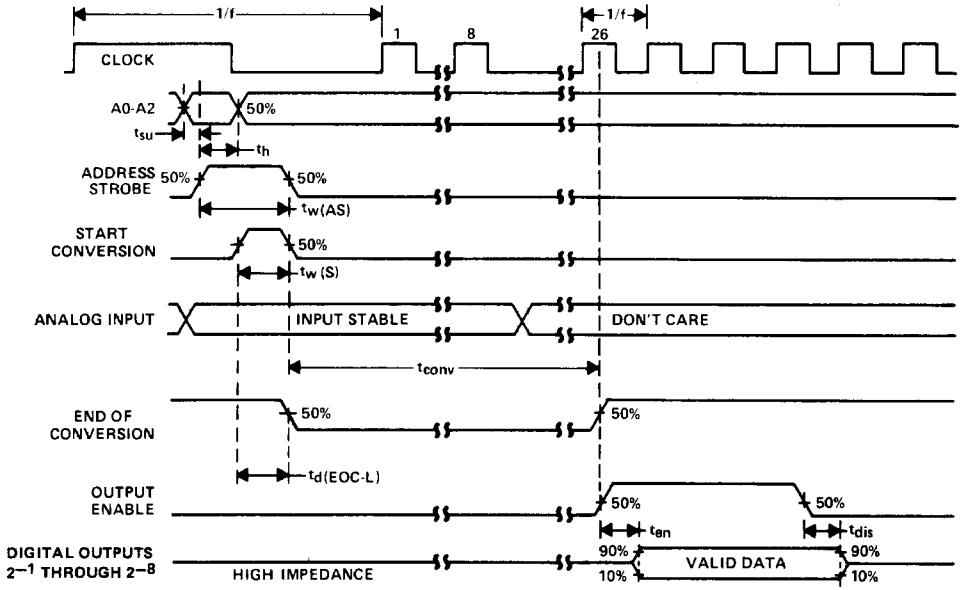
NOTES: 6. $I_{I(op)}$ is measured on a selected channel and decays exponentially during the first clock pulse.
7. $I_{I(stdby)}$ is measured on a selected channel with the clock input at 0 V.
8. Current increases linearly with frequency of the clock at the rate of approximately 10% per 100 kHz.

TL522 operating characteristics, T_A = 25°C, V_{REF+} = 3 V to 5.5 V, V_{REF-} = 0, f_{clock} = 130 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
k_{SVS}	Supply voltage sensitivity			0.05		%/V
	Linearity error (see Note 9)			±0.25		LSB
	Origin error (see Note 9)			±0.25		LSB
	Total unadjusted error (see Note 9)	V_{CC} = 2.75 V, T_A = 0°C to 70°C		±0.25	±0.5	LSB
		T_A = −40°C to 85°C		±0.25	±0.5	
t_{en}	Output enable time	C_L = 50 pF, R_L = 10 kΩ		0.7	1	μs
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ		0.6	0.8	μs
$t_{d(EOC-L)}$	Delay time, end-of-conversion output		0		100	ns

†All typical values are at V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)
NOTE 9: All errors are measured with reference to an ideal straight-line transfer curve from 9.8 mV to 4.99 V with REF+ = V_{CC}.

timing diagram



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PRINCIPLES OF OPERATION

timing diagram

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the input address code. The address strobe transfers and latches the address into the decoder on the positive-going edge of the signal. The output latch is reset by the postivie-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and lasts for 8 clock periods. The conversion process may be interrupted by a new start pulse before the end of 24 clock periods. The previous data will be lost if a new start of conversio occurs before the 24th clock pulse. Continuous conversion may be accomplished by connecting the end-of-pconversion output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 1). In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 of this capacitor is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF−. If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the reference voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF−. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF+ through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are counted.

With each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is succcessive approximation, but relies on charge shifting rather than a successive-approximation register (and reference D/A) to count and weigh the bits from MSB to LSB.

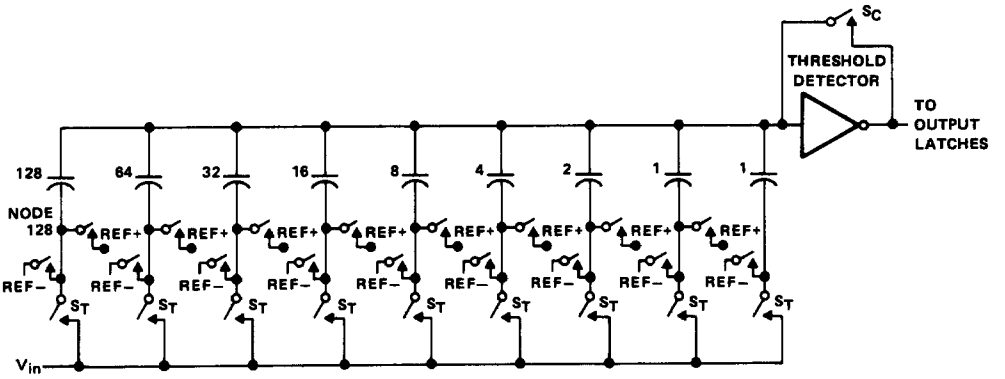


FIGURE 1–SIMPLIFIED MODEL OF THE SUCCESSIVE-APPROXIMATION SYSTEM

TYPICAL APPLICATION INFORMATION

The TL520, TL521, and TL522 are CMOS devices using charge redistribution to achieve A/D conversion. In typical applications as a ratiometric conversion system for a microprocessor, REF− will be connected to ground and REF+ will be connected to V_{CC}. The output will then be a simple proportional ratio between the analog input voltage and V_{CC} (Figure 3). The general relationship is

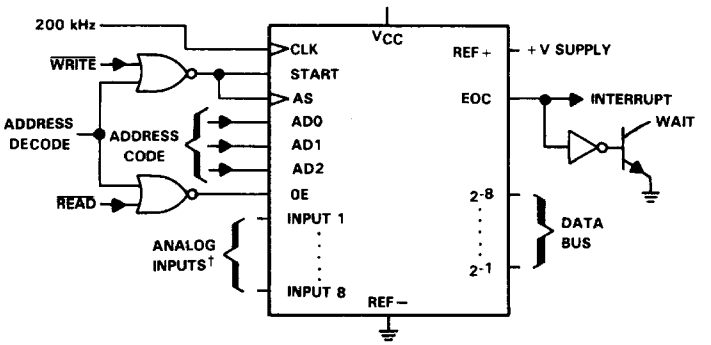
$$\frac{D_{out}}{2^8} = \frac{V_{in}}{V_{REF+} - V_{REF-}}$$

where D_{out} = decimal value of binary output word
V_{in} = analog input voltage
V_{REF+} = positive reference voltage = V_{CC}
V_{REF-} = negative reference voltage = V_{GND}

Latchup may overheat and destroy the device and may occur by either of two kinds of circumstances: out of range reference voltages or by incorrect power-up sequence. V_{REF+} should not be more positive than V_{CC} by more than 300 millivolts or V_{REF-} should not be more negative than GND by more than 300 millivolts. Apply V_{CC} before either of the reference voltages. The advantage of the compressed reference potential is that the full 8-bit resolution applies to be compressed voltage range (Figure 4). However, the cautions mentioned above must be observed. Operation at voltages down to V_{CC} = 3 volts is possible but limits the frequency to 100 kilohertz maximum and thus conversion time to 260 microseconds minimum. Interface for the common microprocessors is shown in Figure 2.

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
TMS7000	RD	WR	EINT
TMS9900	MEMEN	WE	INTREQ
8080	MEMR	MEMW	INTR (Thru RST Circuit)
8085	RD	WR	INTR (Thru RST Circuit)
Z-80	RD	WR	INT (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA + 2 R/W	VMA + 2 R/W	IRQA or IRQB (Thru PIA)



† The full-scale value of the analog input voltage can be shifted between 3 volts and 6.5 volts by varying V_{REF-} and V_{CC}, but only 5 volts guarantees TTL compatibility.

FIGURE 2 — TYPICAL MICROPROCESSOR APPLICATION

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TYPICAL APPLICATION INFORMATION

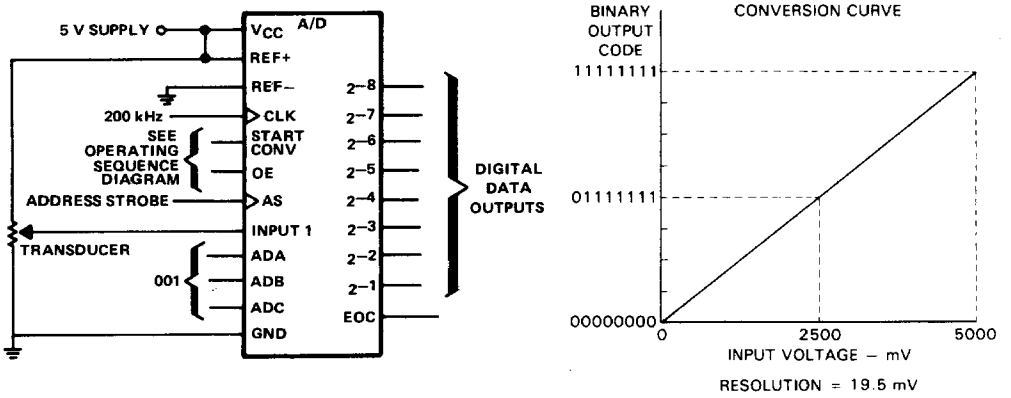

FIGURE 3 – RATIOMETRIC SYSTEM

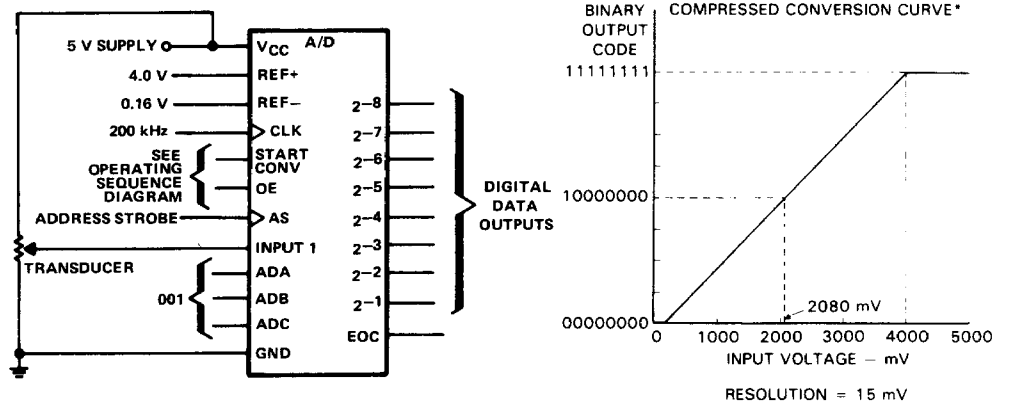

FIGURE 4–COMPRESSED RATIOMETRIC SYSTEM