FEBRUARY 1998
Revision 1.0

SXT6051

STM-1/0 SDH Overhead Terminator

General Description

The SXT6051 Overhead Terminator implements the Regenerator Section Termination, Multiplexer Section Termination and Higher Order Path Termination in STM-0 (51Mb/s) and STM-1 (155Mb/s) multiplexers. It provides micro-controller access for performance monitoring, alarm detection and configuration for transmit and receive paths. When used with the SXT6251 (21E1 Mapper), a complete solution for a 21 E1 or a 63 E1 Multiplexer is realized.

The SXT6051 is compliant with the latest releases of ITU-T G.703 and G.707. It provides all the alarm and control features to easily implement the multiplexer described in ITU-T G.783.

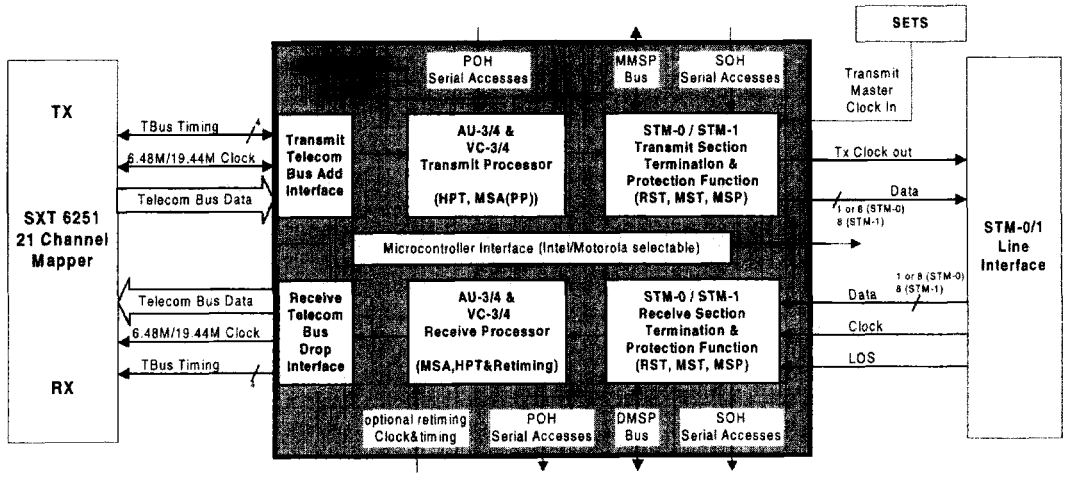
Applications

- SDH Terminal Mux/ADM for microwave radio
- ADM fiber ring Mux
- Digital Loop Carrier (NGDLC) Systems
- Digital Cross-Connect Systems

Features

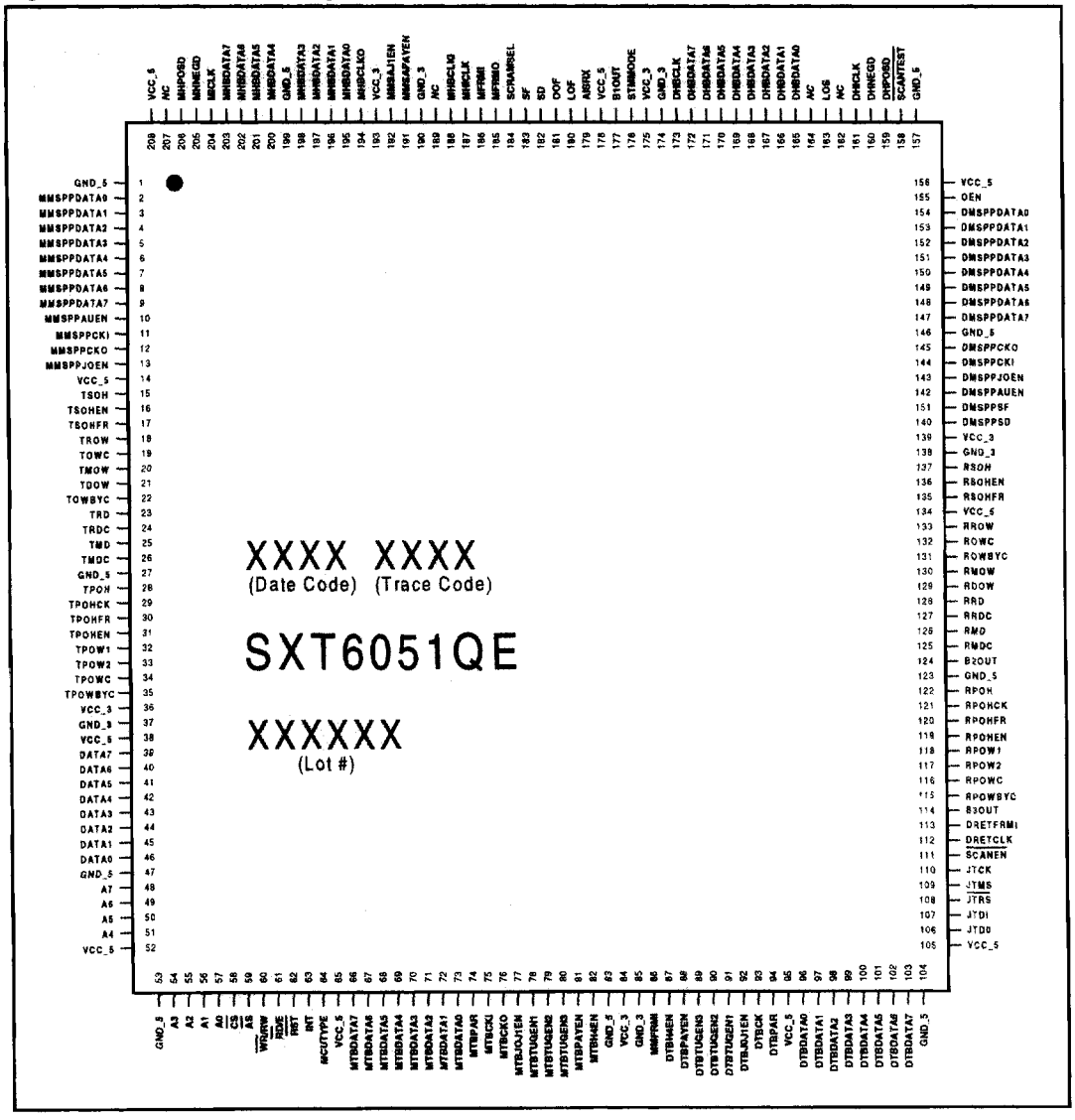
- Performs Regenerator Section, Multiplexer Section, and Higher Order Path Overhead Processing for STM-1 and STM-0 signals.
- Byte parallel interface for STM-1 or STM-0, with byte alignment performed internally. Serial NRZ or B3ZS interface option for STM-0.
- Demultiplexes STM-0/STM-1 signals to Telecom Bus output with optional pointer processor re-timing.
- Multiplexes Telecom Bus data into STM-0 or STM-1 signals with pointer processing.
- Compatible with 1+1 protected ITU architecture.
- Records all RSOH, MSOH, and HPOH alarms. One second counters for B1, B2, B3, M1 REI and G1 REI.
- Full J0/J1 trace identifier processing
- Serial access to STM-1 user-defined, media-dependent and national bytes.
- Dedicated pins for serial access or pass-through feature for E1, E2, F1, F2, F3, D1-D3 & D4-D12 bytes.
- Low power CMOS technology with 3.3V core and 5V I/O in PQFP-208 package.
- IEEE 1149.1 Boundary Scan (JTAG) support

SXT6051 System Block Diagram



PIN ASSIGNMENTS

Figure 1: SXT6051 Pin Assignment



OVERVIEW

Related Documentation

- SXT6051 Datasheet
- SXT6251 Product Overview
- SXT6251 Datasheet
- Application Note for the SFT SDH Chipset

Features

The SXT6051 implements the Regenerator Section Termination, Multiplexer Section Termination and Higher Order Path Termination in STM-0 and STM-1 multiplexers. A Microcontroller interface permits performance monitoring, alarm detection and configuration for transmit and receive paths. Figure 2 shows the functional blocks of the SXT6051. The following operation modes are supported:

- Repeater Mode—Terminates RSOH data only, passing through MSOH and VC-3 or VC-4 payload data
- Terminal Mode without Protection—Terminates RSOH, MSOH, and HPOH data
- Terminal Mode (Protection Main)—Terminates RSOH, MSOH, and HPOH data, implements multiplexer for K2 Multiplexer section protection of main or slave path
- Terminal Mode (Protection Slave)—Terminates RSOH, MSOH, interfaces to Main for K2 protection switching
- Add/Drop Mode without Protection—Terminates RSOH, MSOH, and HPOH data, and implements "pass through" mode for RSOH and MSOH bytes.
- Add/Drop Mode (Protection Main)—Terminates RSOH, MSOH, and HPOH data, Implements Multiplexer section protection switch, and provides ADM "pass through".
- Add/Drop Mode (Protection Slave)—Implements RSOH and MSOH termination with ADM "pass through"

Flexible Line Side Interface

The interface to STM-0 line interface devices can be serial (51.84 MHz) or parallel (6.48 MHz). The interface to STM-1 line interface devices is parallel (19.44 MHz).

The parallel interface does not require external frame synchronization. The parallel byte is rotated internally within the frame synchronization block.

Regenerator mode implements a "constant delay" feature that results in a pipeline delay of two complete bytes, regardless of the input byte rotation.

Pointer Processing

The receive section can optionally implement a pointer processing and re-timing function before the final output on the DTB Telecom bus. The receive data is synchronized with an external clock and frame synchronization signal to provide the J0 position. The payload pointers are adjusted as necessary, with positive and negative pointer events, and the new pointer value is multiplexed onto the telecom bus as well as A1/A2 byte.

The transmit section always implements pointer processing in ADM mode, synchronizing the MTB data with the output line clock. The payload pointers are adjusted as necessary, with positive and negative pointer events recorded in a counter and accessible via the microprocessor. In terminal mode, the payload received on the MTB bus is already synchronized via the telecom bus timing signals and the pointer value is set to 0.

Multiple Access to RSOH, MSOH and HPOH Bytes

Each orderwire and the two DCC channels (Dx, Ex, Fx bytes) are accessible via individual clock/data pin pairs and sync.

Ax framing and Bx parity bytes are automatically generated and monitored. All OH bytes except Ax and Bx can be accessed via four "framed" serial ports (data, clock, frame alignment pulse). There are separate ports for transmit and receive RSOH/MSOH and HPOH bytes. External circuits can generate or monitor any or all accessible OH bytes. Transmit source selection is made per byte via uP register bits.

National use bytes in STM-1 are accessible via uP register bytes, or via serial port. User Defined bytes & Media-Dependent bytes in STM-1 are accessible via serial port.

In ADM mode, the transmit source of E1, E2, F1, F2, F3, D1-D3 and D4-D12 bytes can be individually configured to

come from the telecom bus input, implementing the "pass through" mode.

Receive access to C2, K1, K2, K3 & S1 overhead bytes are provided via the uP registers.

In repeater mode, the transmit source of all RSOH bytes can be individually configured to come from the receiver input, implementing the pass through mode.

Trace Identifier Processing

The SXT6051 implements full J0 byte access with CRC-7 error-check and processing. The receive word is compared with the on-chip expected word, with maskable generation of the TIM alarm (which can cause AIS generation) and CRC-7 error alarm.

The SXT6051 also implements full J1 byte access, programmable as either a 16-byte word with CRC-7 error check or 64-byte word. The receive word is compared with the on-chip expected word. The SXT6051 has a maskable generation of the TIM alarm (which can cause AIS generation) and CRC-7 error alarm.

Telecom Bus Interface

The SXT6051 follows the industry standard Telecom Bus to interface with other SDH products, including the SXT6251. The standard is based on the original work of the IEEE P1396 project, which was never finalized. SFT has enhanced the bus to be compatible with other standard SDH products on the market.

In Terminal mode, the Multiplexer Telecom Bus implements contra-directional timing, meaning the SXT6051 generates the timing references (clock and signals) and receives the synchronized data. The Demultiplexer Telecom bus and the Multiplexer bus in ADM mode implements co-directional timing, where data and timing flow in the same direction

In Terminal mode, the transmit multi-frame can be synchronized by using an external 2 KHz reference signal connected to the MMFRMI input pin. This synchronization input signal can only be active High for a single frame and must be synchronous with MTBCLKO or MHBCKO outputs.

Several transmitters can be cascaded by cascading the synchronization. This is accomplished by connecting the output MTBH4EN of one chip (chip #1) to the input MMFRMI of a second chip (chip #2), etc. If no synchronization is required, MMFRMI is grounded.

Microcontroller Interface

The microprocessor interface is a generic asynchronous interface including an address bus (A<7:0>), data bus (DATA<7:0>), and handshaking signals (WR/RW, RD/E, CSB, and ALE). The MCUTYPE input pin indicates the type of microprocessor interface—Intel or Motorola. There is also an interrupt output pin (INT) that indicates status changes to the microprocessor.

Interrupt Sources

The SXT6051 provides status changes of a monitoring process. For example, the SXT6051 monitors the incoming STM frame for the correct framing pattern and updates the appropriate status bits to indicate the presence or absence of Out-Of-Frame and Loss-Of-Frame conditions. When the value of these status bits change, an interrupt can be generated.

The SXT6051 detects changes in several overhead bytes. For example, the SXT6051 stores the incoming K1 MSOH byte. When the value of the contents in this register changes, an interrupt can be generated.

The SXT6051 also monitors for counter overflows. For example, errors in the B1 parity byte are recorded in the B1 error counter. If the counter overflows, an interrupt can be generated.

Interrupt Enables

For an interrupt source to affect the state of the INT output pin, the associated interrupt enable bit must be set. For every interrupt source, there is an associated enable bit. The setting of the interrupt enables do not affect the updating of the status registers, the overhead byte registers, or the counters.

Radio Applications

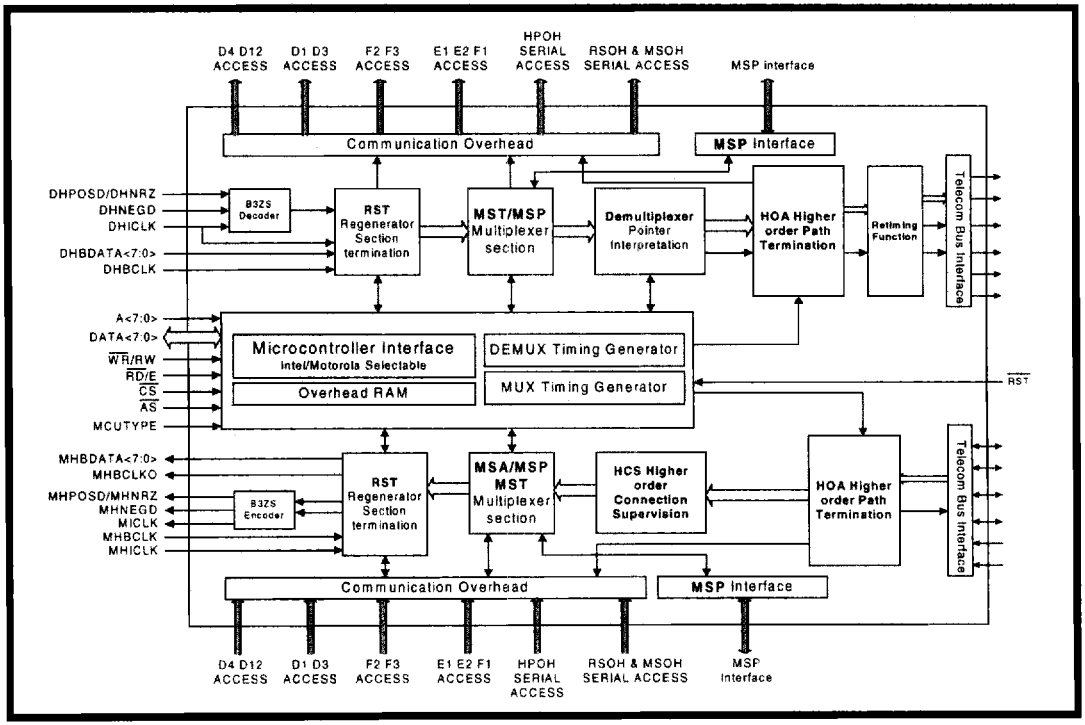
The SXT6051 implements a Programmable Scrambler Length. The standard ITU specified 2^7-1 scrambler at the Regenerator section of the chip, or extended scrambling at or 2^{11}-1 and 2^{13}-1 for radio applications is implemented

A unique frame synchronization in STM-0 provides extra robustness in radio applications and protection against false synchronization which exists within STM-0 systems using the ITU-T specified 2^7-1 scrambler.

Extensive Alarm Monitoring and Control

Numerous alarms are processed internally to the SXT6051, allowing the use of less powerful microcontrollers. Internal one second overflow counters exist for all BIP, REI, and pointer justification events. Configuration of Excessive Error indications are based on B2 for BER estimation. The SXT6051 also supports configuration of the Loss-Of-Frame alarm.

Figure 2: SXT6051 Block Diagram



Transmitter Data Flow

For the transmitter, the input interface is the Multiplexer Telecom Bus with byte wide data (MTBDATA <7:0>) and timing signals for the parallel clock (MTBCK), the frame indicator (MTBJ0J1EN), and the payload active signal (MTBPAYEN). The MTBPAR signal provides parity checking on the MTBDATA <7:0> byte data.

1. The data flow starts with the Higher Order Path Termination section which adds the VC-3 or VC-4 path overhead. After the HPOH data has been added, the Higher Order Connection Supervision block can insert an "unequipped" payload, if configured. A special pass-though mode exists for N1 tandem connection which allows the complete VC-3/4 to be passed through unchanged, including B3 and N1 BIP

- The **J1 byte** is sourced from a microprocessor programmable registers or TPOH input. The microprocessor must calculate the CRC7 byte of the J1 transmit string and store it in the first byte of the registers storing the string.
- The **B3 byte** is calculated internally and inserted. The microprocessor can invert the values of B3 for system testing purposes.
- The **C2 byte** is sourced from a microprocessor programmable register or TPOH input.
- The **G1 byte** is sourced from a microprocessor programmable register, TPOH input or by inserting the receive RDI and REI from the receive portion for the chip if automatic RDI and REI insertion is enabled by the microprocessor

- The **F2** and **F3 bytes** are two 64 Kbit/s channels sourced from TPOW1 and TPOW2 or received **F2** and **F3 bytes**. A clock, TPOWC (at 64 KHz) and TPOWBYC (at 8 KHz) provide the timing references for these channels.
- The **K3 byte** is sourced from a microprocessor programmable register or TPOH input.
- The **H4** multi-frame indicator is internally generated or synchronized to the 2KHz MFRMI signal.
- The **N1** byte can be sourced from the TPOH input.

2. Pointer processing re-timing is performed by the Multiplex Section Adaptation (MSA) section. Positive and negative pointer movement events are stored in counters that can be accessed via the microprocessor interface. The resulting parallel data stream is supplied to the Multiplex Section Termination (MST) and to the Multiplex Section Protection (MSP) port if it is configured as a protection master. The data MMSPPDATA<7:0> along with timing information is sent to the redundant (slave) SXT6051. Thus, both transmitters are synchronous in a 1-for-1 hot stand-by configuration.
3. The MST function adds the Multiplexer Section OverHead (MSOH):
   - The **K1** and **K2 bytes** are sourced from microprocessor programmable registers or TSOH input. In the particular case of **K2**, an internal process inserts the MS-RDI bits (K2<2:0>) based on the receive information if automatic MS-RDI insertion is enabled by the microprocessor.
   - The **D4-D12** bytes are sourced from the TMD input or received **D4-D12 bytes**. A 576 KHz reference clock is supplied at TMDC.
   - **S1** is sourced from the microprocessor programmable register or TSOH input.
   - **M1** is sourced from the TSOH input or an internal process that sets **M1** based on the B2 byte(s) errors from the receive portion of the SXT6051 if automatic MS-REI insertion is enabled by the microprocessor.
   - **E2** is sourced from the TMOW input or received **E2** byte. A 64 KHz reference clock is supplied at TROWC and an 8 KHz sync pulse at TROWBYC.
   - The **B2** byte is calculated internally and inserted. The microprocessor can invert the values of **B2** for system testing purposes.
4. The Regenerator Section OverHead (RSOH) is added by the Regenerator Section Termination (RST).
   - The **J0** byte is sourced from the microprocessor, TSOH input or received **J0** byte. The microprocessor must calculate the CRC7 byte of the **J0** transmit string and store it in the first byte of the registers storing the string.
   - The **B1** byte is calculated internally and inserted. The microprocessor can invert the values of **B1** for system testing purposes.
   - **E1** is sourced from the TROW input or the received **E1** byte. A 64 KHz reference clock is supplied at TROWC and an 8 KHz sync pulse at TROWBYC.
   - **F1** is sourced from the TMOW input or received **F1** byte. A 64 KHz reference clock is supplied at TROWC and an 8 KHz sync pulse at TROWBYC.
   - **D1-D3** are sourced from the TRD input or received **D1-D3** bytes. A 192 KHz reference clock is supplied at TRDC.
5. Finally, the data is scrambled with the configured scrambler type and framing bytes A1/A2 are added. For STM-1, and optionally STM-0, the data is output on the byte parallel bus MHBDATA<7:0> synchronous with the MHBCLKO clock. In STM-0, the output can also be converted from parallel to serial and emitted as NRZ data on MHPOSD, or output as B3ZS encoded data on MHPOSD and MHNEGD. The input selection is configurable via the microprocessor.

Receive Data Flow

1. STM-1 data is input on the parallel, NRZ data bus. Timing is provided by a programmable, parallel data clock. STM-0 data and clock signals can be entered as either parallel data like STM-1, as serial NRZ data, or as B3ZS encoded data. The B3ZS inputs are decoded and the resulting NRZ data converted to parallel format. Timing is provided by the serial data clock.
2. The parallel data is then fed to the framing and de-scrambling block. The framing block synchronizes the timing generator to the incoming data and provides Out-Of-Frame and Loss-Of-Frame alarm signals. These alarms are based on frame counts that can be programmed via the microprocessor interface.
3. After frame synchronization and de-scrambling, the Regenerator Section Termination (RST) logic extracts the Regenerator Section Overhead (RSOH).
   - The expected value of the **J0** string is stored via the microprocessor interface. The receive value of **J0** is compared with the stored version, and also used to calculate a CRC-7 byte. Two alarms can be generated: a J0 (Trace ID) Mismatch alarm and J0 CRC-7 mismatch alarm.

- **B1** byte is calculated internally and compared to the incoming **B1** value. The errors are stored into a set of counters that can be read by the microprocessor interface.
- **E1** is provided serially at the RROW output.
- **F1** is provided serially at the RMOW output. **E1** and **F1** are synchronous and can be accessed synchronously using the 64 KHz clock provided at RROWC and the 8 KHz synchronization pulse provided at RROWBYC.
- **D1-D3** are provided serially at the RRD output. The 192 KHz clock reference for this output is provided at RRDC.

4. Next, the Multiplexer Section Termination (MST) extracts the MSOH.
   - **K1** and **K2** bytes are provided via both microprocessor registers and serially at the RSOH output. A filter based on 3 consecutive identical values of **K1** and **K2** gates the update of the microprocessor registers.
   - **D4-D12** bytes are provided serially at the RMD output. The 576 KHz clock reference for this output is provided at RMDC.
   - **S1** is provided via both a microprocessor register and serially at the RSOH output. A filter based on 3 consecutive identical values of **S1** gates the update of the microprocessor register.
   - **M1** is provided serially at the RSOH output and updates MST REI counters accessible by the microprocessor.
   - **E2** is provided serially at the RMOW output. The 64 KHz clock reference for this output is provided at RROWC and the 8 KHz sync pulse at RROWBYC.
   - **B2** byte is calculated internally and compared to the incoming B2 value. The errors are stored into a set of counters that can be read by the microprocessor interface. These errors are also inserted in the transmitted **M1** byte if enabled.
5. The Multiplexer Section Protection (MSP) block allows the data presented to the Master Multiplexer Section Adaptation (MSA) block to come from either the "Master MST output data" or "Slave MSP output data." The choice is completely under the control of the microprocessor. The microprocessor has access to all the Master and Slave data (K1/K2 bytes, error statistics derived from counters and alarm status from both chips) necessary for making this decision.
6. The MSA block interprets the H1-H3 bytes to determine the location of the VC-3 or VC-4 payload structure. Positive and negative pointer movement events are stored in counters that can be accessed via the microprocessor interface. The data from the MSA section is then output to the High Order Path Termination (HPT) section in a byte parallel format.
7. The HPT section then extracts the HPOH.
   - The expected value of the **J1** string (16 or 64 byte) is stored via the microprocessor interface. The receive value of **J1** is compared with the stored version, and also used to calculate the CRC-7 byte (if 16 byte word). Two alarms can be generated: a J0 (Trace ID) Mismatch alarm and J0 CRC-7 mismatch alarm (16 byte).
   - **B3** byte is calculated internally and compared to the incoming **B3** value. The errors are stored into a set of counters that can be read by the microprocessor interface.
   - The **C2** byte is monitored for changes or a mismatch from the expected value programmed in a register. Errors are indicated as either Signal Label Mismatch, AIS, or Unequipped alarms, depending on the value. Unequipped indication requires other conditions to be met. The value of **C2** can also be read from a register.
   - The **G1** byte supports Remote Error Indication (REI). and Remote Detection Indication (RDI). They, along with G1<0> ("spare" bit), are accessible via a register and alarms indicated.
   - **K3** is provided via a microprocessor register. A filter based on 3 consecutive identical values of **K3** gates the update of the microprocessor register.
   - **N1** is accessible at the RPOH output
   - **F2** and **F3** Bytes are serially accessible via the RPOW1 pin for **F2** and RPOW2 for **F3**. The 64 KHz clock and 8KHz synchronization are provided on pins RPOWC and RPOWBYC.
   - The **H4** byte is monitored for multi-frame synchronization. A Loss of Multiframe (LOM) alarm is indicated in a register after two multi-frames.
8. The last block is the optional re-timing block. This block allows the alignment of the receive payload with the external 8KHz synchronizing pulse (which supplies the J0 position) and an external clock. A new value of the pointer, based on the new alignment position, is assigned to the payload. Typically, this block is bypassed for a multiplexer application. It is only required for external re-timing and alignment of multiple TUG-3 payload signals.
9. The output of the re-timing block is then sent to the Receive Telecom Bus, along with the demultiplexer bus clock and some reference timing signals.