



# RFW-D100: Standard Interface to the RFW100 Series

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## RFW-D100

Vishay RFWaves



The company's products are covered by one or more of the following:

Taiwan Patent No. 155994, Taiwan Patent No. 176767, USA Patent No. 6,535,545. Other patents pending.

### DESCRIPTION

The RFW-D100 is a complimentary chip to the RFW122 chipset. The D100 provides a parallel interface to a MCU (microcontroller unit). It also provides other features, that enable implementing the protocol suitable for wireless communication.

VISHAY ADVANCED TECHNOLOGIES LTD. - RFWAVES DIVISION ("RFWAVES") has developed a very low cost wireless modem (RFW122) for short range, cost sensitive applications. The modem is a physical layer element (PHY) – allowing the transmission and reception of bits from one end to the other.

In an RFWaves application, the MCU is in charge of the MAC layer protocol. The RFW-D100 was developed in order to reduce the real time demands of the MCU handling the MAC protocol. The RFW-D100 gives the MCU an easy parallel interface with the RFW122, similar to memory access. It converts the fast serial input to 8-bit words, which are much easier for an 8-bit MCU to work with. In addition, it requires a lower rate oscillator. It buffers the input through a 16-byte FIFO, giving the MCU access to the RFW-D100 more efficiently. Instead of reading one byte per interrupt, the MCU can read up to 16 bytes in

### FEATURES

- Provides parallel interface with the RFW122\* modem.
- Serial-to-parallel conversion of the RFW122 interface
- Input FIFO (RX\_FIFO)
- Output FIFO (TX\_FIFO)
- Preamble correlation
- Packet address filter (Network and unique)
- CRC calculation
- Watchdog timer driven by internal RC-oscillator
- Working frequencies: 6-24 MHz
- Power save modes: Idle, power down
- Inter-RFWaves networks Carrier sense
- Discharge of the RFW122 reference capacitor
- Compensation for clock drifts between the transmitting RFW-D100 and the receiving RFW-D100 up to 1000 ppm. Hence, the RFW-D100 requires low performance crystal
- Interrupt driver – connected to the MCU's external interrupt and informs the MCU about RFW-D100 events.
- Identifies strong transmissions on channel (RSSI). Used for Carrier sense mechanism.

\* Any reference to the RFW122 includes the RFW102/RFW112.

each interrupt. In cases where each incoming byte causes an interrupt, this reduces the MCU's overhead in reading incoming words, such as stack stuffing and pipeline emptying. When using the FIFO, the MCU pays the same overhead for all the FIFO bytes, as it paid for only one byte without a FIFO.

A low-cost RFW-D100 with a built-in state machine that can support basic wireless communication elements has the following advantages:

- Shorter development time, hence shorter time-to-market
- save CPU power and other resources for other applications
- Offer an easy, standard integrated solution



Not for new design, this product will be obsoleted soon

**RFW-D100**  
Vishay RFWaves

**PIN ASSIGNMENTS**

**LQFP-44 Package - PIN FUNCTION**

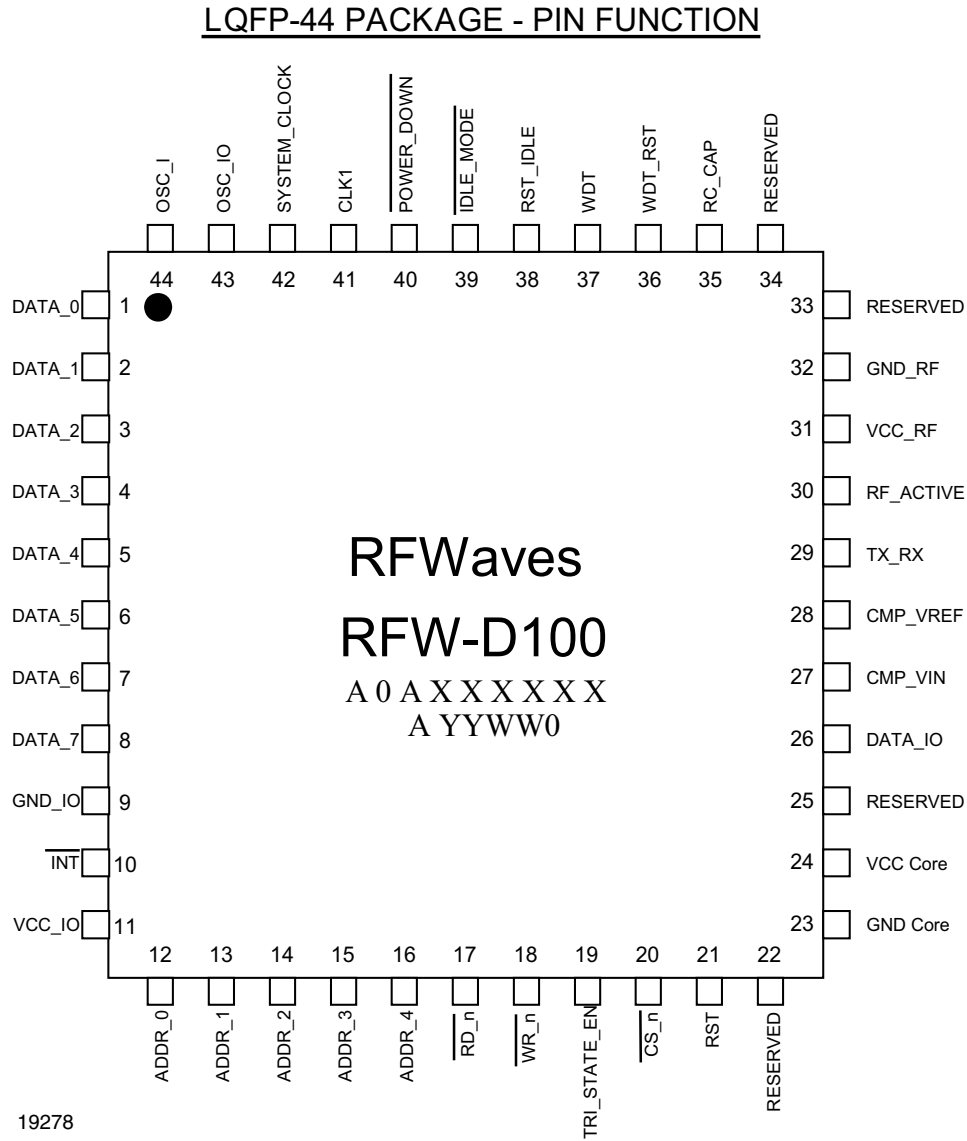
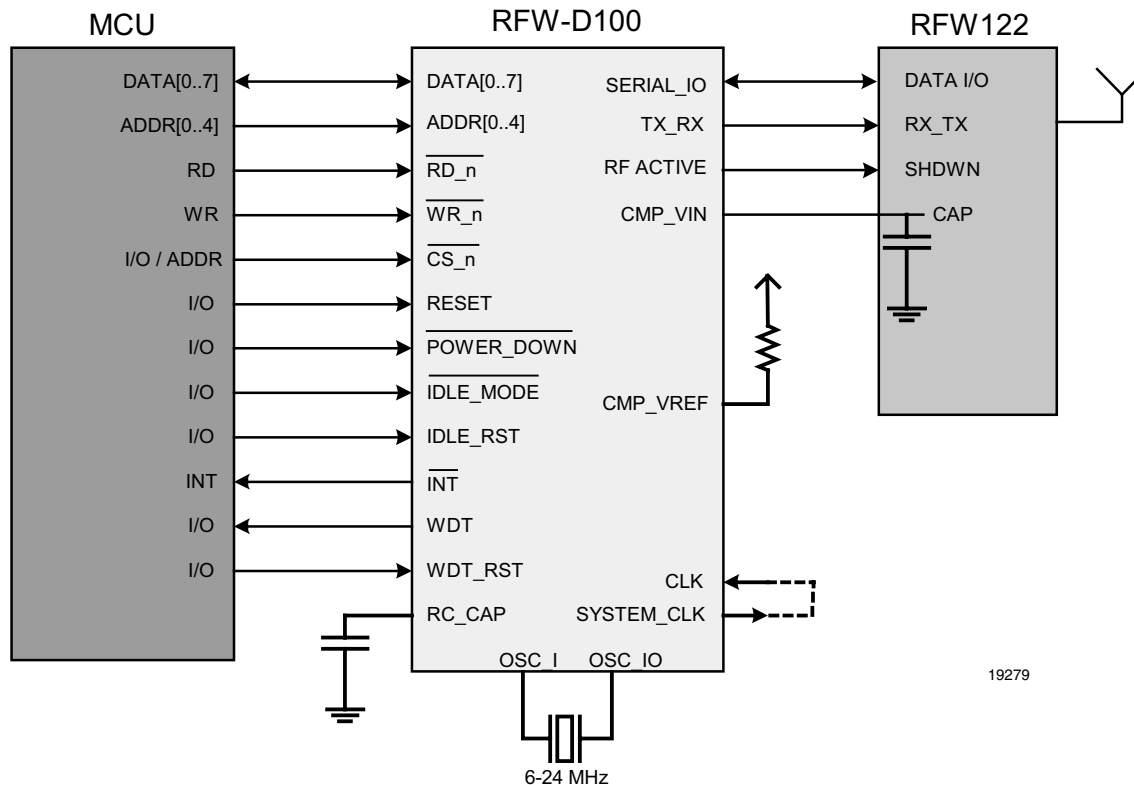


Figure 1. The FRW-D100 - LQFP-44

**RFW-D100 INTERFACE DESCRIPTION**



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Figure 2. RFW-D100 Interface Description

- (1) DATA\_I/O, RX\_TX, SHDWN, and CAP are signals coming from the RFW122 six holes connector. DATA\_I/O is pin number 3. RX\_TX is pin number 1. SHDWN is pin number 4. CAP is pin number 2
- (2) In the above figure, the capacitor connected to pin CAP from the RFW122 is an internal capacitor in the RFW122.



| PIN DESCRIPTIONS    |                  |            |   |
|---------------------|------------------|------------|---|
| Name                | LQFP Pin Numbers | Type       | Description   |
| DATA [0..7]         | 1 - 8            | I/O<br>(U) | This bus comprises eight TRI-STATE input/output lines. The bus provides bi-directional communication between the RFW-D100 and the MCU. Data, control words, and status information are transferred via the DATA[0-7] data bus.  |
| RD_n                | 17               | I<br>(U)   | When RD_n is low while the RFW-D100 is enabled (CS_n='0'), the RFW-D100 outputs one of its internal register values to DATA[0-7] according to ADDR[0-4].  |
| WR_n                | 18               | I<br>(U)   | When WR_n is low while the RFW-D100 is enabled (CS_n='0'), the RFW-D100 enables writing to its internal registers. The register is determined by ADDR [0-4] and the value by DATA [0-7].  |
| ADDR [0..4]         | 12 - 16          | I<br>(U)   | These five input signals determine the register to which the MCU writes or reads from.  |
| CS_n                | 20               | I<br>(U)   | Chip select input pin. When CS_n is low, the RFW-D100 is selected; when high, the RFW-D100 is disabled. This pin overrides all pins excluding RST. This enables communication between the RFW-D100 and the MCU.   |
| INT                 | 10               | O          | Interrupts driver pin. This pin goes low whenever any of the interrupts that are enabled in IER have occurred. The purpose of this pin is to notify the MCU through its external interrupt pin that an event (such as empty TX_FIFO) has occurred. Goes high when the IER register is read.   |
| RST                 | 21               | I<br>(X)   | Chip's reset pin. When this pin is set high, all registers and FIFOs are cleared to their initial values. All transceiver traffic is disabled and aborted. Reset is asynchronous to clock input (CLK1). After power-up, a pulse in RST input should be applied (by POR).  |
| WDT                 | 37               | O          | Watchdog timer output. This pin goes high every time the FRC counter overflows. The pulse duration is determined by FRC-H(4:6) register.  |
| SYSTEM_CLK          | 42               | O          | This pin is the oscillator block output (see Figure 3). It should be connected to the CLK input .   |
| DATA_IO (*)         | 26               | I/O<br>(X) | Serial input or output according to TX_RX mode. It functions as the serial interface for the RFW122 (RFWaves modem). When DATA_IO is input, it is a Schmitt-trigger input. A weak pull-up should be applied to this pin.  |
| TX_RX (*)           | 29               | O          | This pin controls the RFW122 operation mode. It should be connected to the RFW122 RX_TX input pin. When TX_RX is low, the RFW122 is in receiving mode. When RX_TX is high, the RFW122 is in transmitting mode. In most cases TX_RX output pin is determined by SCR2(0) register. SCR3(7) and the capacitor discharge mechanism affect this pin. |
| RF_ACTIVE (*)       | 30               | O          | This output pin controls the RFW122 working/shutdown mode. Its value is determined by SCR4(1).  |
| VCC <sub>CORE</sub> | 24               |            | This pin is the power supply input for the core logic of RFW-D100. A 0.1 μF power bypass capacitor should be placed between VCC <sub>CORE</sub> and GND <sub>CORE</sub> to prevent voltage droppings.   |
| GND <sub>CORE</sub> | 23               |            | This pin is the ground for the core logic of RFW-D100.  |
| VCC <sub>IO</sub>   | 11               |            | This pin is the power supply input for the I/O cells of RFW-D100. A 0.1 μF power bypass capacitor should be placed between VCC <sub>IO</sub> and GND <sub>IO</sub> to prevent voltage droppings.  |
| GND <sub>IO</sub>   | 9                |            | This pin is the ground for the I/O cells of RFW-D100.   |
| VCC <sub>RF</sub>   | 31               |            | This pin is the power supply for the I/O interface of RFW-D100 towards the RF module (TX_RX, DATA_IO, and RF_ACTIVE). A 0.1 μF power bypass capacitor should be placed between VCC <sub>RF</sub> and GND <sub>RF</sub> to prevent voltage droppings. Normally, this capacitor should be common to the RF module VCC as well.                    |
| GND <sub>RF</sub>   | 32               |            | This pin is the ground for the interface of RFW-D100 towards the RF module (TX_RX, DATA_IO, and RF_ACTIVE).   |
| OSC_I               | 44               | I          | This pin is the input of the inverting oscillator amplifier.  |



| PIN DESCRIPTIONS |                  |          |  |
|------------------|------------------|----------|--|
| Name             | LQFP Pin Numbers | Type     | Description  |
| OSC_IO           | 43               | I/O      | This pin is the output of the inverting oscillator amplifier.  |
| POWER_DOWN       | 40               | I<br>(X) | This pin controls the power down mode of the RFW-D100. When this pin is set low, the clock generation in the oscillator block is disabled. Going into power down and getting out of this mode will be discussed in detail later on. When this pin is set high, the oscillator block is enabled.  |
| IDLE_MODE        | 39               | I<br>(U) | The IDLE_MODE pin controls the output of the oscillator block through the SYSTEM_CLOCK pin. When the IDLE_MODE is high, the oscillator output through the SYSTEM_CLOCK is enabled. When the IDLE_MODE is low, the oscillator output is disabled. This pin is used to implement power down mode and idle mode. Further details follow later in this document. |
| IDLE_RST         | 38               | I<br>(X) | The IDLE_RST pin controls the output of the oscillator block through the SYSTEM_CLOCK pin. When IDLE_RST is low, the oscillator output through the SYSTEM_CLOCK is enabled. When IDLE_MODE is high, the oscillator output is disabled. This pin is used to implement power down mode and idle mode. Further details follow later in this document.           |
| WDT_RST          | 36               | I<br>(X) | WDT_RST when high, resets the WDT counter. If the WDT is enabled, the WDT counter starts counting from 0 again.  |
| CMP_VIN          | 27               |          | Comparator input.  |
| CMP_VREF         | 28               |          | Comparator reference voltage.  |
| CLK1             | 41               | I<br>(X) | Primary clock input to the RFW-D100.   |
| TRI_STATE_EN     | 19               | I<br>(U) | In normal working mode, this pin should be set high constantly. When set low, all the RFW-D100's outputs and bi-directional pins are in tri-state.   |
| RC_CAP           | 35               |          | RC oscillator's capacitor is connected to this signal.   |
| RESERVED         | 34, 33, 25, 22   | I<br>(D) | In normal working mode, these pins should be set low constantly. These pins are used for testing.  |

Note 1: All input pins are Schmitt-trigger inputs.

Note 2: All output pins that are marked with '\*' (DATA\_IO, RF\_ACTIVE, TX\_RX) have a 2 mA output buffer. The rest of the output pins have an 8 mA output buffer.

Note 3: For each input pin or bi-directional pin in input mode, in the Type column: (D) specifies a pull-down, (U) specifies a pull-up, and (X) specifies no internal pull-up or pull-down.

**RFW-D100 ARCHITECTURE**

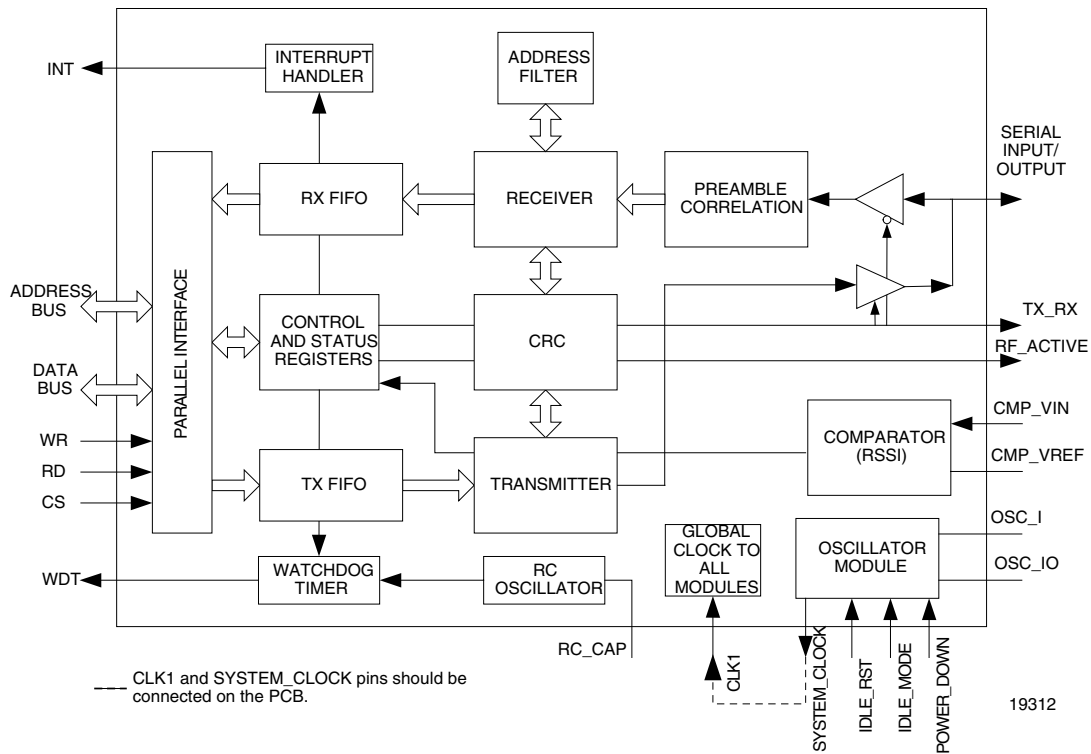


Figure 3. Block Diagram of the RFW-D100 Internal Structure

**RFW-D100 DESCRIPTION**

**Oscillator Characteristics**

The oscillator module can be used as the source of clock to the RFW-D100. It is a stand alone module that can be bypassed. Optionally, an external oscillator can drive the RFW-D100, since the CLK1 pin is a primary clock input to the RFW-D100. When the oscillator module is used, its output SYSTEM\_CLOCK should be connected to the RFW-D100 primary clock input CLK1. Here, the oscillator module controls the RFW-D100's working modes: power down, idle mode,

and working mode. The oscillator module input pins [POWER\_DOWN(40), IDLE\_MODE(39), and IDLE\_RESET(38)] determine the working mode.

The oscillator module is connected to the external crystal through pins OSC\_I and OSC\_IO in pierce topology as shown in Figure 4. C1, C2, and R<sub>d</sub> should be set according to the type of the crystal. R<sub>feb</sub> should be around 1 MO. The crystal frequency can be between 6 ↔ 24 MHz.

**OSCILLATOR CHARACTERISTICS**

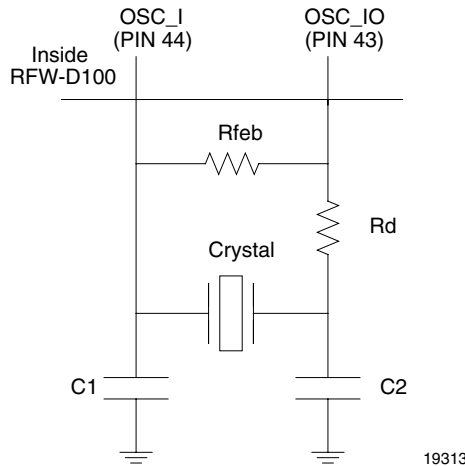


Figure 4. RFW-D100's Oscillator Topology

**RESET**

A reset is achieved by holding the RST pin high for at least 10 oscillator cycles. The reset initializes the RFW-D100 and all of its registers to their initial state.

To ensure good power up, a reset should be given to the RFW-D100 after power up.

**POWER SAVING MODES**

The RFW-D100 was designed to work in similar working modes as the typical MCU.

These modes enable the system to save power when the RFW-D100 is not in use.

**POWER DOWN MODE**

The MCU is able to halt all activity in the RFW-D100 by stopping its clock. This enables the MCU to reduce the power consumption of the RFW-D100 to a minimum.

All registers and FIFOs retain their values when the RFW-D100 is in power-down mode.

In working mode: POWER\_DOWN='1', IDLE\_MODE='1', and IDLE\_RST='0'.

If the MCU wants to put the RFW-D100 into power-down mode, it should do the following:

1. IDLE\_MODE = '0'.
2. WAIT 10  $\mu$ s.
3. POWER\_DOWN = '0'.
4. POWER\_DOWN pin should be kept low as long as the RFW-D100 is in power down mode.
5. IDLE\_MODE = '1' – So this input will be compatible with its internal pull up to lower power consumption in power down mode.

If the MCU wants to wake the RFW-D100 from power-down mode back to working mode, it should do the following:

1. IDLE\_RST = '1'.
2. IDLE\_MODE = '0'.
3. POWER\_DOWN = '1'.
4. WAIT Oscillator Wakeup Time until oscillator is stable.
5. IDLE\_RST = '0'.
6. IDLE\_MODE = '1'.
7. Exit 'Low Mode'.

The wakeup time of the RFW-D100 from power-down mode to fully operating mode is depended on the crystal type. Typically it should be a few milliseconds.

Since the RFW-D100 retains all the register values in power-down mode, special attention should be paid to the register values before it enters power-down. For example, the MCU should check that the RFW-D100 is not in the middle of transmitting or receiving a packet.

The RFACTIVE should be set low to shut down the RFW122, before entering power down mode.

Power consumption in power down mode is < 1  $\mu$ A, if RC\_OSC is disabled.

Power consumption in power down mode is < 10  $\mu$ A, if RC\_OSC is enabled.



### IDLE MODE

In idle mode, the RFW-D100 internally blocks the clock input. The external clock is not stopped, but it is not routed to the internal logic. By doing this, the MCU achieves substantial power savings, and yet the wakeup time is still relatively short. The power consumption is not minimal since the external clock is still active.

All registers and FIFOs retain their values when the RFW-D100 is in idle mode.

The RFW-D100 enters idle mode by setting IDLE\_MODE pin to "0". SYSTEM\_CLOCK pin does not output the oscillator clock.

The RFW-D100 goes back to working mode by setting the IDLE\_MODE pin to "1".

Since the RFW-D100 retains all the registers' values in idle mode, special care should be given to the registers' values before the RFW-D100 enters idle mode. For example, the MCU should check that the RFW-D100 is not in the middle of transmitting or receiving a packet. In addition, the RFACTIVE should be set low, in order to shut down the RFW122.

### PREAMBLE CORRELATION

The transmitting RFW-D100 sends the PREAMBLE in order to synchronize the receiver with its transmission. The RFW-D100 transmits a fixed size PREAMBLE of 20 bits. The first 4 bits are "1111". Their purpose is to initiate the RFW122 on the receiver side. The other 16 bits are determined by PRE-L and PRE-H. They are transmitted from MSB to LSB.

The received PREAMBLE has a variable length of 16 ⇔ 9 bits, determined by SCR2 [5:7]. The receiver correlates the 16 ⇔ 9 bits from its PRE-L and PRE-H registers to the 16 ⇔ 9 bits in its input shift-register. If a correlation was found, then the RFW-D100's receiver state machine is enabled.

The purpose of the PREAMBLE is to filter RFWaves packets from white noise or other transmissions on the channel. Whereas, NODE\_ID and NET\_ID filters are used to filter packets from other RFWaves networks (see section 0).

The PREAMBLE is transmitted MSB to LSB (PRE-H first and then PRE-L).

The value of the PREAMBLE is determined according to PRE-L and PRE-H registers for both the transmitter and the receiver.

The value of the PRE-L and PRE-H registers should be identical in the RFW-D100 in all nodes in the same network.

### REFRESH BIT

When receiving a valid packet, the RFWaves modem (PHY layer) has to receive a "1" symbol each time a certain period has elapsed in order to maintain its sensitivity. The time between adjacent "1" symbols is determined by the value of the reference capacitor. This constraint is transparent to the application layer since the RFW-D100 adds a "1" symbol (refresh bit) if too many "0" symbols are transmitted consecutively. On the receiver side, these additional "1" symbols (refresh bits) are removed by the RFW-D100.

This refresh bit is transparent to the application layer. The only thing the application layer has to do is initialize the maximum allowed number of consecutive x "00" bytes.

The RFW-D100 has the flexibility to add a refresh bit every 1 to 7 bytes. This is configured by RB(0:2) bits in PPR register. The value of RB(0:2) bits in PPR register determines the overhead the refresh bit has on the throughput of the link.

The refresh bit does not add substantial overhead to the bit stream, since it is only added when the number of consecutive x "00" bytes exceeds a certain value.

The data that is sent is application dependent, so the application can be adjusted so that there will be a negligible probability of this event occurring.

Example of how to calculate the refresh bit value:

Typical RFWaves capacitor: C=1 nF

Normal discharge current = 200 nA

Each 10 mV on the capacitor represent 1 dB in receiving power.

$$\Delta t = \frac{C \cdot \Delta V}{I} = \frac{1\text{nF} \cdot 10\text{mV}}{200\text{nA}} = 50 \mu\text{s}$$

The capacitor is charged with each received "1" symbol.

The receiver is allowed to lose about 2 dB before a new "1" is received.

Thus, after each 100 consecutive "0" bits in 1 Mbps (100 μsec), a "1" symbol should be sent.

In this case, setting RB(0:2) in PPR register to be 7 ("111") would be sufficient (7 bytes = 56 bits).

When RB(0:2) bits are set to "000" a refresh bit is added to every transmitted byte, regardless of its content. This introduces a constant overhead of 12.5 %.

### BIT STRUCTURE

The RFW-D100 uses an oscillator ranging from 6 ⇔ 24 MHz. In order to determine the output and input bit rate, the RFW-D100 must be configured to the



number of clock cycles contained in each bit. This gives the applicator the control over the bit rate with certain restrictions. Each bit must have at least 6 clock cycles.

The maximum bit rate is: 1 Mbps

The minimum bit rate is: 10 Kbps (TBD)

However, it is recommended to work only at 1 Mbps, since reducing the bit rate does not change the energy of a transmitted bit. In other words, reducing the bit rate does not improve the bit error rate or the range between the transmitter and the receiver.

Bit Length Register (BLR) determines the number of clock cycles per bit (bit period).

The BLR value is given a fixed offset of 6, since the minimum number of clock cycles in one bit is 6.

Bit Rate = Oscillator/(BLR + 6).

For example, if the input clock frequency is 12 MHz and the wanted bit-rate is 1 Mbit/sec, then the BLR should be set to 6 ( $12 / (6 + 6) = 1$  Mbps). Other examples of setting the BLR are shown in Table 2:

| BLR REGISTER SETTING         |                                  |           |
|------------------------------|----------------------------------|-----------|
| Required Bit Rate (Mbit/sec) | RFW-D100's Clock Frequency (MHz) | BLR Value |
| 1                            | 6                                | 0         |
| 1                            | 12                               | 6         |
| 1                            | 18                               | 12        |
| 1                            | 24                               | 18        |
| 0.5                          | 12                               | 18        |
| 0.1                          | 1                                | 4         |

The RFW-D100 outputs (for the RFW122) the bit structure shown in Figure 5.

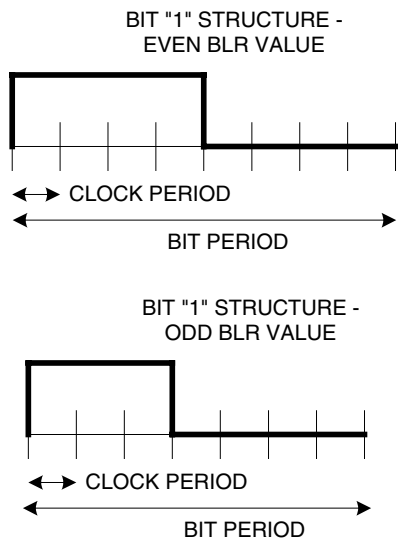


Figure 5. RFW-D100's Bit Structure

In the even clock number example, one bit contains 8 cycles of clocks and BLR=2.

In the odd clock number example, one bit contains 7 cycles of clocks and BLR=1.

The number of clocks when the line is "1" is determined as follows:

Number of "1"s = FLOOR\* ((BLR + 6)/2).

In case of "0" bit, RFW-D100 output "0" value for BLR + 6 clock pulses.

\* FLOOR - Rounds towards zero

**CRC**

The CRC is a redundant code, which is calculated and added to each packet on the transmitter side. The CRC enables the receiver to detect errors in the received packets.

The RFW-D100 adds additional CRC information to each packet in the transmitter module, in order to enable the protocol to detect errors. The CRC is also calculated on the receiver side. The CRC calculation result of the receiver and the CRC field in the received packet are compared in the receiver by the CRC module in the RFW-D100 (see Figure 3). If the CRC results are equal, then the receiver knows with reasonable probability that the packet was received correctly. If the CRC results are not equal, then the receiver knows with probability that the packet was received incorrectly.

The CRC mode is configured by the PPR (3:4) register.

Both the receiving mode and the transmitting mode in the network have to be in the same CRC mode.

The RFW-D100 can apply CRC in three different ways:

- 16-Bit CRC – using polynomial  $1 + X^2 + X^{15} + X^{16}$
- 8-Bit CRC – using polynomial  $1 + X + X^2 + X^8$
- No CRC

This gives each application the flexibility to choose the adequate amount of overhead it adds to each packet and the corresponding level of protection that the CRC code has.

If CRC is enabled, then the RFW-D100 calculates the CRC of each incoming packet. **It does not put the received CRC value in the RX FIFO.** Rather, it puts the result of its calculation in the RX\_FIFO as the last byte of the packet:

0x55 – CRC was received correctly.

0xAA – CRC was received incorrectly.

The status bit SSR(0) stores the result of the last received packet.

### LOW FREQUENCY RC OSCILLATOR

The RFW-D100 includes a built-in low frequency RC oscillator that enables the full transceiver chipset to maintain a very low current consumption once the system enters into sleep mode operation.

This RC oscillator is used as a clock source for the

communication watchdog (WDT) in the RFW-D100. The RC oscillator is enabled/disabled by the SCR1(5) flag.

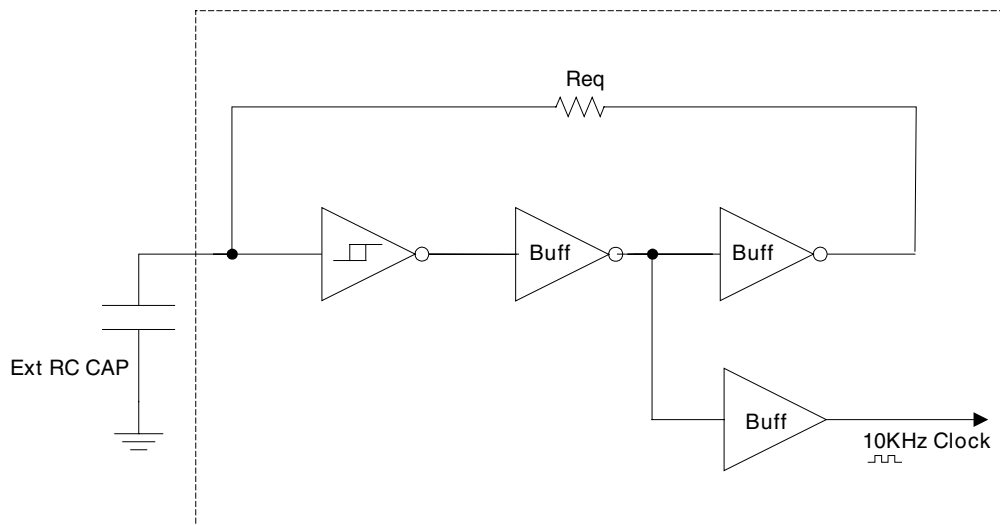


Figure 6. RC Oscillator Block Diagram

Operation Frequency: 10 KHz at  $C_{ext} = 30 \text{ pF}$   
 (Frequency is linear with  $C_{ext}$  value).  
 Operation current consumption:  $< 7 \mu\text{A}$   
 Frequency Deviation :  $\pm 20 \%$  over temperature.

### WDT

The WDT is used as a communication watchdog in the system. Its purpose is to wake up the MCU from power down or idle mode, whenever a packet is transmitted or a packet is received.

The watchdog timer (WDT) is a separate module inside the RFW-D100. A different oscillator from all the other modules in the RFW-D100 drives it. The watchdog clock source is an internal 10 kHz RC oscillator that uses an external capacitor to set its fre-

quency. The RC oscillator works only when SCR1(4) is set high.

Controlling the WDT is done through three registers (SCR1, FRC-H, FRC-L) and WDT\_RST input pin. When modifying one of these registers, WDT must be disabled (SCR1(3) – WDT\_EN = '0').

The WDT\_RST pin is used to reset the watchdog counter, i.e. set its value to 0. If the watchdog is enabled and WDT\_RST is set low, then the watchdog counter runs normally. When WDT\_RST is set high, the watchdog counter value is 0.

If WDT\_RST is set high while the WDT output pin is high, then the WDT pulse will be reset and the WDT output pin will be zero (as default).

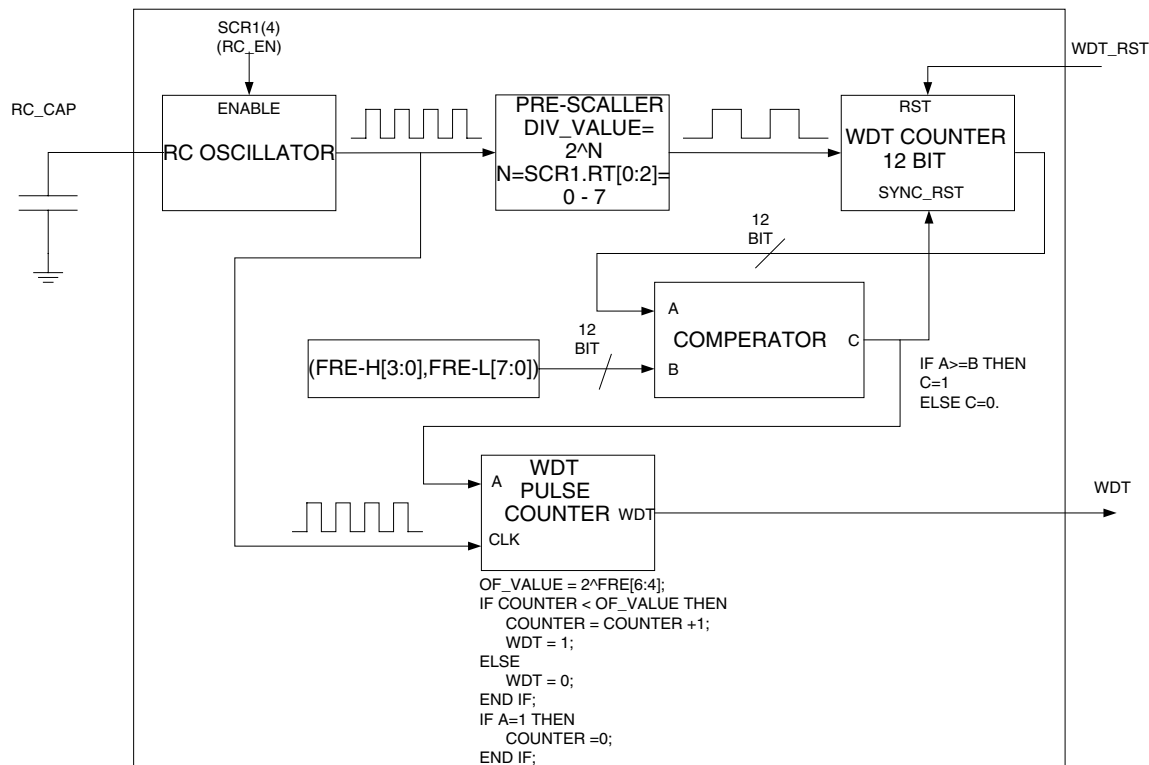


Figure 7. WDT and RC Oscillator System

RT[0:2] in SCR1 register determines the division value (DIV\_VALUE) of the RC oscillator input clock (see PRE-SCALLER in Figure 7). The clock output of the PRE-SCALLER module is CLK\_RC/DIV\_VALUE (CLK\_RC is the clock output of the RC oscillator). FRC-L and FRC-H (0-4) registers determine the overflow value of the WDT\_COUNTER. The WDT\_COUNTER counts (FRC-L(0:7) + FRC-H(0:3)\*28) \* DIV\_VALUE RC oscillator periods before reaching its overflow value. When overflow occurs, the WDT\_COUNTER is cleared and the RFW-D100 outputs a pulse through the WDT output pin.

The pulse duration from the WDT output pin is determined by FRC\_H(4:6) value. The pulse duration is  $2^{(FRC\_H(6-4))} * RC$  oscillator periods.

SCR1(3) enables/disables the WDT. When SCR1(3) is set high, the WDT is enabled otherwise, it is disabled. The WDT works when the RFW-D100 is in IDLE or POWER-DOWN mode, since a different clock drives it. The purpose of the WDT is to enable the MCU and the RFW-D100 to enter power-down or idle mode and then to wake them up at a predetermined time.

WDT operating sequence:

1. Disable WDT – SCR1(3) = '0'.

2. Enable RC oscillator – SCR1(4) = '1'.
3. Apply WDT\_RST.
4. Set registers (FRE-H, FRE-L, SCR1) values according to needed WDT pulse.
5. Enable WDT - SCR1(3) = '1'.

### RX FIFO

The purpose of having an input FIFO in the RFW-D100 is to reduce the real-time burden on the MCU. The FIFO is used as a buffer, which theoretically enables the MCU to read the incoming data every RX\_FIFO\_SIZE \* 8 bit/byte \* 1 μsec = 128 μsec, instead of every 1 μsec in the case of serial input or every 8 μsec in the case where there is a serial to parallel converter.

The actual buffer size for practical use is a bit smaller, since the MCU response time is taken into account. All received bytes are transferred to the RX\_FIFO. The RX\_FIFO stores the input data until the MCU reads the data from it. The RX\_FIFO size is 16 bytes. CRC and PREAMBLE bytes are not transferred to the RX\_FIFO.

The RX\_FIFO is accessed just like all other read-only registers in the RFW-D100. The MCU cannot write to



RX\_FIFO, it can only read from it.

The MCU has three ways of learning about the RX\_FIFO status:

- The RX\_FIFO Status Register (RFSR) – contains the number of bytes in the RX\_FIFO. Each incoming byte increment RFSR, and each read from RX\_BYTE by MCU decrement RFSR.
- RX\_FIFO Almost Full Interrupt (RX\_AF) – INT pin. If configured appropriately, the INT pin will be “1” each time RX\_FIFO is almost full. This invokes an MCU interrupt if the INT pin is connected to the MCU’s external interrupt pin.
- RX\_FIFO Overflow Interrupt – bit RX\_OF in IER indicates when an overflow event has occurred. If a received byte is written to a full RX\_FIFO, then the received byte is discarded and the RX\_OF interrupt is invoked. This interrupt tells the user that at least one byte has been lost from the currently received packet.

The RX\_AF interrupt should invoke the MCU to read from the RX\_FIFO. Using the almost full event gives the MCU 32  $\mu$ sec (4 bytes \* 8  $\mu$ sec) to respond before it loses data, assuming a bit rate of 1 Mbps. It uses most of the RX\_FIFO size, even if the response latency of the MCU is very short. Should the MCU not respond properly to the almost full event, and an input byte is written to the RX\_FIFO when it is full, then this byte will be discarded and will not be written to the RX\_FIFO.

The threshold that determines when RX\_AF interrupt is invoked is programmable. When SCR4(3) (FIFO\_FLAGS) is set to ‘0’, RX\_AF interrupt is invoked when RX\_FIFO contains 12 bytes. When SCR4(3) (FIFO\_FLAGS) is set to ‘1’, RX\_AF interrupt is invoked when RX\_FIFO contains 8 bytes. The last mode should be used with a slow MCU or long response time for interrupts.

LOCK\_OUT interrupt should also trigger the MCU to read from the RX\_FIFO. If a packet has ended and the RX\_AF interrupt was not invoked, the MCU should be triggered by the LOCK\_OUT interrupt.

When using NODE\_ID and/or NET\_ID filters, the data of a new incoming packet is not reachable for the MCU until NODE\_ID and/or NET\_ID has been identified correctly. RFSR is only updated after NODE\_ID and/or NET\_ID has been identified correctly. On the other hand, the internal RX\_FIFO counter is incremented with no regard to NET\_ID and NODE\_ID. This may cause an RX\_AF interrupt while RFSR is lower than 12 (when SCR4(3)=‘0’). In the worst case scenario, RX\_FIFO contains 7 bytes from previously received packets. The NODE\_ID is enabled and set to be the 5<sup>th</sup>

byte in each packet. In this case, the RX\_AF interrupt can be invoked when there are only 7 bytes in RX\_FIFO available for the MCU (RFSR=7).

### **TX\_FIFO**

The purpose of TX\_FIFO is to have an output buffer between the MCU and the serial output towards the RFW122. This reduces the real time burden of the MCU in a transmitting process. The TX\_FIFO enables the MCU, theoretically, to write to the TX\_FIFO every 128  $\mu$ sec instead of every 8  $\mu$ sec, as is the case with a regular 8-bit shift register.

The interface to the TX\_FIFO is similar to all the other write-only registers in the RFW-D100.

The MCU has three ways to learn about the TX\_FIFO status:

- TX\_FIFO Status Register (TFSR) – indicates the number of bytes in the TX\_FIFO.
- TX\_FIFO almost Empty Interrupt (TX\_AE) – when SCR4(3) equals ‘0’, the TX\_AE interrupt is invoked whenever the number of bytes in TX\_FIFO goes from 5 to 4 (when SCR4(3)=‘1’ it is from 9 to 8). The TX\_AE tells the MCU that it should reload the TX\_FIFO if it still has bytes from the current packet, since the RFW-D100 is about to finish transmitting the data in TX\_FIFO. It gives the MCU 32  $\mu$ sec to respond to reload the TX\_FIFO. For slow MCUs or when response time for interrupt is long, the interrupt threshold can be set to 8 bytes in TX\_FIFO (by SCR4(3)=‘1’). This gives the MCU up to 64  $\mu$ sec to respond to the TX\_AE.
- TX\_FIFO underflow flag (TX\_UF in SSR) – If the RFW-D100 tries to read from an empty TX\_FIFO, the RFW-D100 stops transmitting. The TX\_EMPTY interrupt is invoked and TX\_UF flag in SSR is set to ‘1’. TX\_UF flag indicates the transmission has ended abnormally, since the RFW-D100 has tried to read from an empty TX\_FIFO.

### **INTERRUPT DRIVER**

The INT output pin is the summation of all interrupt sources in the RFW-D100. Whenever an interrupt event has occurred and is enabled (IER), INT will go from low to high. INT will stay high until IIR register is read. IIR register contains all the interrupt events that have occurred since the last read. It shows the event only for enabled interrupts. If an interrupt is disabled, even if the event that invoked this interrupt has occurred, then the interrupt flag will be low. IER register is used to enable/disable each of the interrupt. SCR4(0) enables/disables all the interrupts.



The INT pin can be used to invoke MCU interrupts, if it is connected to the MCU's external interrupt pin.

There are 8 events in the RFW-D100 that can cause the INT pin to go from low to high:

1. **LOCK\_IN** – This interrupt indicates that the RFW-D100 has started receiving a new packet. The PREAMBLE has been identified. If the NET\_ID and/or the NODE\_ID are enabled, then they have been identified correctly. This event signals the beginning of an incoming packet.
2. **LOCK\_OUT** – This interrupt indicates that the RFW-D100 has finished receiving a full packet, including CRC. The RFW-D100 decides that it has reached the end of a packet according to the packet's size. If the RFW-D100 is in fixed packet size mode, then it has finished receiving PSR bytes, not including CRC bytes. If the RFW-D100 is not in fixed packet size mode, then it has finished receiving a packet size as indicated in the packet header. Although RX\_STOP and setting TX\_RX=1 (SCR2) terminate the receiving of the packet, they do not cause a LOCK\_OUT event, since the MCU is already aware of it (the MCU initiated it). The LOCK\_OUT interrupt tells the MCU when to get data out of the RX\_FIFO.
3. **LINK\_DIS** – This interrupt indicates that a “zero counter” capacitor discharge event has occurred. If a consecutive number of zero bits (according to SCR3(4:6)) have been received, this interrupt is set, even if zero count capacitor discharge is disabled (SCR3(3) – EN\_ZERO\_DIS = '0'). The actual capacitor discharge and its interrupt are two separate mechanisms that are both invoked by the same event, but are enabled/disabled in two separate registers (IER(2) for the interrupt and SCR3(3) for the discharge).
4. **RX\_OF** – This interrupt indicates that a byte from an incoming packet was discarded, since the RX\_FIFO was already full. The receiver module (see Figure 3) tried to write a byte to a full RX\_FIFO. The MCU should know that the corresponding packet is corrupted, since it is lacking at least one byte.
5. **TX\_EMPTY** – This interrupt indicates that the RFW-D100 has finished transmitting a packet normally or abnormally. Normal ending means that all the bytes of the packet including the CRC were transmitted. Abnormal ending means that either the RFW-D100 has been moved to RX mode in the middle of the packet by the MCU or the RFW-D100

has stopped transmitting since TX\_FIFO has been empty when it should not have been. In the last case, SRR(6) – TX\_UF is also set to one.

6. **RX\_FIFO\_AF** – This interrupt indicates that RX\_FIFO is almost full, i.e. the number of bytes in RX\_FIFO reached 12 if SCR4(3)='0' or 8 if SCR4(3)='1'. If the MCU does not want the RX\_FIFO to overflow, then it should empty it.
  7. **TX\_FIFO\_AE** – This interrupt indicates that TX\_FIFO is almost empty, i.e. the number of bytes in TX\_FIFO reached 4 if SCR4(3)='0' or 8 if SCR4(3)='1'. If the MCU did not finish putting the transmitted packet in the TX\_FIFO, then it should continue doing so now, otherwise an underflow event will occur.
- CS(Carrier Sense)**– This interrupt indicates that CS status line has gone from “1” to “0”. This signals the MCU that an identified or unidentified packet has ended. Identified packet means that a PREAMBLE has been identified. Unidentified packet means that a PREAMBLE has not been identified. If the MCU has a packet to transmit, and CS=“1” than the MCU waits for this event.

All these events can be masked. If an event is masked, then even if that event occurs, it does not set INT pin to be “1”. The masking is done by register IER.

The reason for masking is that in different applications or in different situations in the same application, these events have different priorities. The MCU decides which of these events will invoke an MCU interrupt.

### **PACKET SIZE**

There are two types of packet structure determined by PPR[5] (FIXED).

- **Fixed Sized Packet** – all packets have the same, fixed size. The packet size is determined in PSR register. The packet size can be 2 ⇔ 255 bytes.
- **Variable Sized Packet** – the header of the incoming packet determines the packet size. One of the header bytes contains the packet size. Bits SIZE\_LOC[0:1] in LCR register determines the location (offset) of packet size inside each incoming packet header. The RFW-D100 reads the packet size byte in the packet header according to LCR register.

In both cases, the packet size does not include the CRC addition or the PREAMBLE.

### **NET\_ID AND NODE\_ID FILTERS**

NET\_ID and NODE\_ID are two filters in the receiver. They filter incoming packets according to their network address and node address.



The address field in each incoming packet is compared to NET\_ID byte and NODE\_ID byte. If one of the above comparisons fails, then the packet is discarded and the MCU will not be aware of it.

NET\_ID and NODE\_ID are both one byte. Their values are stored in NIR and BIR registers accordingly. The byte to which they are compared is set by LCR register, i.e. their location in the packet header is determined in the LCR register.

**NET\_ID location in the packet header must always be before NODE\_ID location.**

Each of them can be enabled or disabled independently (PPR register).

NET\_ID is targeted to be a filter on the network address. It is supposed to be common for all nodes in the network.

NODE\_ID is targeted to be a filter on the specific node address. It is supposed to be unique to each node in the network.

The purpose of these filters is to save MCU power and to reduce its load. In a multi-node network, a node can filter all packets that are not sent to it, while in a multi-network environment, a node can filter packets from other RFWaves networks.

In certain networks, a multicast ability inside the network is required. Even if NODE\_ID filter is applied, addresses '111111XX' (where 'X' represents do not care) in NODE\_ID filter are preserved for multicast transmissions. NODE\_ID filter will not discard those 4 addresses in any case.

## **CARRIER SENSE**

Carrier sense protocols are protocols in which a node (station) listens to the common channel before it starts transmitting. The node tries to identify other transmissions in order to avoid collision that might block its own transmission. In a wider perspective, a network that applies carrier sense protocol utilizes the channel bandwidth more efficiently. A more efficient network enables lower power consumption to each node, shorter delay, and higher probability of reaching destination to each packet.

The RFW-D100 uses two complimentary techniques in order to achieve very robust carrier sense abilities. On the one hand, it has an internal comparator that gives it rough Radio Signal Strength Indicator (RSSI). The RSSI enables the RFW-D100 to identify any strong transmission that with good probability will block its transmission. On the other hand, it has an internal implementation of RFWaves Network Carrier Sense algorithm. The second case enables it to avoid collisions with other RFWaves stations on its network or from other networks in the area.

While the carrier sense status bits in SSR (CS and COMP\_IN) tell the MCU when not to transmit, the two interrupt CS and LINK\_DIS gives the MCU a flag when to transmit. LINK\_DIS will be invoked whenever any transmission has ended, while CS interrupt will be invoked only when an RFWaves transmission has ended. An application of course, can use some of the above mechanisms and not all of them - according to its needs.

A more comprehensive discussion on how to implement a CSMA protocol using the RFWaves chipset is given in the "CSMA Protocol for Wireless Keyboard and Mouse" document.

## **RSSI - RADIO SIGNAL STRENGTH INDICATOR (COMPARATOR)**

The purpose of the RSSI mechanism is to identify strong transmissions in the area of the RFW-D100.

In general, the RFW-D100, using an internal comparator, detects transmissions whose received power exceeds a certain threshold. An external resistor sets the threshold value. When a strong transmission is identified, there is no use in starting to transmit a new packet, since it is highly probable that it will be blocked.

SCR1(5) (COMP\_EN) enables/disables the use of the comparator/RSSI.

The comparator output is given in SSR(7) – COMP\_IN. A more detailed description is given in Appendix A – Radio Signal Strength Indicator (RSSI).

## **INTER/INTRA-RFWAVES NETWORKS CARRIER SENSE**

The RFW-D100 implements a carrier sense algorithm that identifies similar RFWaves networks. The algorithm uses the RFWaves special bit structure. This mechanism enables the MCU to avoid collisions with other nodes in its network or other networks in its area. Even if the RSSI did not identify other transmissions, it does not want to collide with other transmissions in the network, since the network efficiency will decrease. This will result in higher power consumption or even, in extreme cases, prevent the transfer of all requested packets.

The RFWaves network carrier sense mechanism helps the MCU in two ways:

- Detecting transmission of a node from its network, if it has started listening in the middle of the packet (a PREAMBLE or a NET\_ID will be recognized).
- Detecting transmission of a node from a similar network in the area (different PREAMBLE or NET\_ID).

**RFWAVES CARRIER SENSE ALGORITHM:**

Assuming our bit rate is 1 Mbps. According to the described bit structure (section 0 Bit Structure), the time difference between two raising edges on DATA\_IO must be an integer number of 1 μsec. If we take into account the frequency deviation between the two RFW-D100 oscillators, the time difference between two raising edges is 1 μsec ± Δ. The Δ depends on the frequency deviation between the two RFW-D100 oscillators. The RFW-D100 uses this quality in its carrier sense algorithm. If an N (N=(CSR(0:3) x 2) + 2) number of “1” bits, where each is preceded by at least one “0” bit, is received with time difference of an integer number of 1 μsec between two consecutive “1” bits, then CS flag in SSR equals ‘1’. Basically, the RFW-D100 counts “0” to “1” transits on DATA\_IO input, where the time difference between two transits

should be an integer number (≥ 2) of 1 μsec. The number of consecutive “1” bits that obey this rule is counted in the following example (Figure 8) in ONE\_CNT counter. ONE\_CNT is incremented only if a “1” bit that comes after a “0” bit is received, where the time gap between the “1” bit and the preceding “1” bit is as mentioned above. If the time difference between two consecutive “1” bits is out of the allowed deviation, then the ONE\_CNT is reset. ONE\_CNT is also reset if the number of consecutive “0” exceeds (CSR(4:7) x 2) + 2, where CSR is the Carrier Sense Register (see 0 Carrier Sense Register (CSR)). The number of consecutive “0” bits from the last “1” bit received is counted in ZERO\_CNT. ZERO\_CNT is reset each time “1” bit is received.

Both M and N values are determined in CSR register (CSR(7:4) and CSR(3:0) accordingly).

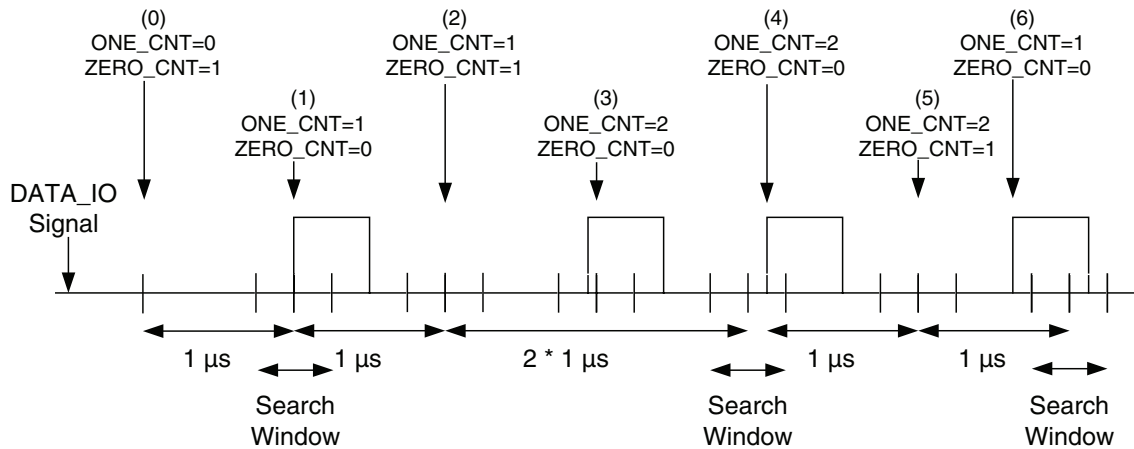


Figure 8. RFWaves Carrier Sense Example

In the example shown in Figure 8, at time (1) a new “1” bit is received after a “0” bit was received. Thus, CNT\_ONE equals 1 and ZERO\_CNT is reset to 0. At time (2), a “0” bit is received, so the ZERO\_CNT is incremented. At time (3), a “1” is received after a “0” bit was received. Thus ONE\_CNT is incremented and ZERO\_CNT is reset. At time (4) a “1” bit is received after a “1” bit, thus there is no change in any counter. At time (6) a “1” bit is received out of the allowed window, so ONE\_CNT is reset to 1. CSR register is used to configure the carrier sense algorithm sensitivity. CSR register determines the number of “1” bits that are required in order to decide that a carrier exists. CSR also determines the number of successive “0” bits that reset the carrier sense state machine. In SSR register, bit CS notifies whether a carrier was identified. Carrier sense can also be used as an interrupt. When CS in SSR goes from ‘1’ to ‘0’, i.e. the transmission has stopped and a CS interrupt is

invoked (if enabled in IER). The purpose of this interrupt is to inform the MCU that the channel is free again.

If the RFW-D100 identifies a packet, the carrier sense algorithm halts. When the RFW-D100 is in RX mode and LOCK flag in SSR is “0”, CS mechanism is working. When LOCK flag in SSR is “1”, CS mechanism is not working, since CS flag does not add any information because a PREAMBLE was identified, already. After a PREAMBLE is identified CS in SSR equals ‘1’.

**RECEIVER REFERENCE CAPACITOR DISCHARGE**

The RFW-D100 implements two independent mechanisms for receiver capacitor discharge:

- At the end of each received packet
- Zero counter



Mechanism 1 is enabled/disabled by bit EN\_CAP\_DISCH in SCR3.

Mechanism 2 is enabled/disabled by bit EN\_ZERO\_DISCH in SCR3.

The number of "0" bits that will cause a discharge in mechanism 2 is determined by bits ZERO\_DISCH\_CNT [0:2].

For both mechanisms, the discharge time is determined by CAP\_DIS\_PERIOD in SCR3(2). This should be set according to the used oscillator frequency so that the discharge duration will be ~ 3 μsec.

Discharge is done by setting RX\_TX pin to '1' for a certain time and then setting it back to '0'.

An interrupt LINK\_DIS is attached to the zero counter capacitor discharge mechanism. The interrupt and the actual discharge are two separate mechanisms. They are disabled and enabled separately. An interrupt can be invoked even if zero counter discharge is disabled (SCR3.EN\_ZERO\_DISCH = '0'). If the conditions for a zero counter discharge are reached, SCR3.EN\_ZERO\_DISCH = '0' and LINK\_DIS are enabled and LINK\_DIS will be invoked.

LINK\_DIS interrupt is used to synchronize the MCU about the end of an unidentified transmission on the channel, so the MCU can initiate a packet transmission.

(\*) More detailed explanations of the reference capacitor discharge algorithms and motivations can be found in the "RFW - Capacitor Discharge.pdf" document.

**CHANGING THE RFW-D100'S CONFIGURATION**

It is not recommended to change the RFW-D100 configuration while it is in the middle of receiving or transmitting a packet.

Thus, before writing to any of the RFW-D100 control registers (such as BLR, PRE-L, PRE-H, PPR, CSR etc):

1. Change TX\_RX mode to RX.
2. Disable PREAMBLE search (SEARCH\_EN in SCR2).
3. Stop all RX receiving – RX\_STOP.

It is then safe to change the RFW-D100's configuration.

**REGISTER DESCRIPTION**

All registers are read and write registers, except the status registers that are read only.

In case of a RST pulse, all registers are set to their default value.

**BIT LENGTH REGISTER (BLR)**

This register determines the length of the bit in terms of clock cycles.

The bit length is (BLR + 6) clocks, since the RFW-D100 adds the value 6 to the value in BLR.

The RFW-100's bit rate is:

Oscillator frequency/(BLR + 6).

Default Value: 00 (0 + 6 = 6).

**PREAMBLE LOW REGISTER (PRE-L)**

This register contains the 8 least significant bits of the PREAMBLE.

| Name  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| PRE-L | PR-7  | PR-6  | PR-5  | PR-4  | PR-3  | PR-2  | PR-1  | PR-0  |

**PREAMBLE HIGH REGISTER (PRE-H)**

This register contains the 8 least significant bits of the PREAMBLE.

| Name  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| PRE-H | PR-15 | PR-14 | PR-13 | PR-12 | PR-11 | PR-10 | PR-9  | PR-8  |

Default Value: 0 x FF.



**FREE RUN COUNTER – LOW (FRC-L)**

FRC is a wrap-around 12 bit counter incremented WDT\_CLK clock.

Whenever the counter reaches its overflow value (FRC-H(4-0), FRC-L), a pulse is generated in the WDT pin, according to FRC-H(4:6). This counter can implement a kind of watchdog timer for the MCU.

This register contains the 8 least significant bits of the 16 bits overflow value.

Default Value: 0 x FF.

**FREE RUN COUNTER – HIGH (FRC-H)**

FRC-H[3-0]:

FRC is a wrap-around 12 bit counter incremented WDT\_CLK clock.

Whenever the counter reaches its overflow value (FRC-H(3-0), FRC-L), a pulse is generated in the WDT pin. This counter can implement a kind of watchdog timer for the MCU.

Bit 0-3 in this register contains the 4 most significant bits of the 12-bits overflow value.

FRC-H[6-4]: pulse count

These bits determine the watchdog pulse width.

The pulse width is:  $2^{(FRC\_H(6-4))} \times RC$  oscillator periods.

It is important to emphasize that the clock source for the WDT pulse is the RC oscillator and not the pre-scaled clock.

Default Value: 0 x FF.

**PACKET PARAMETER REGISTER (PPR)**

| Name | Bit 7     | Bit 6      | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------|-----------|------------|-------|-------|-------|-------|-------|-------|
| PPR  | NET ID_EN | NODE ID_EN | FIXED | CRC1  | CRC0  | RB-2  | RB-1  | RB-0  |

This is a read/write register.

It contains control flags of the transmitted and received packet structure.

Default Value: 0 x 3A.

Bits 0-2: Refresh Bit - RB [2:0]

These bits determine the maximum number of successive “zero” bytes allowed before an added “one” bit is stuffed to the packet by the transmitter state machine. The reason for this feature is to keep the RFW122 reference capacitor charged, thus retaining the receiver’s sensitivity.

| Refresh Bit   | Bit 2 | Bit 1 | Bit 0 |
|---|-------|-------|-------|
| Refresh bit is added to every byte, no matter what its content. | 0     | 0     | 0     |
| Refresh bit is added if 1 byte equals x“00”.                    | 0     | 0     | 1     |
| Refresh bit is added if 2 successive bytes equal x“00”.         | 0     | 1     | 0     |
| Refresh bit is added if 3 successive bytes equal x“00”.         | 0     | 0     | 1     |
| Refresh bit is added if 4 successive bytes equal x“00”.         | 1     | 0     | 0     |
| Refresh bit is added if 5 successive bytes equal x“00”.         | 1     | 0     | 1     |
| Refresh bit is added if 6 successive bytes equal x“00”.         | 1     | 1     | 0     |
| Refresh bit is added if 7 successive bytes equal x“00”.         | 1     | 1     | 1     |

The value of the refresh bit is determined by the value of the reference capacitor.

Bit 4, 3: CRC [0:1]

These bits control the CRC operation for both transmit and receive mode:

| CRC    | Bit 4 | Bit 3 |
|--------|-------|-------|
| No CRC | 0     | 0     |
| CRC 8  | 0     | 1     |
| CRC 8  | 1     | 0     |
| CRC 16 | 1     | 1     |

Bit 5: FIXED

Controls the packet mode.

When FIXED bit is high, the RFW-D100 sends and receives packets with a fixed size/length that is specified in the **Packet Size Register (PSR)**.

When FIXED bit is low, the packet size is variable. The size is specified in the header of the incoming or outgoing packets. The location of the packet size field is specified in the **LCR** register.

Bit 6: NODE\_ID\_EN

This is NODE\_ID enable/disable bit.

When NODE\_ID\_EN is 1, NODE\_ID filter is enabled according to LCR, BIR.

When NODE\_ID\_EN is 0, NODE\_ID filter is disabled.



Bit 7: NET\_ID\_EN  
This is NET\_ID enable/disable bit.

When NET\_ID\_EN is 1, NET\_ID filter is enabled according to LCR, NIR.  
When NET\_ID\_EN is 0, NET\_ID filter is disabled.

**SYSTEM CONTROL REGISTER 1 (SCR1)**

| Name | Bit 7 | Bit 6 | Bit 5  | Bit 4 | Bit 3  | Bit 2 | Bit 1 | Bit 0 |
|------|-------|-------|--------|-------|--------|-------|-------|-------|
| SCR1 |       |       | CMP_EN | RC_EN | WDT_EN | RT2   | RT1   | RT0   |

This register is a general control register. It is a read/write register.

**Bits 0-2: RT [0:2]**

These bits determine the division rate (DIV\_VALUE) of the RC oscillator clock. The divided clock (RC oscillator/DIV\_VALUE) drives the WDT module (see WDT chapter).

The DIV\_VALUE, i.e. the division rate of watchdog external oscillator, is by powers of 2 (1,2,4,8,...,64,128).  
 $DIV\_VALUE = 2^{RT[0:2]}$ .

**Bit 3: WDT\_EN**

This is the watchdog (WDT) enable/disable control bit. When WDT is '1' – the WDT module is enabled. The WDT counter runs, and if it equals its overflow values it generates a pulse on the WDT output pin. When WDT is '0' – the WDT module is disabled.

The control registers SCR1(2:0) (RT(2:0)), FRC-L and FRC-H should be modified only when WDT\_EN is '0', i.e. the WDT is disabled.

**Bit 4: RC\_EN**

This bit controls the RC oscillator module. When RC\_EN is '1' – the RC oscillator is enabled. When RC\_EN is '0' – the RC oscillator is disabled.

Enabling the RC oscillator is a preliminary condition to work with the WDT.

**Bit 5: CMP\_EN**

This bit controls the analog comparator module (RSSI). When CMP\_EN is '1' – the comparator is enabled. When CMP\_EN is '0' – the comparator is disabled. Default Value: 0 x 00.

**SYSTEM CONTROL REGISTER 2 (SCR2)**

| Name | Bit 7      | Bit 6      | Bit 5      | Bit 4   | Bit 3         | Bit 2         | Bit 1     | Bit 0 |
|------|------------|------------|------------|---------|---------------|---------------|-----------|-------|
| SCR2 | PRE_MASK 2 | PRE_MASK 1 | PRE_MASK 0 | STOP_RX | TX_FIFO RESET | RX_FIFO RESET | SEARCH_EN | TX_RX |

This register controls the RFW-D100 operation modes. This register is a read/write register.

**Bit 0: TX\_RX**

Controls the transceiver mode: receive mode or transmit mode.

When TX\_RX is low – the RFW-D100 is in receive mode (default mode). The output pin TX\_RX is set to '0'. The RFW-D100 searches for a PREAMBLE. If PREAMBLE is found, it handles the process of receiving a packet.

There two cases in which SCR2(0) equals '0' but TX\_RX output pin is in TX mode ('1'):

1. If a SCR3(7) is set, then the RFW-D100 goes to RX mode and the output pin TX\_RX goes to TX mode.

2. The capacitor discharge can change the output pin TX\_RX to TX mode even if RFW-D100 are in RX mode. In this case, the output pin TX\_RX will be in TX mode for a short duration and then return to RX mode.

When TX\_RX is high – the RFW-D100 is in transmit mode. The output pin TX\_RX is set to '1'. The RFW-D100 handles the process of transmitting a packet according to the data in the TX\_FIFO. When it finishes transmitting the packet, it automatically goes back to receive mode. When RDW-D100 goes back to receive mode, SCR2(0) (TX\_RX) is '0' again.

**Bit 1: SEARCH\_EN**

Preamble search enable bit. When 1: Enables the search for PREAMBLE in receive mode. When 0: Disables the search for PREAMBLE in receive mode (used when user configures the

# RFW-D100



## Vishay RFWaves

RFW-D100 while in default receive mode). This bit's default value is '0'. It must be set to '1' in order to start receiving a packet. When modifying control registers in the RFW-D100, this register must be set to '0'. Changing the RFW-D100's configuration must be done when the RFW-D100 is in RX mode and no packet is being received and the search for a PREAMBLE is disabled.

### Bit 2: RX\_FIFO\_RESET

This bit resets the RX\_FIFO address pointers when set to logic 1. This bit is set by the MCU and is cleared automatically by the RFW-D100.

### Bit 3: TX\_FIFO\_RESET

This bit resets the TX\_FIFO address pointers when set to logic 1. This bit is set by the MCU and is cleared automatically by the RFW-D100.

### Bit 4: STOP\_RX

This bit stops receiving the current packet, resets the RX\_FIFO counters, and start new searches for PREAMBLE. This bit is set by the MCU and is cleared

automatically by the RFW-D100.

### Bits 5-7: PRE\_MASK [0:2]

These bits determine the mask on PRE-H in PREAMBLE correlation. Meaning, it determines the size of the PREAMBLE in the receiver. The PRE-L is always used in the PREAMBLE correlation. The RFW-D100 cuts off bit from PRE-H register, starting from the MSB.

| PRE_MASK 2 | PRE_MASK 1 | PRE_MASK 0 | PREAMBLE size |
|------------|------------|------------|---------------|
| 0          | 0          | 0          | 16            |
| 0          | 0          | 1          | 15            |
| 0          | 1          | 0          | 14            |
| 0          | 1          | 1          | 13            |
| 1          | 0          | 0          | 12            |
| 1          | 0          | 1          | 11            |
| 1          | 1          | 0          | 10            |
| 1          | 1          | 1          | 9             |

Default Value: 0 x 40

## SYSTEM CONTROL REGISTER 3 (SCR3)

This register is a read/write register.

| Name | Bit 7    | Bit 6           | Bit 5           | Bit 4           | Bit 3         | Bit 2          | Bit 1        | Bit 0 |
|------|----------|-----------------|-----------------|-----------------|---------------|----------------|--------------|-------|
| SCR3 | Not Used | ZERODISCH CNT 2 | ZERODISCH CNT 0 | ZERODISCH CNT 0 | EN ZERO DISCH | CAP DIS PERIOD | EN CAP DISCH |       |

### Bit 1: EN\_CAP\_DISCH

Enables/disables the capacitor discharge mechanism that discharges the reference capacitor after each received packet:

- 1: Enables discharge.
  - 0: Disables discharge.
- This bit overrides bit 3.

mechanism:

- 1: Enables zero counter capacitor discharge.
- 0: Disables zero counter capacitor discharge.

### Bit 2: CAP\_DIS\_PERIOD

Determines the capacitor discharge duration:  
 1: The pulse width is 72 clocks (3 μsec at 24 MHz clock).  
 0: The pulse width is 36 clocks (3 μsec at 12 MHz clock).  
 The recommended discharge period should be at least 3 μsec.  
 If the RFW-D100 oscillator frequency is bigger than 12 MHz

### Bits 4-6: ZERO\_DISCH\_CNT [0:2]

Determines the number of consecutive zero bits that will trigger a capacitor discharge by the zero counter capacitor discharge mechanism.

| ZERO DISCH CNT 2 | ZERO DISCH CNT 1 | ZERO DISCH CNT 0 | Number of Zeros |
|------------------|------------------|------------------|-----------------|
| 0                | 0                | 0                | 20              |
| 0                | 0                | 1                | 30              |
| 0                | 1                | 0                | 40              |
| 0                | 1                | 1                | 50              |
| 1                | 0                | 0                | 60              |
| 1                | 0                | 1                | 70              |
| 1                | 1                | 0                | 80              |
| 1                | 1                | 1                | 90              |

### Bit 3: EN\_ZERO\_DISCH

Enables/disables zero counter capacitor discharge

Bit 7: Not in Use



This bit must be 0 at all times for the RFW-D100 to work properly.  
Default Value: 0 x 01

**SYSTEM CONTROL REGISTER 4 (SCR4)**

This register is a read/write register.

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3      | Bit 2    | Bit 1     | Bit 0 |
|------|-------|-------|-------|-------|------------|----------|-----------|-------|
| SCR4 |       |       |       |       | FIFO FLAGS | WIN CONT | RF_ACTIVE | IE    |

**Bit 0: IE**

This flag enables all interrupts when set to '1'.  
When '0', all interrupts are disabled.

**Bit 1: RF\_ACTIVE**

This bit controls RF\_ACTIVE output pin.  
When this bit is high, the RF\_ACTIVE output pin is high.  
When this bit is low, the RF\_ACTIVE output pin is low.  
It controls the RFW122 ACT pin, enabling the RFW122 either to active mode or standby mode.

**Bit 2: WIN CONT**

Determines the size of the WINDOW in the PREAMBLE search module.  
If (BLR + 6) > 14 and WIN\_CONT=1, then the preamble window size is 5 samples.  
If (BLR + 6) < 14 or WIN\_CONT=0, then the preamble window size is 3 samples.

**Bit 3: FIFO FLAGS**

Determines the RX\_FIFO AF flags and the TX\_FIFO AE flag:  
If FIFO\_FLAGS=0, then AF=12 and AE=4.  
If FIFO\_FLAGS=1, then AF=8 and AE=8.  
RX\_AF interrupt is invoked when RFSR=AF (exceptions are described in the RX\_FIFO chapter).  
TX\_AE interrupt is invoked when RFSR=AE.  
Default Value: 0 x 00.

**Transmit FIFO Status Register (TFSR)**

This register is a read-only register.  
Contains the number of bytes in the TX\_FIFO.  
Default Value: 0 x 00 (TX\_FIFO empty).

**Receive FIFO Status Register (RFSR)**

This register is a read only register.  
Contains the number of bytes in the RX\_FIFO.  
Default Value: 0 x 00 (TR\_FIFO empty).

**Location Control Register (LCR)**

This is a read/write register.  
This register determines the location of fields NET\_ID, NODE\_ID, and PACKET\_SIZE in the packet structure.  
PPR[6] determines whether the packet size is fixed or variable.  
PPR[7] determines whether NODE\_ID is enabled/disabled.  
PPR[8] determines whether NET\_ID is enabled/disabled.  
If two or three of the following are enabled:  

- Variable packet size
- NET\_D filter enabled
- NODE\_ID filter enabled

then the following relative values must be kept:  
NET\_ID location < NODE\_ID location < Size Location.

| Name | Bit 7 | Bit 6      | Bit 5      | Bit 4      | Bit 3     | Bit 2     | Bit 1      | Bit 0      |
|------|-------|------------|------------|------------|-----------|-----------|------------|------------|
| LCR  |       | SIZE LOC 2 | SIZE LOC 1 | SIZE LOC 0 | NET LOC 1 | NET LOC 0 | NODE LOC 1 | NODE LOC 0 |

**Bits 0,1: NODE\_LOC [0:1]**

These bits determine the location of the NODE\_ID parameter in the header (the location is specified in bytes excluding preamble). The location should be fixed for all of the different kinds of packets transferred by the network.

NODE\_ID location in the packet header must always come after NET\_ID location.

| NODE_ID Location | NODE LOC 1 | NODE LOC 0 |
|------------------|------------|------------|
| 2                | 0          | 0          |
| 3                | 0          | 1          |
| 4                | 1          | 0          |
| 5                | 1          | 1          |

**Bits 2, 3: NET\_LOC [0:1]**

These bits determine the location of the NET\_ID parameter in the header (the location is specified in bytes excluding PREAMBLE). The location should be fixed for all the different kinds of packets transferred by the network.  
NET\_ID location in the packet header must always be before NODE\_ID location.



| NET_ID Location | NET LOC 1 | NET LOC 0 |
|-----------------|-----------|-----------|
| 1               | 0         | 0         |
| 2               | 0         | 1         |
| 3               | 1         | 0         |
| 4               | 1         | 1         |

Bits 4-6: SIZE\_LOC [0:2]

These bits determine the location of the packet size parameter in the header (the location is specified in bytes excluding preamble). The location should be fixed for all the different kinds of packets transferred by the network.

| Size Location | SIZE LOC 2 | SIZE LOC 1 | SIZE LOC 0 |
|---------------|------------|------------|------------|
| 2             | 0          | 0          | 0          |
| 3             | 0          | 0          | 1          |
| 4             | 0          | 1          | 0          |
| 5             | 0          | 1          | 1          |
| 6             | 1          | 0          | 0          |
| 7             | 1          | 0          | 1          |
| 8             | 1          | 1          | 0          |
| 9             | 1          | 1          | 1          |

If NET\_ID or NODE\_ID filters are enabled, then the packet's size location must always come after NET\_ID or NODE\_ID locations.

Default Value: 0 x 00

**Node Identity Register (BIR)**

This is a read/write register.

This register contains the NODE\_ID value.

When the receiver in the RFW-D100 builds the incoming packet, it compares the value in the BIR register to the received data at the location specified in LCR.

If the received NODE\_ID and the expected NODE\_ID are not equal, the packet is discarded.

Four multicast NODE\_ID addresses are implemented in RFW-D100. All received packets with NODE\_ID "111111XX", where 'X' represents do not care, will be accepted, regardless of the BIR value.

Default Value: 0 x 00

**Net Identity Register (NIR)**

This is a read/write register.

This register contains the NET\_ID value.

When the receiver in the RFW-D100 builds the incoming packet, it compares the value in the NIR to the received data at the location specified in LCR. If received NET\_ID and the expected NET\_ID are not equal, the packet is discarded.

Default Value: 0 x 00

**System Status Register (SSR)**

| Name | Bit 7   | Bit 6 | Bit 5     | Bit 4 | Bit 3 | Bit 2    | Bit 1     | Bit 0     |
|------|---------|-------|-----------|-------|-------|----------|-----------|-----------|
| SSR  | COMP_IN | TX_UF | BIT ERROR | LOCK  | CS    | TX EMPTY | LOCKED_IN | CRC ERROR |

This register is a read-only register.

This register provides status information to the MCU concerning the RFW-D100 status, incoming bits, and transmitted data. Bits 1, 2, 3 can trigger the interrupt if enabled in the IER. Bits 0, 5 and 6 are set by HW and cleared automatically after the MCU reads the register, since they reflect some error in the operation of the RFW-D100 and they are kept until the MCU knows about it. Bits 1 ↔ 4 and 7 are set and cleared by HW, since they reflect the current status of internal state-machine or the serial input.

**Bit 0: CRC\_ERROR**

This flag indicates a CRC Error in the packet. The CRC Block sets this flag at the end of a received packet, if the CRC calculation result is false. The RFW-D100 compares the calculated CRC and the received CRC. When these values differ, the flag goes high.

The flag is cleared only after the MCU reads the SSR register.

The CRC flag remains "1", if the MCU does not read the SSR register.

**Bit 1: LOCKED\_IN**

This flag indicates that a packet is being received.

Bit 1 is set to logic 1 whenever the RFW-D100 identifies a new incoming packet (triggers LOCK\_IN interrupt). After PREAMBLE, NET\_ID, and NODE\_ID have been identified, LOCKED\_IN flag goes high. If NODE\_ID and NET\_ID are disabled, PREAMBLE identification is sufficient. LOCKED\_IN flag goes low when the packet ends (triggers LOCK\_OUT interrupt).

**Bit 2: TX\_EMPTY**

This bit is the Transmitter Empty flag. When this bit is high, the RFW-D100 is available for loading the next



packet for transmission and the RFW-D100 is in receive mode. When the TX\_EMPTY flag is low, the RFW-D100 is in the middle of a packet transmission. When transmitting successive packets, the MCU should wait to the end of a packet before it reloads the TX\_FIFO with the next packet.

Bit 3: CS

Carrier Sense detection bit.

When this bit is high, the RFW-D100 has identified a structure of packet transmission in the air according to CSR. When low, no carrier has been detected. This bit is only valid in receive mode. The conditions for setting or clearing this flag are determined in the CS register. When LOCKED is high then CS is meaningless.

Bit 4: LOCK

Signals whether a PREAMBLE was identified.

When flag is "0" the receiver is searching for PREAMBLE.

When flag is "1" a PREAMBLE was identified. If a packet was discarded for any reason, LOCK flag goes low. If the packet has ended LOCK, goes low as well. This indicator is important because when a packet is ready for transmission, the indicator can determine if the line is busy and that in most cases the transmission will not succeed. If a PREAMBLE has been recognized but NET\_ID and NODE\_ID are still not compared, then the LOCK flag indicates that a packet is being received before the LOCK\_IN interrupt is invoked.

Bit 5: BIT\_ERROR

This flag indicates that there was some error in the received packet. The packet was not received according the expected timing specifications.

The packet can still pass CRC verification.

Bit 6: TX\_UF

This flag is set whenever the RFW-D100 reads a byte from an empty TX\_FIFO.

This flag indicates an abnormal end of packet transmission. The RDW-D100 transmitter's state machine has expected to find a valid byte in the TX\_FIFO according to the packet size, but it found an empty TX\_FIFO. When this event occurs, the TX\_EMPTY interrupt is invoked and the TX\_UF (under flow) flag is set to '1'.

This flag is set by hardware and cleaned by the MCU. It is cleaned whenever the MCU reads the SSR register.

Bit 7: COMP\_IN

This flag reflects the output of the COMPERATOR (for RSSI) module.

When CMP\_VIN > CMP\_VREF, then COMP\_IN equals '1'.

When CMP\_VIN < CMP\_VREF, then COMP\_IN equals '0'.

Default Value: 0 x 04.

Packet Size Register (PSR)

This is a read/write register.

This register determines the packet size in byte units, when working in fixed size packets [see PPR(5)]. The size is fixed for all received and transmitted packets.

The size in PSR excludes 2 bytes of PREAMBLE and 2, 1, or 0 bytes of CRC.

Default Value: 0 x 00.

Carrier Sense Register (CSR)

This is both a read and a write register.

This register configures the carrier sense mechanism in the RFW-D100.

| Name | Bit 7      | Bit 6      | Bit 5      | Bit 4      | Bit 3     | Bit 2     | Bit 1     | Bit 0     |
|------|------------|------------|------------|------------|-----------|-----------|-----------|-----------|
| CSR  | ZERO CNT.3 | ZERO CNT.2 | ZERO CNT.1 | ZERO CNT.0 | ONE CNT.3 | ONE CNT.2 | ONE CNT.1 | ONE CNT.0 |

Bits 0-3: ONE\_CNT [0:3]

This determines the number of successive "1" bits that set carrier sense high.

If (2\*ONE\_CNT[0:3] + 2) of '1' bits are received according to the carrier sense specifications, then CS flag in SSR is set high.

Bits 4-7: ZERO\_CNT [0:3]

The number of successive "0" bits that reset carrier sense (CS='0').

If (2\*ZERO\_CNT[0:3] + 2) of '0' bits are received successively, then CS flag in SSR is set low and

ONE\_CNT is reset.

YOU MUST NOT CHANGE THIS REGISTER WHILE THE RFW-D100'S PREAMBLE SEARCH IS ENABLED (SCR2(1) - 'SEARCH\_EN' MUST BE '0' while setting this register).

Default Value: 0 x 44



**INTERRUPT REGISTERS**

**Interrupt Enable Register (IER)**

This register is a read/write register.

This register determines whether each of the events mentioned below will cause an interrupt.

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4    | Bit 3 | Bit 2    | Bit 1    | Bit 0   |
|------|-------|-------|-------|----------|-------|----------|----------|---------|
| IER  | CS    | TX_AE | RX_AF | TX_EMPTY | RX_OF | LINK_DIS | LOCK_OUT | LOCK_IN |

For all flags in this register:

1 – Enable.

0 – Disable.

**Bit 0: LOCK\_IN**

This flag enables/disables the LOCK\_IN interrupt. PREAMBLE + NODE\_ID + NET\_ID identified correctly, triggers LOCK IN interrupt.

**Bit 1: LOCK\_OUT**

This flag enables/disables the LOCK\_OUT interrupt. Normal ending of received packet triggers LOCK\_OUT interrupt. Normal ending means that all the bytes of the packets were received.

**Bit 2: LINK\_DIS**

This flag enables/disables the LINK\_DIS interrupt. The zero counter capacitor discharge triggers the LINK\_DIS interrupt.

**Bit 3: RX\_OF**

This flag enables/disables the RX\_OF interrupt. End of received packet triggers RX\_OF interrupt.

**Bit 4: TX\_EMPTY**

This flag enables/disables the TX\_EMPTY (Transmitter Empty) interrupt. TX\_EMPTY interrupt tells the MCU that the transmitter has just finished transmitting a packet. The RFW-D100 goes to RX mode after finishing the transmission of a packet.

**Bit 5: RX\_AF**

This flag enables/disables the RX\_AF interrupt. The RX\_AF interrupt is triggered when the RX\_FIFO AF flag goes from '0' to '1'.

**Bit 6: TX\_AE**

This flag enables/disables the TX\_AE interrupt. The TX\_AE interrupt is triggered when the TX\_FIFO AE flag goes from '0' to '1'.

**Bit 7: CS**

This flag enables/disables the CS interrupt. A negative edge of CS flag in SSR triggers CS interrupt.  
Default Value: 0 x 00

**Interrupt Identification Register (IIR)**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4    | Bit 3 | Bit 2    | Bit 1    | Bit 0   |
|------|-------|-------|-------|----------|-------|----------|----------|---------|
| IIR  | CS    | TX_AE | RX_AF | TX_EMPTY | RX_OF | LINK_DIS | LOCK_OUT | LOCK_IN |

This is a read only register.

This register shows the enabled interrupt events that occurred, since the last time it was read. Each time the register is read, all the flags are cleared. This register is only cleared by global reset (RST) or by reading from it. Each time an interrupt occurs, its corresponding flag is set.

**Bit 0: LOCK\_IN**

This bit reflects the LOCK\_IN flag interrupt when enabled by IER.

LOCK\_IN interrupt is invoked whenever a PREAMBLE + NET\_ID + NODE\_ID is recognized.

If NET\_ID is disabled, then a received PREAMBLE + NODE\_ID invokes the interrupt.

If NODE\_ID is disabled, then a received PREAMBLE + NET\_ID invokes the interrupt.

If NET\_ID and NODE\_ID are disabled, then a received

PREAMBLE invokes the interrupt.

LOCK\_IN interrupt signals the MCU that a new packet is started to be received.

**Bit 1: LOCK\_OUT**

This bit reflects the LOCK\_OUT flag interrupt when enabled by IER.

LOCK\_OUT interrupt is invoked whenever the RFW-D100 has finished receiving a packet. The end of the packet is determined according to the packet size.

**Bit 2: LINK\_DIS**

This interrupt is invoked by the zero counter capacitor discharge mechanism.

The actual discharge mechanism can be disabled, but the interrupt can occur if it is enabled.

**Bit 3: RX\_OF**



This bit reflects the RX\_OF (over flow) flag interrupt when enabled by IER.

Bit 4: TX\_EMPTY

This bit reflects the TX\_EMPTY flag interrupt when enabled by IER.

Bit 5: RX\_AF

This bit reflects the RX\_FIFO AF (almost full) flag interrupt when enabled by IER.

Bit 6: TX\_AE

This bit reflects the TX\_FIFO AE (almost empty) flag interrupt when enabled by IER.

Bit 7: CS

This flag indicates that a carrier sense interrupt has occurred.

Whenever CS flag in SSR goes from “1” to “0”, a CS interrupt is invoked.

This interrupt tells the MCU that the current transmission on the shared channel has ended.

| MEMORY MAP       |         |         |                |
|------------------|---------|---------|----------------|
| Register Address | Write   | Read    | Default Values |
| 0 (00000)        | TX_FIFO | RX_FIFO | ---            |
| 1 (00001)        |         | PRE_L   | 0 x EB         |
| 2 (00010)        |         | PRE_H   | 0 x FF         |
| 3 (00011)        |         | FRC_L   | 0 x FF         |
| 4 (00100)        |         | FRC_H   | 0 x FF         |
| 5 (00101)        |         | SCR1    | 0 x 00         |
| 6 (00110)        |         | SCR2    | 0 x 40         |
| 7 (00111)        |         | SCR3    | 0 x 01         |
| 8 (01000)        |         | SCR4    | 0 x 00         |
| 9 (01001)        |         | LCR     | 0 x 00         |
| 10 (01010)       |         | BIR     | 0 x 00         |
| 11 (01011)       |         | NIR     | 0 x 00         |
| 12 (01100)       |         | PSR     | 0 x 00         |
| 13 (01101)       |         | PPR     | 0 x 3A         |
| 14 (01110)       |         | BLR     | 0 x 00         |
| 15 (01111)       |         | CSR     | 0 x 44         |
| 16 (10000)       |         | IER     | 0 x 00         |
| 17 (10001)       | ---     | IIR     | ---            |
| 18 (10010)       | ---     | SSR     | 0 x 04         |
| 19 (10011)       | ---     | TFR     | 0 x 00         |
| 20 (10100)       | ---     | RFR     | 0 x 00         |
| 21 (10101)       | ---     | ---     | ---            |

## DC ELECTRICAL CHARACTERISTICS

| ABSOLUTE MAXIMUM RATING |                                |                    |                                |       |
|-------------------------|--------------------------------|--------------------|--------------------------------|-------|
| Symbol                  | Parameter                      |                    | Rating                         | Units |
| T <sub>STG</sub>        | Storage temperature range      |                    | - 55 to 150                    | °C    |
| V <sub>CC</sub>         | Supply voltage relative to GND |                    | - 0.3 to 4.2                   | V     |
| V <sub>IN</sub>         | Input voltage relative to GND  |                    | - 0.3 to V <sub>CC</sub> + 0.3 | V     |
| V <sub>OUT</sub>        | Output voltage                 |                    | - 0.3 to V <sub>CC</sub> + 0.3 | V     |
| V <sub>ANALOG</sub>     | Analog pins                    |                    | - 0.3 to V <sub>CC</sub> + 0.3 | V     |
| T <sub>j</sub>          | Commercial Temperature         | Junction Operating | 0 to 115                       | °C    |

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



| RECOMMENDED OPERATING CONDITIONS |                                  |           |                |          |       |
|----------------------------------|----------------------------------|-----------|----------------|----------|-------|
| Symbol                           | Parameter                        | Min.      | Limits Typical | Max.     | Units |
| $V_{CC}$                         | Power supply                     | 3.0 (2.7) | 3.3            | 3.6      | V     |
| $V_{IN}$                         | Input voltage                    | 0         | -              | $V_{CC}$ | V     |
| $T_{OP}$                         | Operating temperature under bias | 0         |                | 70       | °C    |

| GENERAL DC CHARACTERISTICS |   |                             |              |                |              |       |
|----------------------------|---|-----------------------------|--------------|----------------|--------------|-------|
| Symbol                     | Parameter   | Conditions                  | Min.         | Limits Typical | Max.         | Units |
| $V_{IL}$                   | Input low voltage (Schmitt trigger negative going threshold)  |                             | 0.9          | 1.2            |              | V     |
| $V_{IH}$                   | Input high voltage (Schmitt trigger positive going threshold) |                             |              | 2.1            | 2.5          | V     |
| $V_{OL}$                   | Output voltage low  | 8 mA Output pin             |              |                | $V_{CC}-0.4$ | V     |
|                            |   | 2 mA Output buffer          |              |                | $V_{CC}-0.4$ |       |
| $V_{OH}$                   | Output voltage high   | 8 mA Output pin             | $V_{CC}-0.4$ |                |              | V     |
|                            |   | 2 mA Output buffer          | $V_{CC}-0.4$ |                |              |       |
| $I_{CCW}$                  | Power supply current in working mode                          | At 6 MHz working frequency  |              | 3              |              | mA    |
|                            |   | At 24 MHz working frequency |              | 7              |              | mA    |
| $I_{CCI}$                  | Power supply current in idle mode                             | At 6 MHz working frequency  |              | 0.45 (*)       |              | mA    |
|                            |   | At 24 MHz working frequency |              | 0.8 (*)        |              | mA    |
| $I_{CCP}$                  | Power supply current in power down mode                       |                             |              |                | 1 (*)        | μA    |
| $C_{IN}$                   | Input capacitance   |                             |              | 2.8            |              | pF    |
| $C_{OUT}$                  | Output capacitance  |                             | 2.7          |                | 4.9          | pF    |
| $C_{BID}$                  | Bi-directional buffer capacitance                             |                             | 2.7          |                | 4.9          | pF    |
| $I_{IL}$                   | Input leakage current (with no pull-up or pull-down)          |                             | -1           |                | 1            | μA    |
| $I_{OZ}$                   | Tri-state leakage current                                     |                             | -1           |                | 1            | μA    |

(\*) - All input pins are set according to internal pull-ups/downs.

**AC ELECTRICAL CHARACTERISTICS**

| READ CYCLE  |        |  |                        |                        |      |
|-------------|--------|--|------------------------|------------------------|------|
| Symbol      | Figure | Parameter                                | Min.                   | Max.                   | Unit |
| $1/t_{OSC}$ | 8      | Clock frequency at RFW-D100 input - CLK1 | DC                     | 24                     | MHz  |
| $t_{RDPW}$  | 8      | RD pulse width                           | $3 \cdot t_{OSC} + 10$ |                        | ns   |
| $t_{CSR D}$ | 8      | CS low to RD low                         | 0                      |                        | ns   |
| $t_{ADRD}$  | 8      | ADDRESS valid to RD low                  | 0                      |                        | ns   |
| $t_{RDDV}$  | 8      | RD low to DATA valid                     |                        | $3 \cdot t_{OSC} + 10$ | ns   |
| $t_{RHDT}$  | 8      | DATA float after RD                      |                        | $t_{OSC}$              | ns   |
| $t_{DHAR}$  | 8      | DATA hold after RD                       | 0                      |                        | ns   |
| $t_{RHDT}$  | 8      | Time between consecutive RD pulses       | $3 \cdot t_{OSC}$      |                        | ns   |
| $t_{RDAN}$  | 8      | ADDRESS valid after RD low               | $3 \cdot t_{OSC} + 10$ |                        | ns   |

The values were determined according to SDF simulations.

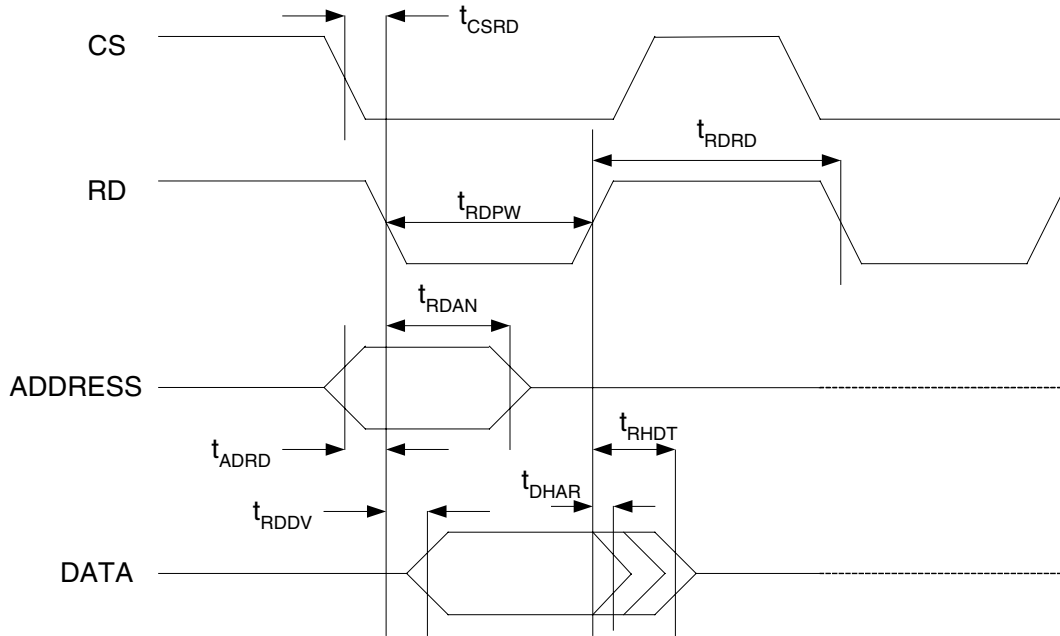


Figure 9. The RFW-D100 Read Cycle

| WRITE CYCLE |        |                                    |                        |      |      |
|-------------|--------|------------------------------------|------------------------|------|------|
| Symbol      | Figure | Parameter                          | Min.                   | Max. | Unit |
| $1/t_{OSC}$ | 9      | Oscillator frequency               | 0.1                    | 24   | MHz  |
| $t_{WRPW}$  | 9      | WR pulse width                     | $3 \cdot t_{OSC} + 10$ |      | ns   |
| $t_{CSWR}$  | 9      | CS low before WR low               | 0                      |      | ns   |
| $t_{ADWR}$  | 9      | ADDRESS valid before WR low        | 0                      |      | ns   |
| $t_{DVRD}$  | 9      | DATA valid before WR low           | 0                      |      | ns   |
| $t_{AVAW}$  | 9      | ADDRESS valid after WR low         | $3 \cdot t_{OSC} + 10$ |      | ns   |
| $t_{WRWR}$  | 9      | Time between consecutive WR pulses | $3 \cdot t_{OSC}$      |      | ns   |
| $t_{DVAW}$  | 9      | DATA valid after WR low            | $3 \cdot t_{OSC} + 10$ |      | ns   |

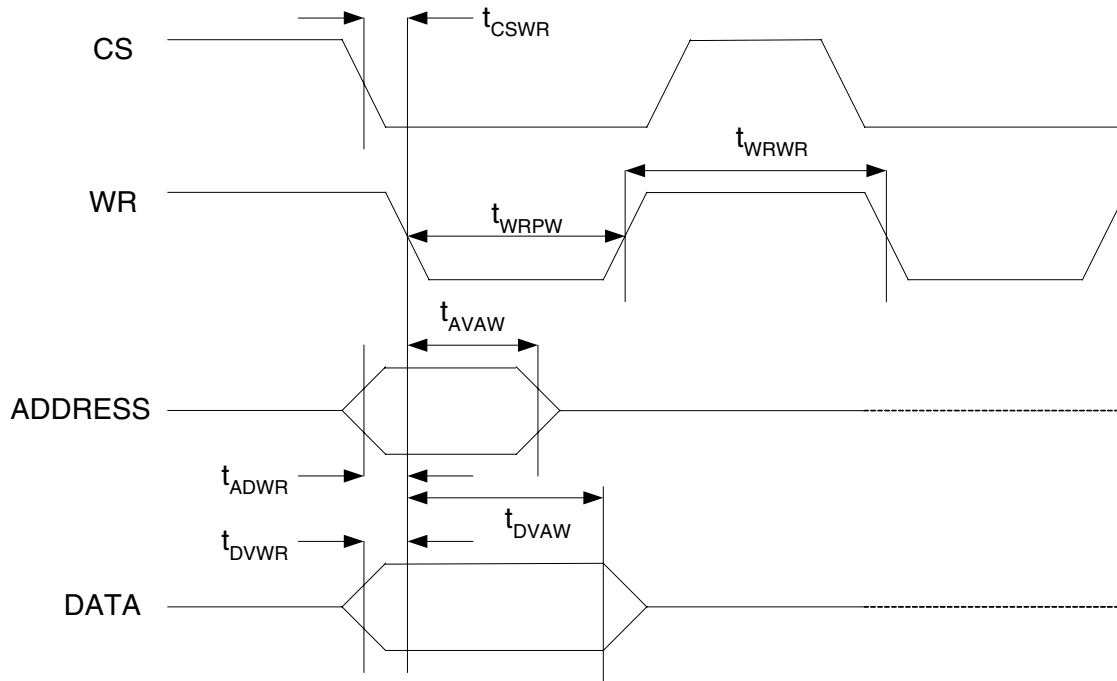
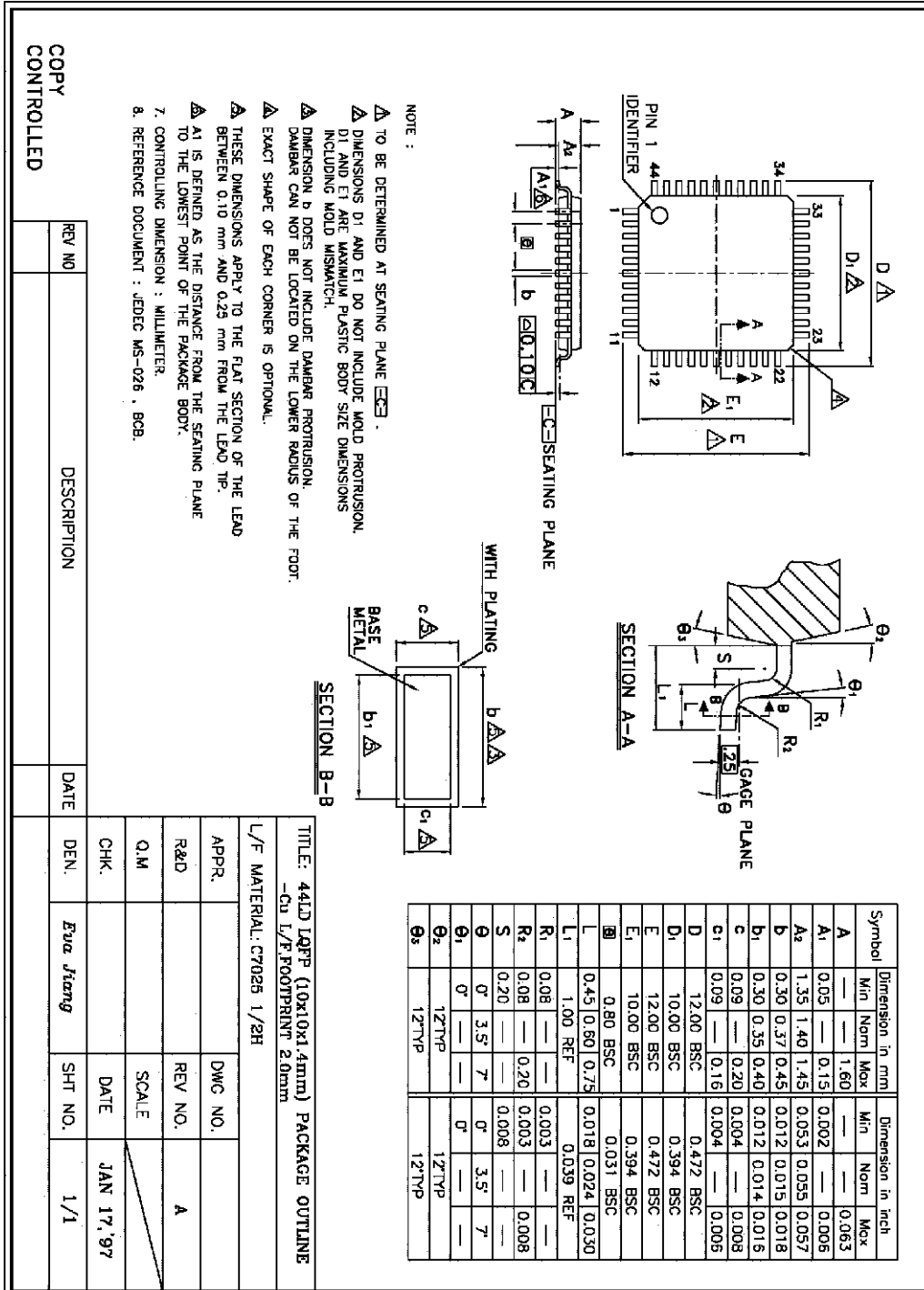


Figure 10. The RFW-D100 Write Cycle



**LQFR-44 PACKAGE DESCRIPTION**



COPY CONTROLLED

| REV NO | DESCRIPTION | DATE |
|--------|-------------|------|
|        |             |      |



**APPENDIX A - RADIO SIGNAL STRENGTH INDICATOR (RSSI)**

**General Description:**

The RFW-D100 includes a special built-in Analog module that supports Carrier detection. The principle of operation is rather simple. In order to maintain a ‘well-behaved’ protocol under a CSMA assumption, It would be highly efficient if each node could detect whether “the air is free” or not. This would mean that each node has the ability to find out prior to its own transmission, whether or not some other pre-executed transmissions are taking place simultaneously. Once this “competitive transmission” has been detected, the node just delays its own transmission until the current transmission terminates. This carrier sense or “traffic light” concept, reduces the probability of transmission collisions within the primary network and moreover, it avoids collisions that might occur with potential

intruder transmissions coming on from other networks that share the same space.

**Implementation:**

The RFW transceiver RSSI module comprises two main blocks. The front-end is a 20 MHz BW power meter, centered at 2.44 GHz, while the back end is a simple decision stage implemented as a voltage slicer. The front-end power meter is designed to produce a reference output voltage, which is correlated with the detected radio power at the specified BW and frequency. Figure 10 shows the power regulation of the power meter. Note that the output voltage keeps linearity over a wide range of input power (~ 75 dB) with a characteristic slope of 10 mV/dB. In order to maintain the high dynamic range that is required, a logarithmic peak detector is applied. It can be modeled as  $V_{out} = a * P_{in}$ , where  $P_{in}$  is in dBm (logarithmic), and  $V_{out}$  is in volts (linear).

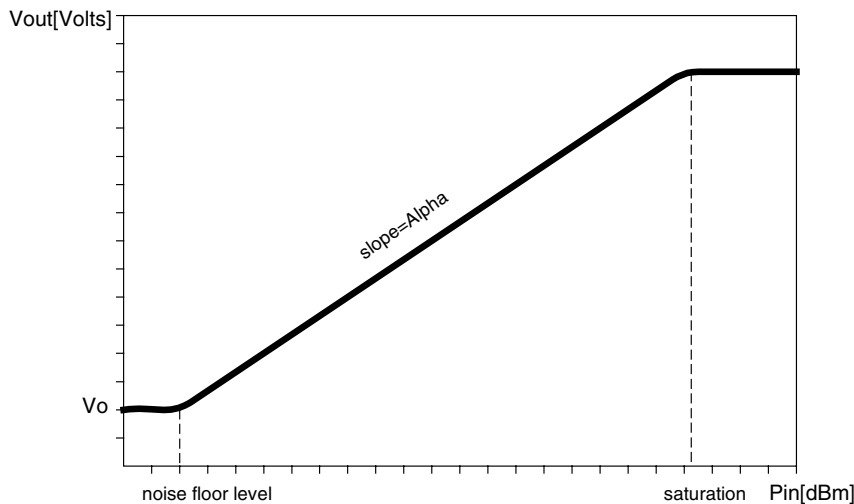


Figure 11. The RFW122 Peak detector  $V_{out}$  (PIN) Graph

At the back end, the peak detector power reference voltage is being compared to a pre-defined reference voltage. Once the detected power at the RFW transceiver occupied Bandwidth reaches the pre-defined threshold (Slicers reference voltage) the slicer comparator will change its output level from Low to High, as an indication of “powerful” transmission detection. Once the transmitted power level at the receiver port will go 5 dB below the power threshold (50 mV at the reference voltage), the slicer output will resume its low level, thus indicating “free air” condition. The following Figure is the complete RSSI block diagram.

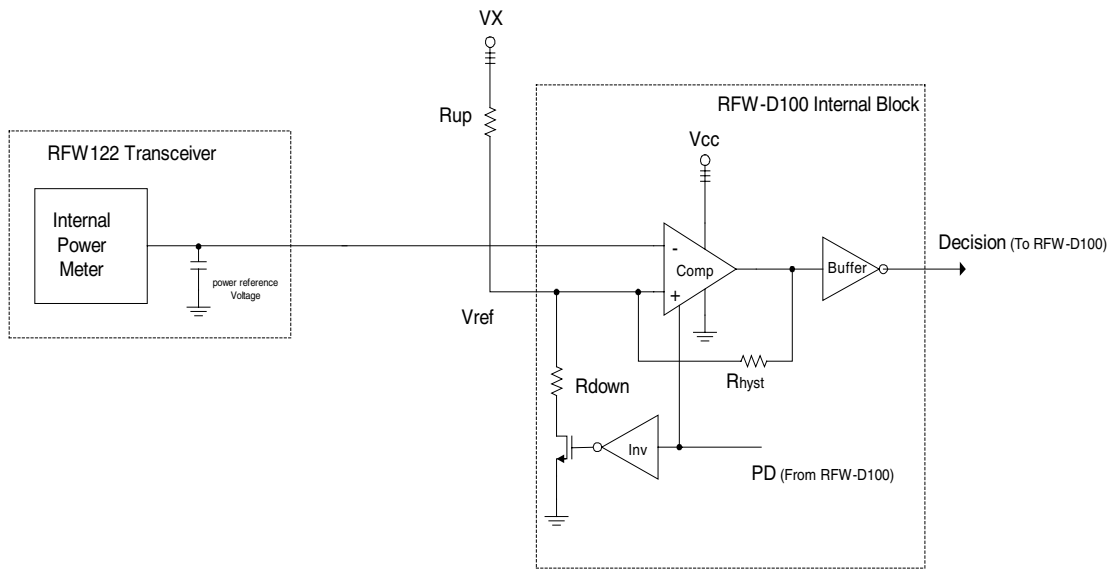


Figure 12. The RSSI Block Diagram

**Setting the power threshold:**

The reference power threshold can be easily controlled by simply changing the value of the external  $R_{up}$ . A simple resistor voltage divider is used for setting up the “reference power”. The internal  $R_{down}$  is about 30 k $\Omega$ , so the reference voltage can be approximated by :

$$V_{ref} = \frac{V_{CC}}{1 + R_{Up}/R_{Down}} = \frac{V_{CC}}{1 + R_{Up}/30\text{ k}\Omega}$$

As mentioned, the slicer includes an internal Hysteresis circuit that prevents the stage from bouncing around the reference voltage. The Hysteresis envelope is about 50 mV.

**Power down:**

By invoking the appropriate command, the MCU can shut down the slicer block and thereby maintain a very low quiescent current.

| SLICER TYPICAL CHARACTERISTIC |            |              |
|-------------------------------|------------|--------------|
| Parameter                     | Symbol     | Value        |
| Operating voltage             | $V_{CC}$   | 2.7 to 3.6   |
| Current consumption           | $I_C$      | 160 $\mu$ A  |
| Quiescent current             | $I_q$      | < 1 $\mu$ A  |
| Comparator bias current       | $I_b$      | < 1 nA       |
| Reference voltage             | $V_{ref}$  | 0.2 to 1.8 V |
| Hysteresis envelope           | $V_{hyst}$ | 50 mV        |



**APPENDIX B - RFWAVES PACKET STRUCTURE**

This section describes the recommended packet structure when using RFWaves hardware. The packet structure is closely tied with the RFW-D100.

|                        |                         |                     |                     |                       |                              |  |                              |
|------------------------|-------------------------|---------------------|---------------------|-----------------------|------------------------------|--|------------------------------|
| PREAMBLE –<br>2 octets | NETWORK –<br>4-2 octets | DST ID –<br>1 octet | SRC ID –<br>1 octet | SEQUENCE –<br>1 octet | SIZE – 1 octet<br>(optional) | PAYLOAD – determined<br>by SIZE (0-255 octets) | CRC –<br>2 octets (optional) |
|------------------------|-------------------------|---------------------|---------------------|-----------------------|------------------------------|--|------------------------------|

- **PREAMBLE-** The purpose of the PREAMBLE is to synchronize the receiver with the transmitter. The transmitted preamble is set to 16 bits. The correlation in the receiver RFW-D100 is actually done only on 8 ⇔ 16 bits. The first 0 to 8 transmitted bits are ignored in the receiver. Nevertheless, it is important to transmit all the 16 bits of preamble since it initializes the receiver.
- **NETWORK-** The RFWaves network field is recommended to be 16 ⇔ 32 bits. This determines the total number of RFWaves networks that can coexist without an address collision (6.5e4 ⇔ 4e9 networks). The RFW-D100 implements 8-bit network id filter, in order to filter packets sent by other networks. This should reduce the overhead on the MCU.
- **DST ID (8 bits) -** determines the destination of the packet.

Using 8 bits for DST ID means that each network will have at most 256 participants.

The location of the DST ID field is recommended to be constant in the packet header, since it enables the RFW-D100 to filter packets according to their DST ID. Few of the address are preserved in the RFW-D100 for multicast.

- **SRC ID (8 bits) –** determines who sent the packet.
- **SEQUENCE (8 bits)-** determines the sequence number of this packet. The sequence number is used to identify this specific packet in order to implement a reliable protocol (using ACKs and retransmissions).
- **SIZE (8 bits) –** determines the size of the packet in bytes units, excluding the preamble. The maximum size of a packet is 255 bytes.

This field should be set to a fixed position, since it is read by the RFW-D100 (the RFW-D100 is programmed to read a certain location).

This field is optional, since in some networks the packet size is fixed (the RFW-D100 can be programmed to receive only fixed sized packets).

- **PAYLOAD –** data for higher layers protocols and/or applications. The size of this field is the value of SIZE field minus all the overhead of the protocol (NETWORK, DST ID, SRC ID, SEQUENCE, SIZE, and CRC) excluding the PREAMBLE.

**CRC (16 bits) –** 16 is used for error detection. This function is implemented in the RFW-D100, which means there is no processing overhead on the MCU. The usage of the 16-CRC is optional. The RFW-D100 also supports 8-CRC (8 bits) for applications that are more sensitive to the overhead. The CRC can also be entirely removed.



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