HARRIS HD-6409/883

January 1992

CMOS Manchester Encoder-Decoder

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Converter or Repeater Mode**
- **Independent Manchester Encoder and Decoder Operation**
- **Static to One Megabit/sec Data Rate Guaranteed**
- **Low Bit Error Rate**
- **Digital PLL Clock Recovery**
- **On Chip Oscillator**
- **Low Operating Power: 50mW Typical at +5V**
- **Available in 20 Pin Dual-In-Line and 20 Pad LCC Package**

Description

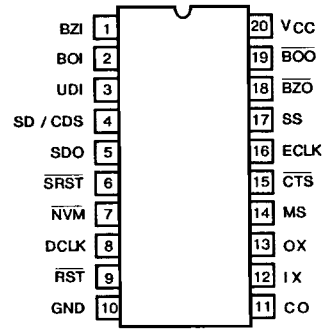
The HD-6409/883 Manchester Encoder-Decoder (MED) is a high speed, low power device manufactured using self-aligned silicon gate technology. The device is intended for use in serial data communication, and can be operated in either of two modes. In the converter mode, the MED converts Nonreturn-to-Zero code (NRZ) into Manchester code and decodes Manchester code into Nonreturn-to-Zero code. For serial data communication, Manchester code does not have some of the deficiencies inherent in Nonreturn-to-Zero code. For instance, use of the MED on a serial line eliminates DC components, provides clock recovery, and gives a relatively high degree of noise immunity. Because the MED converts the most commonly used code (NRZ) to Manchester code, the advantages of using Manchester code are easily realized in a serial data link.

In the Repeater mode, the MED accepts Manchester code input and reconstructs it with a recovered clock. This minimizes the effects of noise on a serial data link. A digital phase lock loop generates the recovered clock. A maximum data rate of 1MHz requires only 50mW of power.

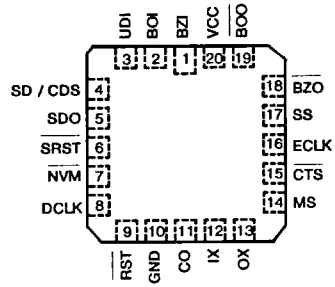
Manchester code is used in magnetic tape recording and in fiber optic communication, and generally is used where data accuracy is imperative. Because it frames blocks of data, the HD-6409/883 easily interfaces to protocol controllers.

Pinouts

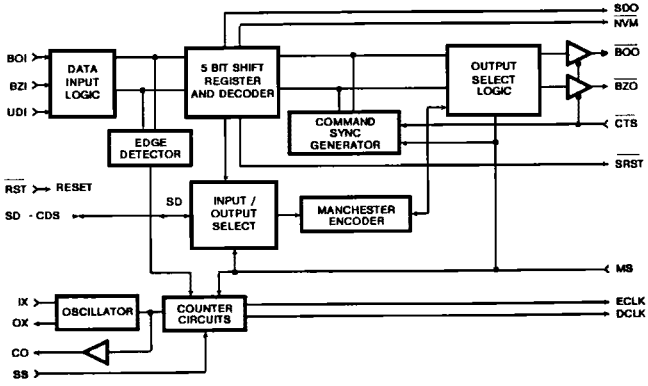
HD1-6409/883 (CERAMIC DIP)
TOP VIEW



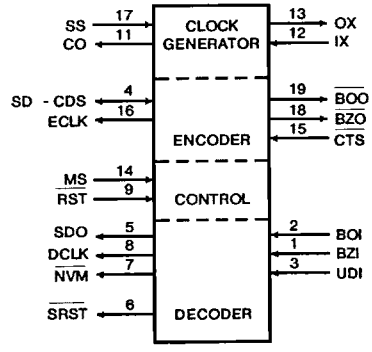
HD4-6409/883 (CERAMIC LCC)
TOP VIEW



Block Diagram



Logic Symbol



File Number **2959**

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	83°C/W	23°C/W
Ceramic LCC Package	84°C/W	24°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 602mW
Ceramic LCC Package 595mW
Gate Count ..... 250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Voltage Range ..... +4.5V to +5.5V
Input Rise and Fall Times ..... 50ns Max
Sync. Transition Span (t2) ..... 1.5 DBP Typical, (Notes 1, 2)
Short Data Transition Span (t4) ..... 0.5 DBP Typical, (Notes 1, 2)
Long Data Transition Span (t5) ..... 1.0 DBP Typical, (Notes 1, 2)
Zero Crossing Tolerance (tCD5) ..... (Note 3)

NOTES: 1. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.
2. The input conditions specified are nominal values, the actual input waveforms transition spans may vary by ± 2 I_X clock cycles (16X mode) or ± 6 I_X clock cycles (32X mode).
3. The maximum zero crossing tolerance is ± 2 I_X clock cycles (16X mode) or ± 6 I_X clock cycles (32 mode) from the nominal.

TABLE 1. HD-6409/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logic '1' Input Voltage	VIH	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	70% VCC	-	V
Logic '0' Input Voltage	VIL	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	20%VCC	V
Logic '1' Input Voltage ($\overline{Reset}$)	VIHR	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC -0.5	-	V
Logic '0' Input Voltage ($\overline{Reset}$)	VILR	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	GND +0.5	V
Logic '1' Input Voltage (Clock)	VIHC	VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC -0.5	-	V
Logic '0' Input Voltage (Clock)	VILC	VCC = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	GND +0.5	V
Input Leakage Current (Except I_X)	II	VIN = VCC or GND VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-1.0	+1.0	µA
Input Leakage Current (I_X)	II	VIN = VCC or GND VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-20	+20	µA
I/O Leakage Current	IO	VOUT = VCC or GND VCC = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10	+10	µA
Output HIGH Voltage (All except O_X)	VOH	IOH = -2.0mA VCC = 4.5V (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	VCC -0.4	-	V
Output LOW Voltage (All except O_X)	VOL	IOL = +2.0mA VCC = 4.5V (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Standby Power Supply Current	ICCSB	VIN = VCC or GND, VCC = 5.5V, Outputs Open	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	100	µA
Operating Power Supply Current	ICCOP	f = 16.0MHz, VIN = VCC or GND VCC = 5.5V, CL = 50pF	1, 2 ,3	$-55°C \leq T_A \leq +125°C$	-	18.0	mA
Functional Test	FT	(Note 2)	7, 8	$-55°C \leq T_A \leq +125°C$	-	-	-

NOTES: 1. Interchanging of force and sense conditions is permitted.
2. Tested as follows: f = 16MHz, VIH = 70% VCC, VIL = 20% VCC, VOH ≥ VCC/2, and VOL ≤ VCC/2, VCC = 4.5V and 5.5V.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. HD-6409/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Clock Frequency	f_C		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	16	MHz
Clock Period	t_C		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	$1/f_C$	-	sec
Bipolar Pulse Width	t_1		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	t_C+10	-	ns
One-Zero Overlap	t_3		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	t_C-10	ns
Clock High Time	t_{CH}	f=16.0MHz	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Clock Low Time	t_{CL}	f=16.0MHz	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Serial Data Setup Time	t_{CE1}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Serial Data Hold Time	t_{CE2}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	ns
DCLK to SDO, $\overline{NVM}$	t_{CD2}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
ECLK to $\overline{BZO}$	t_{R2}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns

NOTES: 1. AC Testing as follows: f = 4.0MHz, VIH = 70% VCC, VIL = 20% VCC, Speed Select = 16X, VOH $\geq$ VCC/2, VOL $\leq$ VCC/2, VCC = 4.5V and 5.5V, Input rise and fall times driven at 1ns/V, Output load = 50pF.

TABLE 3. HD-6409/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz All Measurements are referenced to device GND	1, 2	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CI/O		1, 2	$T_A = +25^oC$	-	12	pF
Output Rise Time (All except Clock)	t_r	From 1.0 to 3.5V CL = 50pF	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Output Fall Time (All except Clock)	t_f	From 3.5 to 1.0V CL = 50pF	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Clock Output Rise Time	t_r	From 1.0 to 3.5V CL = 20pF	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	11	ns
Clock Output Fall Time	t_f	From 3.5 to 1.0V CL = 20pF	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	11	ns
ECLK to $\overline{BZO}$, $\overline{BOO}$	t_{CE3}		1, 3	$-55^oC \leq T_A \leq +125^oC$	0.5	1.0	DBP
$\overline{CTS}$ Low to $\overline{BZO}$ $\overline{BOO}$ Enabled	t_{CE4}		1, 3	$-55^oC \leq T_A \leq +125^oC$	0.5	1.5	DBP
$\overline{CTS}$ Low to ECLK Enabled	t_{CE5}		1, 3	$-55^oC \leq T_A \leq +125^oC$	10.5	11.5	DBP
$\overline{CTS}$ High to ECLK Disabled	t_{CE6}		1, 3	$-55^oC \leq T_A \leq +125^oC$	-	1.0	DBP
$\overline{CTS}$ High to $\overline{BZO}$ $\overline{BOO}$ Disabled	t_{CE7}		1, 3	$-55^oC \leq T_A \leq +125^oC$	1.5	2.5	DBP
UDI to SDO, $\overline{NVM}$	t_{CD1}		1, 3	$-55^oC \leq T_A \leq +125^oC$	2.5	3.0	DBP
$\overline{RST}$ Low to DCLK, SDO, $\overline{NVM}$ Low	t_{CD3}		1, 3	$-55^oC \leq T_A \leq +125^oC$	0.5	1.5	DBP
$\overline{RST}$ High to DCLK, Enabled	t_{CD4}		1, 3	$-55^oC \leq T_A \leq +125^oC$	0.5	1.5	DBP
UDI to $\overline{BZO}$, $\overline{BOO}$	t_{R1}		1, 3	$-55^oC \leq T_A \leq +125^oC$	0.5	1.0	DBP
UDI to SDO, $\overline{NVM}$	t_{R3}		1, 3	$-55^oC \leq T_A \leq +125^oC$	2.5	3.0	DBP

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested.

2. Guaranteed via characteristics at initial device design and after major process and/or design changes.

3. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.

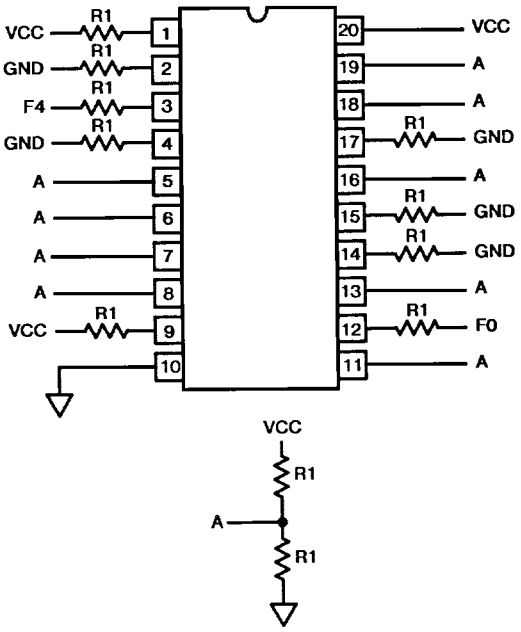
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

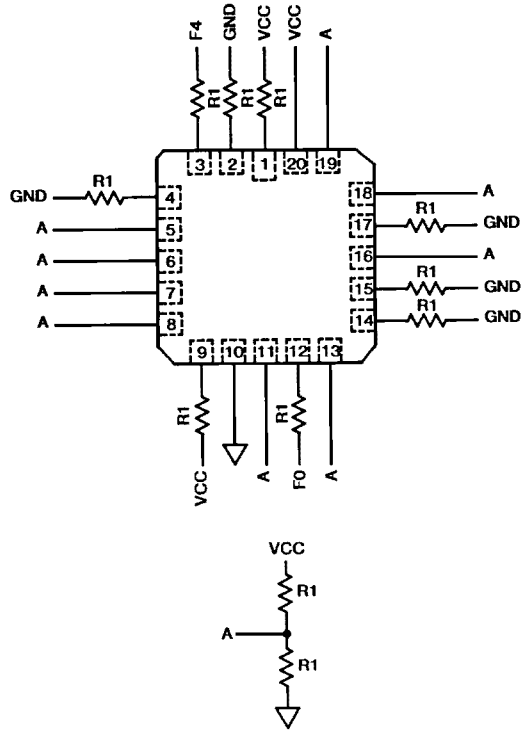
Burn-In Circuits

HD-6409/883 CERAMIC DIP



NOTES:
VCC = 5.5V ±0.5V
VIH = 4.5V ±10%
VIL = -0.2V to 0.4V
R1 = 47kΩ ±5%
F0 = 100kHz ±10%
F4 = F0/16

HD-6409/883 CERAMIC LCC



NOTES:
VCC = 5.5V ±0.5V
VIH = 4.5V ±10%
VIL = -0.2V to 0.4V
R1 = 47KΩ ±5%
F0 = 100kHz ±10%
F4 = F0/16

Metallization Topology

DIE DIMENSIONS:
88 x 78 x 19 ±1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: Metal 1: 8kÅ ± 1kÅ
Metal 2: 16kÅ ± 1kÅ

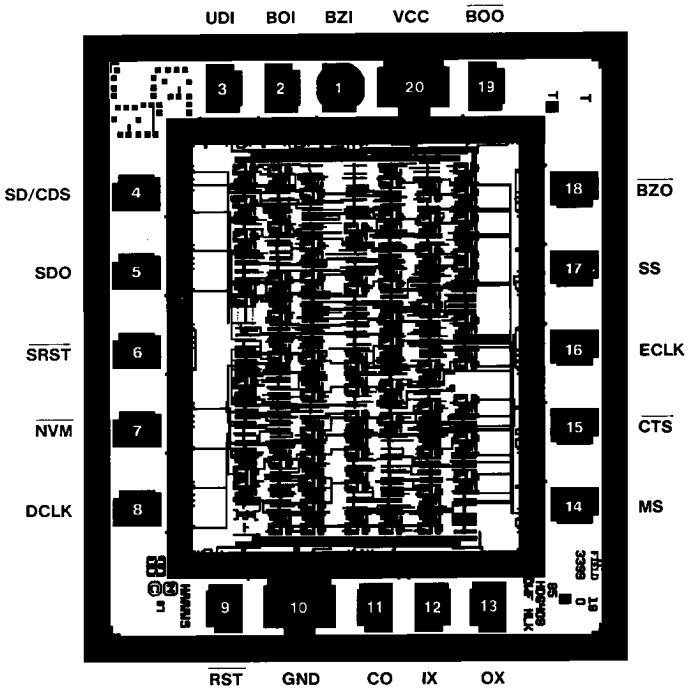
GLASSIVATION:
Type: Si_3N_4 • SiO_x
Thickness: 10kÅ ± 2kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
0.8×10^5 A/cm^2

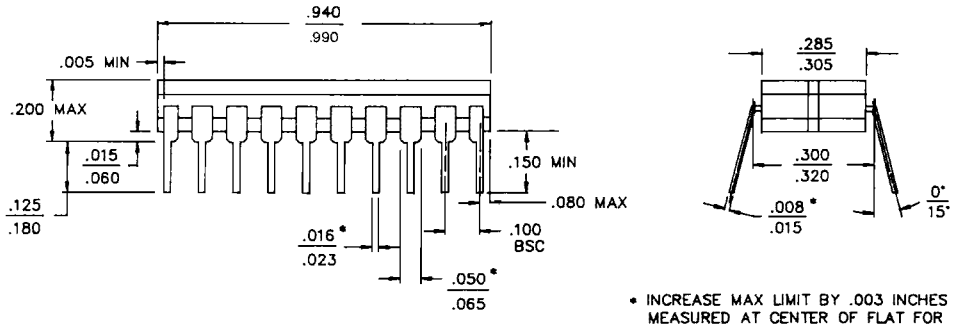
Metallization Mask Layout

HD-6409/883



Packaging

20 PIN CERAMIC DIP

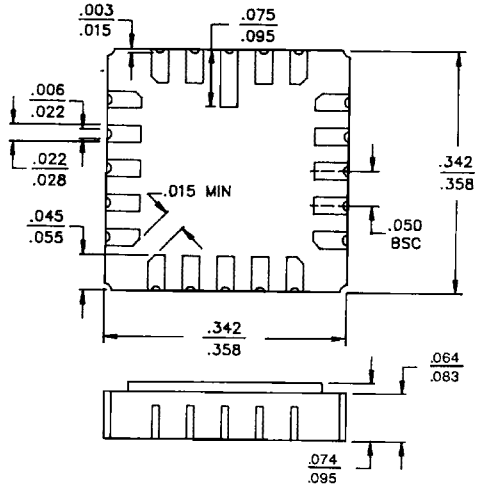


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD FINISH: Type A
MATERIALS: Compliant to MIL-M-38510

COMPLIANT OUTLINE: MIL-STD-1835, GDIP1-T20

20 PAD CERAMIC LCC



LEAD FINISH: Type A
MATERIALS: Compliant to MIL-M-38510

COMPLIANT OUTLINE: MIL-STD-1835, CQCC1-N20

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.