FEATURES

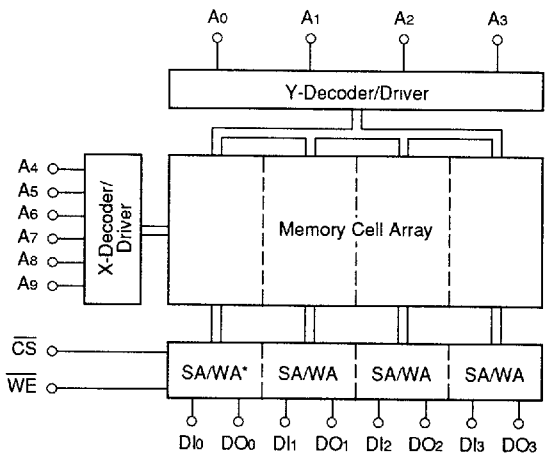
- **Address access time, t_{AA}: 2.5/3/4/5/7ns max.**
- **Chip select access time, t_{AC}: 2ns max.**
- **Write pulse width, t_{WW}: 3ns min.**
- **Edge rate, t_r/t_f: 500ps typ.**
- **Power supply current, I_{EE}: –300mA, -220mA for -5/7ns**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ I technology**
- **Fully compatible with industry standard 10K/100K ECL I/O levels**
- **Noise margins improved with on-chip voltage and temperature compensation**
- **Open emitter output for easy memory expansion**
- **Available in hermetic Dip, Flatpack and MLCC**
- **ESD protection of 2000V**

DESCRIPTION

The Synergy SY10/100/101474 are 4096-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 1024-words-by-4-bits and meet the standard 10K/100K family signal levels. The SY100474 is also supply voltage-compatible with 100K ECL, while the SY101474 operates from 10K ECL supply voltage (–5.2V). All feature on-chip voltage and temperature compensation for improved noise margin.

The SY10/100/101474 employ proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but also allow device operation with virtually no soft error sensitivity and with outstanding device reliability in volume production.

BLOCK DIAGRAM



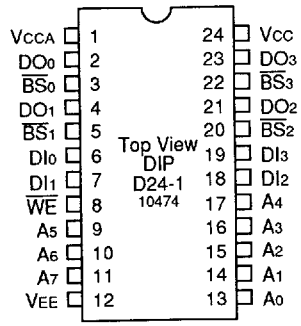
* SA = Sense Amplifier
WA = Write Amplifier

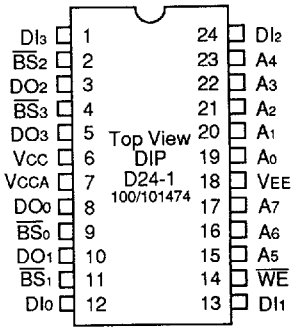
8

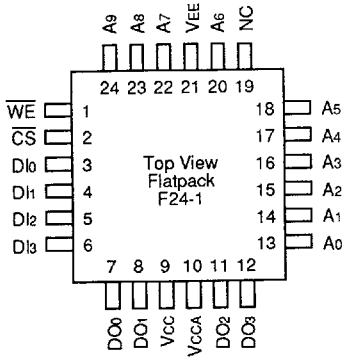
Rev.: B Amendment: /0
Issue Date April, 1994

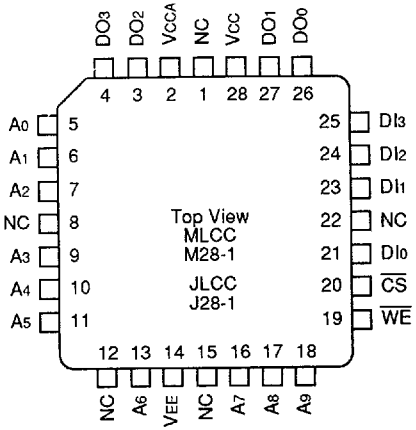
SYNERGY SEMICONDUCTOR

PIN CONFIGURATIONS









PIN NAMES

Label	Function
A0 - A9	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
DI0 - DI3	Data Input (DIN)
DO0 - DO3	Data Output (DOUT)
VCC	GND (0V)
VCCA	Output GND (0V)
VEE	Supply Voltage
NC	No Connect

TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	DOUT	Read

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Synergy SY10/100/101474 are 4096-bit RAMs organized as 1024-words-by-4-bits. Memory cell selection is achieved by using the 10 address bits designated as A_0 through A_9. Each of the 2^{10} possible input address combinations corresponds to a unique word location in memory. The active low Chip Select ($\overline{CS}$) is provided for memory expansion. The active low Write Enable ($\overline{WE}$) controls the read and write operation. Data resident on the D_{IN} inputs (D_{I0} through D_{I3}) is written into the addressed location only when $\overline{WE}$ and $\overline{CS}$ are held low. In order to perform a read operation, $\overline{WE}$ is held high, $\overline{CS}$ is held low and the non-inverted output data at the addressed location is transferred to D_{OUT} (DO_0 through DO_3) to be read out. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to –2.0V or an equivalent circuit must be used to provide the specified output levels.

The outputs are brought to a logical low level when the RAM is being written into ($\overline{WE}$ = LOW) or when the device is deselected via the active low chip select pin ($\overline{CS}$ = HIGH).

ABSOLUTE MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to V_{CC} Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
DC Output Current (Output High)	I_{OUT}	–30	mA
Temperature Under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{store}	–65 to +150	°C

NOTE:

1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (1)	10K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	75	°C
Supply Voltage(1)	100K	V_{EE}	–4.8	–4.5	–4.2	V
Case Temperature		T_C	0	—	85	°C
Supply Voltage(1)	101K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	85	°C

NOTE:

1 Referenced to V_{CC}

RISE AND FALL TIME

Parameter	Code(1)	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	F	tr	—	500	—	ps
Output Fall Time	F	tf	—	500	—	ps

NOTE:

1 F = Fast Edge Rate
S = Standard Edge Rate

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	5	—	pF

8

SYNERGY SEMICONDUCTOR

10K DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V; Tc = 0°C to +75°C; V_{EE} = –5.2V; Airflow > 2.5m/s; Output Load = 50Ω to –2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	0°C +25°C +75°C	–1000 –960 –900	–840 –810 –720	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1665 –1650 –1625	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	0°C +25°C +75°C	–1020 –980 –920	— — —	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	0°C +25°C +75°C	— — —	–1645 –1630 –1605	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	0°C +25°C +75°C	–1145 –1105 –1045	–840 –810 –720	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1490 –1475 –1450	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0°C to +75°C	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	0°C to +75°C	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	0°C to +75°C	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	0°C to +75°C	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	0°C to +75°C	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0°C to +75°C	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply -2.5ns, -3ns, -4ns Current -5ns, -7ns	0°C to +75°C	–300 –220	— —	mA	All Inputs and Outputs Open

100K/101K DC ELECTRICAL CHARACTERISTICS

V_{CCA} = 0V V_{EE} = –4.5V (100K) Tc = 0°C to +85°C Airflow > 2.5m/s
V_{CC} = 0V V_{EE} = –5.2V (101K) Output Load = 50Ω to –2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	–1025	–880	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	–1810	–1620	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	–1035	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	—	–1610	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	–1165	–880	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	–1810	–1475	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply -2.5ns, -3ns, -4ns Current -5ns, -7ns	–300 –220	— —	mA	All Inputs and Outputs Open

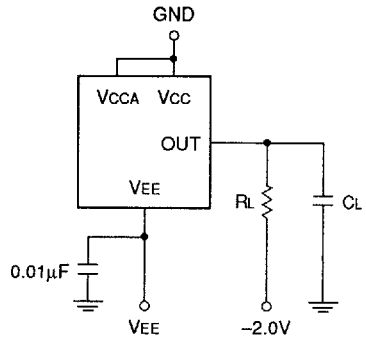
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

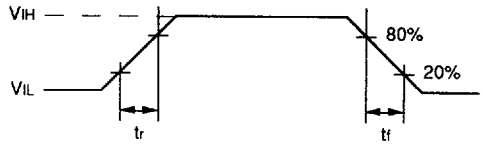
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to −2.0V
$V_{EE} = -5.2V \pm 5\%$(10K) T_C = 0°C to +75°C (10K)
$V_{EE} = -4.5V \pm 0.3V$(100K) T_C = 0°C to +85°C (100K/101K)
$V_{EE} = -5.2V \pm 5\%$(101K) Airflow > 2.5m/s

	T_C	V_{IH}	V_{IL}
10K	0°C	−0.933V	−1.733V
	+25°C	−0.90V	−1.70V
	+75°C	−0.863V	−1.663V
100/101K	0°C to +85°C	−0.90V	−1.70V

Loading Condition



Input Pulse



tr = tf = 1 0ns typ
OUTPUT LOAD R_L = 50Ω
C_L = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to −2V.)

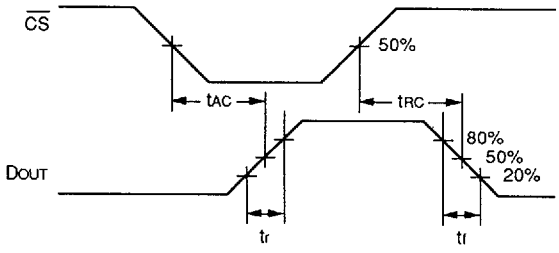
NOTE: All timing measurements referenced to 50% input levels

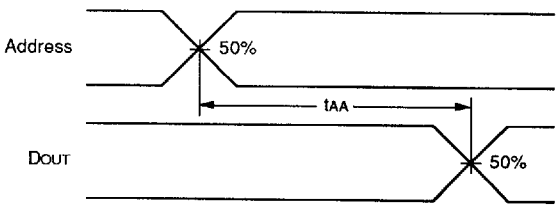
READ CYCLE

Symbol		Parameter	SY10474-2.5 SY100474-2.5 SY101474-2.5		SY10474-3 SY100474-3 SY101474-3		SY10474-4 SY100474-4 SY101474-4		SY10474-5 SY100474-5 SY101474-5		SY10474-7 SY100474-7 SY101474-7		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tAA	TAVQV	Address Access Time	—	2.5	—	3	—	4	—	5	—	7	ns
tAC	TSLQV	Chip Select Access Time	—	2	—	2	—	2	—	3	—	3	ns
tRC	TSHQL	Chip Select Recovery Time	—	2	—	2	—	2	—	3	—	3	ns

8

READ CYCLE TIMING DIAGRAM



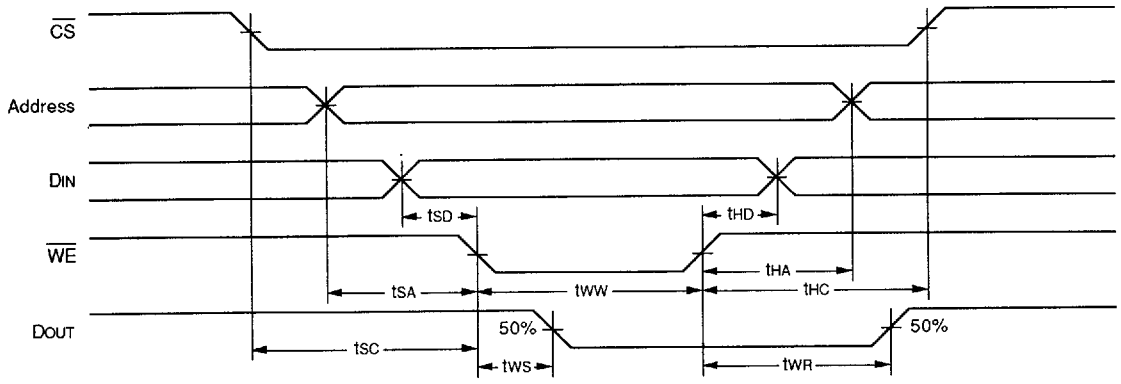


SYNERGY SEMICONDUCTOR

WRITE CYCLE

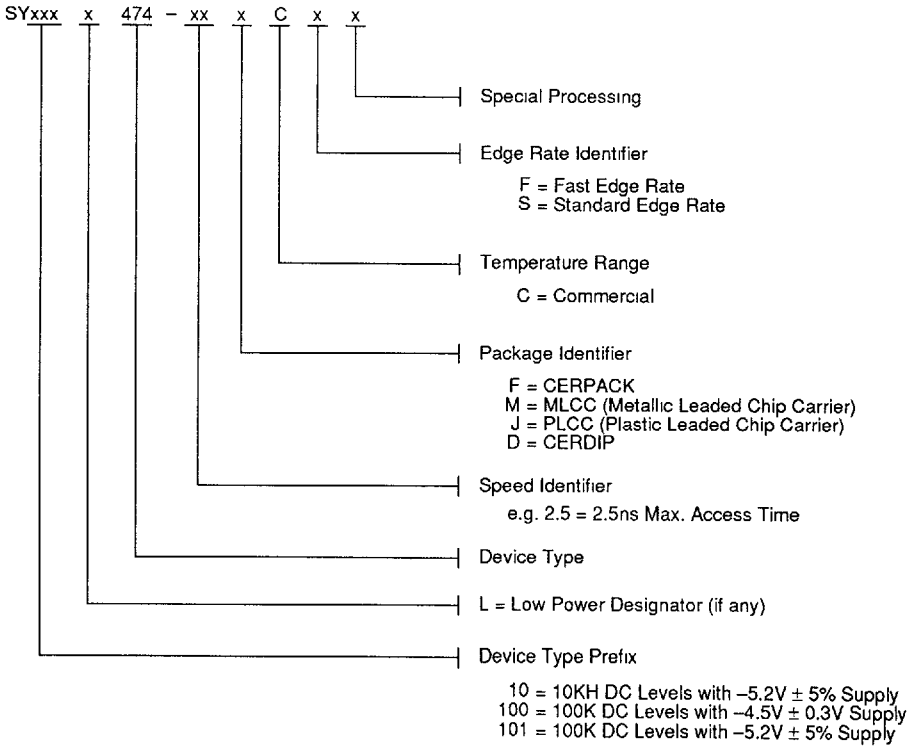
Symbol		Parameter	SY10474-2.5 SY100474-2.5 SY101474-2.5		SY10474-3 SY100474-3 SY101474-3		SY10474-4 SY100474-4 SY101474-4		SY10474-5 SY100474-5 SY101474-5		SY10474-7 SY100474-7 SY101474-7		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tWW	TWLWH	Write Pulse Width	3	—	3	—	4	—	3.5	—	5	—	ns
tWS	TWLQL	Write Disable Time	—	2.5	—	3	—	4	—	3.5	—	4	ns
tWR	TWHQV	Write Recovery Time	—	2.5	—	3	—	4	—	3.5	—	4	ns
tSA	TAVWL	Address Set-up Time	1	—	1	—	1	—	0.5	—	1	—	ns
tSC	TSLWL	Chip Select Set-up Time	0	—	0	—	0	—	0.5	—	1	—	ns
tSD	TDVWL	Data Set-up Time	0	—	0	—	0	—	0.5	—	1	—	ns
tHA	TWHAX	Address Hold Time	1	—	1	—	1	—	1.0	—	1	—	ns
tHC	TWHSX	Chip Select Hold Time	1	—	1	—	1	—	1.0	—	1	—	ns
tHD	TWHDX	Data Hold Time	1	—	1	—	1	—	1.0	—	1	—	ns

WRITE CYCLE TIMING DIAGRAM



PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
2.5	SY10/100/101474-2.5FCF	Fast	F24-1	Commercial
	SY10/100/101474-2.5MCF	Fast	M28-1	Commercial
3	SY10/100/101474-3FCF	Fast	F24-1	Commercial
	SY10/100/101474-3MCF	Fast	M28-1	Commercial
4	SY10/100/101474-4FCF	Fast	F24-1	Commercial
	SY10/100/101474-4MCF	Fast	M28-1	Commercial
5	SY10/100/101474-5FCS	Standard	F24-1	Commercial
	SY10/100/101474-5JCS	Standard	J28-1	Commercial
	SY10/100/101474-5DCS	Standard	D28-1	Commercial
7	SY10/100/101474-7FCS	Standard	F24-1	Commercial
	SY10/100/101474-7JCS	Standard	J28-1	Commercial
	SY10/100/101474-7DCS	Standard	D28-1	Commercial



8