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# HB56UW272EJN Series, HB56UW264EJN Series

HB56UW272EJN  
16 MB Unbuffered EDO DRAM DIMM  
2-Mword  $\times$  72-bit, 2 k Refresh, 1-Bank Module  
(9 pcs of 2 M  $\times$  8 Components)

HB56UW264EJN  
16 MB Unbuffered EDO DRAM DIMM  
2-Mword  $\times$  64-bit, 2 k Refresh, 1-Bank Module  
(8 pcs of 2 M  $\times$  8 Components)

# HITACHI

ADE-203-717C (Z)  
Rev.3.0  
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## Description

The HB56UW272EJN, HB56UW264EJN belong to 8 Byte DIMM (Dual In-line Memory Module) family, and have been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56UW272EJN is a 2M  $\times$  72 dynamic RAM module, mounted 9 pieces of 16-Mbit DRAM (HM51W17805) sealed in SOJ package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56UW264EJN is a 2M  $\times$  64 dynamic RAM module, mounted 8 pieces of 16-Mbit DRAM (HM51W17805) sealed in SOJ package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56UW272EJN, HB56UW264EJN offer Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56UW272EJN, HB56UW264EJN is 168-pin socket type package (dual lead out). Therefore, the HB56UW272EJN, HB56UW264EJN make high density mounting possible without surface mount technology. The HB56UW272EJN, HB56UW264EJN provide common data inputs and outputs. Decoupling capacitors are mounted on the module board.

## Features

- 168-pin socket type package (Dual lead out)
  - Outline: 133.35 mm (Length)  $\times$  25.40 mm (Height)  $\times$  5.28 mm (Thickness)
  - Lead pitch: 1.27 mm
- Single 3.3 V ( $\pm$ 0.3 V) supply

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## HB56UW272EJN Series, HB56UW264EJN Series

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- High speed
  - Access time :  $t_{RAC} = 50/60/70\text{ns}$  (max)  
:  $t_{CAC} = 13/15/18\text{ns}$  (max)
- Low power dissipation
  - Active mode : 3.56/3.24/2.92 W (max) (HB56UW272EJN Series)  
: 3.17/2.88/2.59 W (max) (HB56UW264EJN Series)
  - Standby mode (TTL): 64.8 mW (max) (HB56UW272EJN Series)  
(TTL): 57.6 mW (max) (HB56UW264EJN Series)  
(CMOS): 4.86 mW (max) (L-version) (HB56UW272EJN Series)  
(CMOS): 4.32 mW (max) (L-version) (HB56UW264EJN Series)
- JEDEC standard outline unbuffered 8-byte DIMM
- EDO page mode capability
- Refresh period
  - 2048 refresh cycles : 32 ms  
: 128 ms (L-version)
- 4 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
  - Self refresh (L-version)

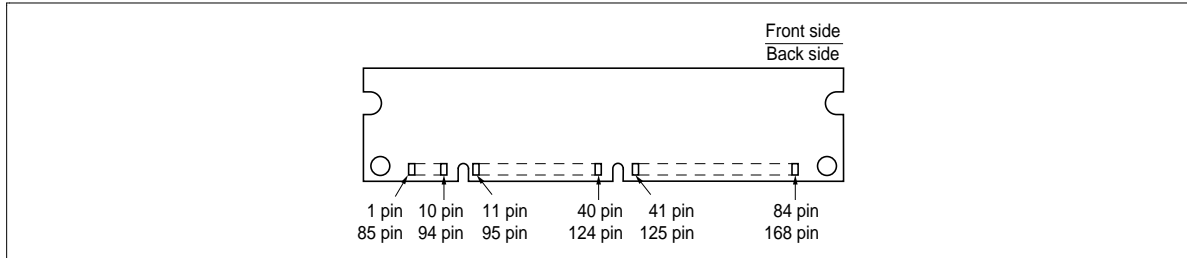
### Ordering Information

Type No.	Access time	Package	Contact pad
HB56UW272EJN-5	50 ns	168-pin dual lead out socket type	Gold
HB56UW272EJN-6	60 ns		
HB56UW272EJN-7	70 ns		
HB56UW272EJN-5L	50 ns		
HB56UW272EJN-6L	60 ns		
HB56UW272EJN-7L	70 ns		
HB56UW264EJN-5	50 ns		
HB56UW264EJN-6	60 ns		
HB56UW264EJN-7	70 ns		
HB56UW264EJN-5L	50 ns		
HB56UW264EJN-6L	60 ns		
HB56UW264EJN-7L	70 ns		

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## HB56UW272EJN Series, HB56UW264EJN Series

### Pin Arrangement



### Pin Arrangement

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V <sub>SS</sub>	43	V <sub>SS</sub>	85	V <sub>SS</sub>	127	V <sub>SS</sub>
2	DQ0	44	$\overline{\text{OE2}}$	86	DQ32	128	NC
3	DQ1	45	$\overline{\text{RAS2}}$	87	DQ33	129	NC
4	DQ2	46	$\overline{\text{CAS2}}$	88	DQ34	130	$\overline{\text{CAS6}}$
5	DQ3	47	$\overline{\text{CAS3}}$	89	DQ35	131	$\overline{\text{CAS7}}$
6	V <sub>CC</sub>	48	$\overline{\text{WE2}}$	90	V <sub>CC</sub>	132	NC
7	DQ4	49	V <sub>CC</sub>	91	DQ36	133	V <sub>CC</sub>
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2 (NC) <sup>*3</sup>	94	DQ39	136	CB6 (NC) <sup>*7</sup>
11	DQ8	53	CB3 (NC) <sup>*4</sup>	95	DQ40	137	CB7 (NC) <sup>*8</sup>
12	V <sub>SS</sub>	54	V <sub>SS</sub>	96	V <sub>SS</sub>	138	V <sub>SS</sub>
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V <sub>CC</sub>	101	DQ45	143	V <sub>CC</sub>
18	V <sub>CC</sub>	60	DQ20	102	V <sub>CC</sub>	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0 (NC) <sup>*1</sup>	63	NC	105	CB4 (NC) <sup>*5</sup>	147	NC
22	CB1 (NC) <sup>*2</sup>	64	V <sub>SS</sub>	106	CB5 (NC) <sup>*6</sup>	148	V <sub>SS</sub>
23	V <sub>SS</sub>	65	DQ21	107	V <sub>SS</sub>	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55

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## HB56UW272EJN Series, HB56UW264EJN Series

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### Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
26	V <sub>CC</sub>	68	V <sub>SS</sub>	110	V <sub>CC</sub>	152	V <sub>SS</sub>
27	$\overline{\text{WE0}}$	69	DQ24	111	NC	153	DQ56
28	$\overline{\text{CAS0}}$	70	DQ25	112	$\overline{\text{CAS4}}$	154	DQ57
29	$\overline{\text{CAS1}}$	71	DQ26	113	$\overline{\text{CAS5}}$	155	DQ58
30	$\overline{\text{RAS0}}$	72	DQ27	114	NC	156	DQ59
31	$\overline{\text{OE0}}$	73	V <sub>CC</sub>	115	NC	157	V <sub>CC</sub>
32	V <sub>SS</sub>	74	DQ28	116	V <sub>SS</sub>	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V <sub>SS</sub>	120	A7	162	V <sub>SS</sub>
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V <sub>CC</sub>	82	SDA	124	V <sub>CC</sub>	166	SA1
41	V <sub>CC</sub>	83	SCL	125	NC	167	SA2
42	NC	84	V <sub>CC</sub>	126	NC	168	V <sub>CC</sub>

- Notes:
1. CB0: HB56UW272EJN, NC: HB56UW264EJN
  2. CB1: HB56UW272EJN, NC: HB56UW264EJN
  3. CB2: HB56UW272EJN, NC: HB56UW264EJN
  4. CB3: HB56UW272EJN, NC: HB56UW264EJN
  5. CB4: HB56UW272EJN, NC: HB56UW264EJN
  6. CB5: HB56UW272EJN, NC: HB56UW264EJN
  7. CB6: HB56UW272EJN, NC: HB56UW264EJN
  8. CB7: HB56UW272EJN, NC: HB56UW264EJN

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## HB56UW272EJN Series, HB56UW264EJN Series

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### Pin Description

Pin name	Function
A0 to A10	Address input Row address: A0 to A10 Column address: A0 to A9 Refresh address: A0 to A10
DQ0 to DQ63	Data-in/data-out
$\overline{\text{RAS0}}$ , $\overline{\text{RAS2}}$	Row address strobe
$\overline{\text{CAS0}}$ to $\overline{\text{CAS7}}$	Column address strobe
$\overline{\text{WE0}}$ , $\overline{\text{WE2}}$	Read/Write enable
$\overline{\text{OE0}}$ , $\overline{\text{OE2}}$	Output enable
SDA	Serial data for PD
SCL	Serial clock for PD
SA0 to SA2	Serial address for PD
CB0 to CB7* <sup>1</sup>	Check bit
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

Note: 1. This function is supported only HB56UW272EJN Series.

## HB56UW272EJN Series, HB56UW264EJN Series

### Serial PD Matrix\*<sup>1</sup>

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128 byte
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	0	1	0	02	EDO
3	Number of row addresses bits	0	0	0	0	1	0	1	1	0B	11
4	Number of column addresses bits	0	0	0	0	1	0	1	0	0A	10
5	Number of banks	0	0	0	0	0	0	0	1	01	1
6	Module data width (HB56UW272EJN)	0	1	0	0	1	0	0	0	48	72
	(HB56UW264EJN)	0	1	0	0	0	0	0	0	40	64
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTTL
9	RAS access time -5/-5L	0	0	1	1	0	0	1	0	32	$t_{RAC} = 50$ ns
	-6/-6L	0	0	1	1	1	1	0	0	3C	$t_{RAC} = 60$ ns
	-7/-7L	0	1	0	0	0	1	1	0	46	$t_{RAC} = 70$ ns
10	CAS access time -5/-5L	0	0	0	0	1	1	0	1	0D	$t_{CAC} = 13$ ns
	-6/-6L	0	0	0	0	1	1	1	1	0F	$t_{CAC} = 15$ ns
	-7/-7L	0	0	0	1	0	0	1	0	12	$t_{CAC} = 18$ ns
11	Module configuration type (HB56UW272EJN)	0	0	0	0	0	0	1	0	02	ECC
	(HB56UW264EJN)	0	0	0	0	0	0	0	0	00	Non parity
12	Refresh rate/type -5/-6/-7	0	0	0	0	0	0	0	0	00	Normal (15.625 $\mu$ s)
	-5L/-6L/-7L	1	0	0	0	0	1	0	0	84	Self refresh (62.5 $\mu$ s)
13	DRAM width	0	0	0	0	1	0	0	0	08	2M $\times$ 8
14	Error checking DRAM width (HB56UW272EJN)	0	0	0	0	1	0	0	0	08	2M $\times$ 8
	(HB56UW264EJN)	0	0	0	0	0	0	0	0	00	—
15 to 31	Reserved for future offerings	0	0	0	0	0	0	0	0	00	
32 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future offerings
62	SPD data revision code	0	0	0	0	0	0	0	1	01	Rev.1

## HB56UW272EJN Series, HB56UW264EJN Series

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
63	Checksum for bytes 0 to 62 (HB56UW272EJN-5)	0	0	1	1	1	0	1	1	3B	
	(HB56UW272EJN-6)	0	1	0	0	0	1	1	1	47	
	(HB56UW272EJN-7)	0	1	0	1	0	1	0	0	54	
	(HB56UW272EJN-5L)	1	0	1	1	1	1	1	1	BF	
	(HB56UW272EJN-6L)	1	1	0	0	1	0	1	1	CB	
	(HB56UW272EJN-7L)	1	1	0	1	1	0	0	0	D8	
	(HB56UW264EJN-5)	0	0	1	0	1	0	0	1	29	
	(HB56UW264EJN-6)	0	0	1	1	0	1	0	1	35	
	(HB56UW264EJN-7)	0	1	0	0	0	0	1	0	42	
	(HB56UW264EJN-5L)	1	0	1	0	1	1	0	1	AD	
	(HB56UW264EJN-6L)	1	0	1	1	1	0	0	1	B9	
	(HB56UW264EJN-7L)	1	1	0	0	0	1	1	0	C6	
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	×	* <sup>2</sup> (ASCII-8bit code)
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
77	Manufacturer's part number	0	1	0	1	0	1	0	1	55	U
78	Manufacturer's part number	0	1	0	1	0	1	1	1	57	W
79	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
80	Manufacturer's part number (HB56UW272EJN)	0	0	1	1	0	1	1	1	37	7
	(HB56UW264EJN)	0	0	1	1	0	1	1	0	36	6
81	Manufacturer's part number (HB56UW272EJN)	0	0	1	1	0	0	1	0	32	2
	(HB56UW264EJN)	0	0	1	1	0	1	0	0	34	4
82	Manufacturer's part number	0	1	0	0	0	1	0	1	45	E
83	Manufacturer's part number	0	1	0	0	1	0	1	0	4A	J
84	Manufacturer's part number	0	1	0	0	1	1	1	0	4E	N
85	Manufacturer's part number	0	1	0	1	1	1	1	1	5F	—
86	Manufacturer's part number -5/-5L	0	0	1	1	0	1	0	1	35	5
	-6/-6L	0	0	1	1	0	1	1	0	36	6
	-7/-7L	0	0	1	1	0	1	1	1	37	7

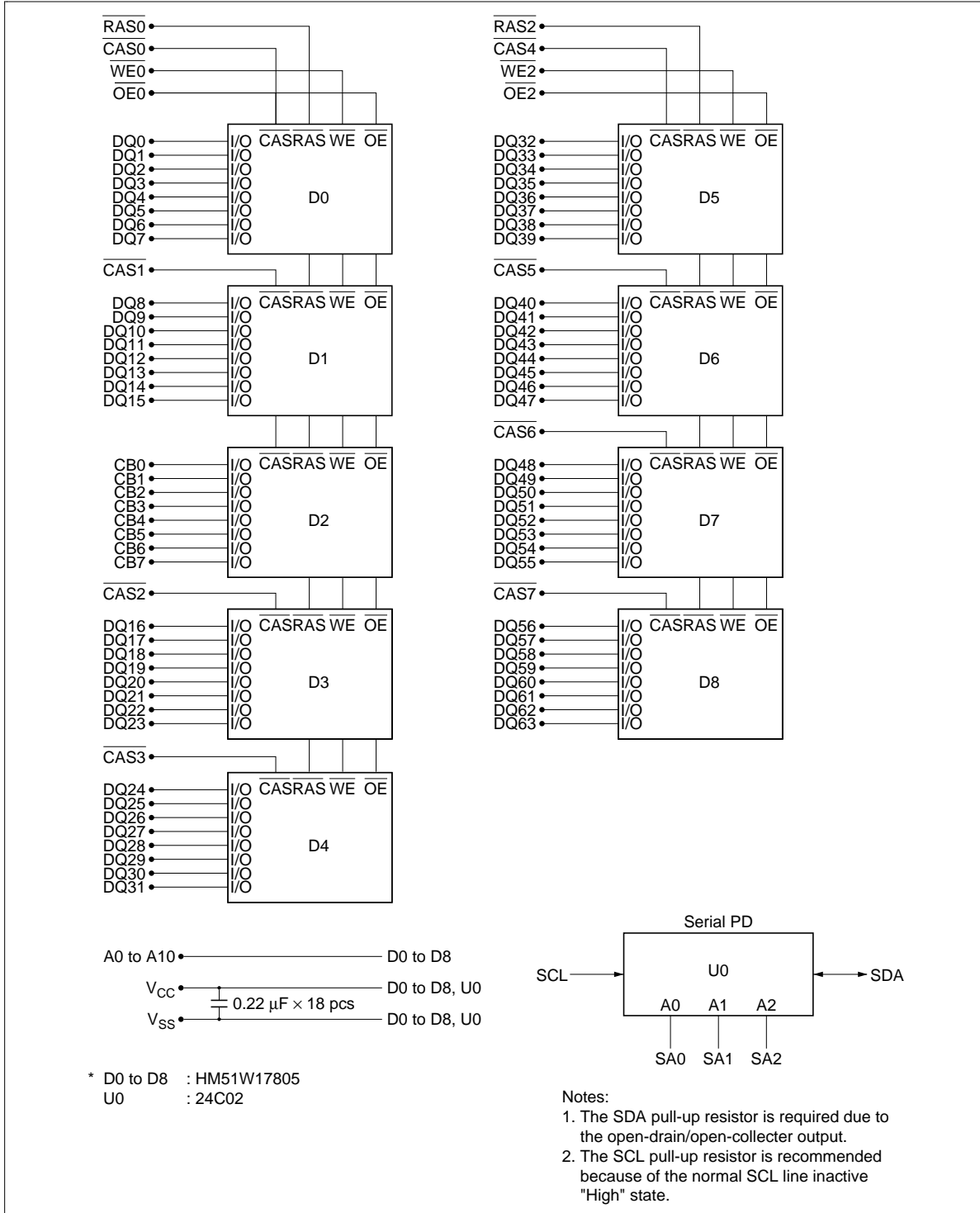
## HB56UW272EJN Series, HB56UW264EJN Series

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
87	Manufacturer's part number -5/-6/-7	0	0	1	0	0	0	0	0	20	(Space)
	-5L/-6L/-7L	0	1	0	0	1	1	0	0	4C	L
88	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	xx	Year code (binary) * <sup>3</sup>
94	Manufacturing date	×	×	×	×	×	×	×	×	xx	Weak code (binary) * <sup>4</sup>
95 to 98	Assembly serial number	* <sup>5</sup>									
99 to 125	Manufacturer specific data	* <sup>6</sup>									
126	Reserved	0	0	0	0	0	0	0	0	00	Not use
127	Reserved	0	0	0	0	0	0	0	0	00	Not use

- Notes:
1. All serial PD data are not protected. 0: Serial data, "driven Low", 1: Serial data, "driven High"
  2. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4Ah. 4Ah shows "J" on ASCII code.)
  3. Byte 93 (Manufacturing date-year code) ex: 61h shows year '97. 62h shows year '98.
  4. Byte 94 (Manufacturing date-week code) ex: 0Bh shows week 11. 24h shows week 36.
  5. Byte 95 through 98 are assembly serial number.
  6. All bits of 99 through 125 are not defined ("1" or "0").

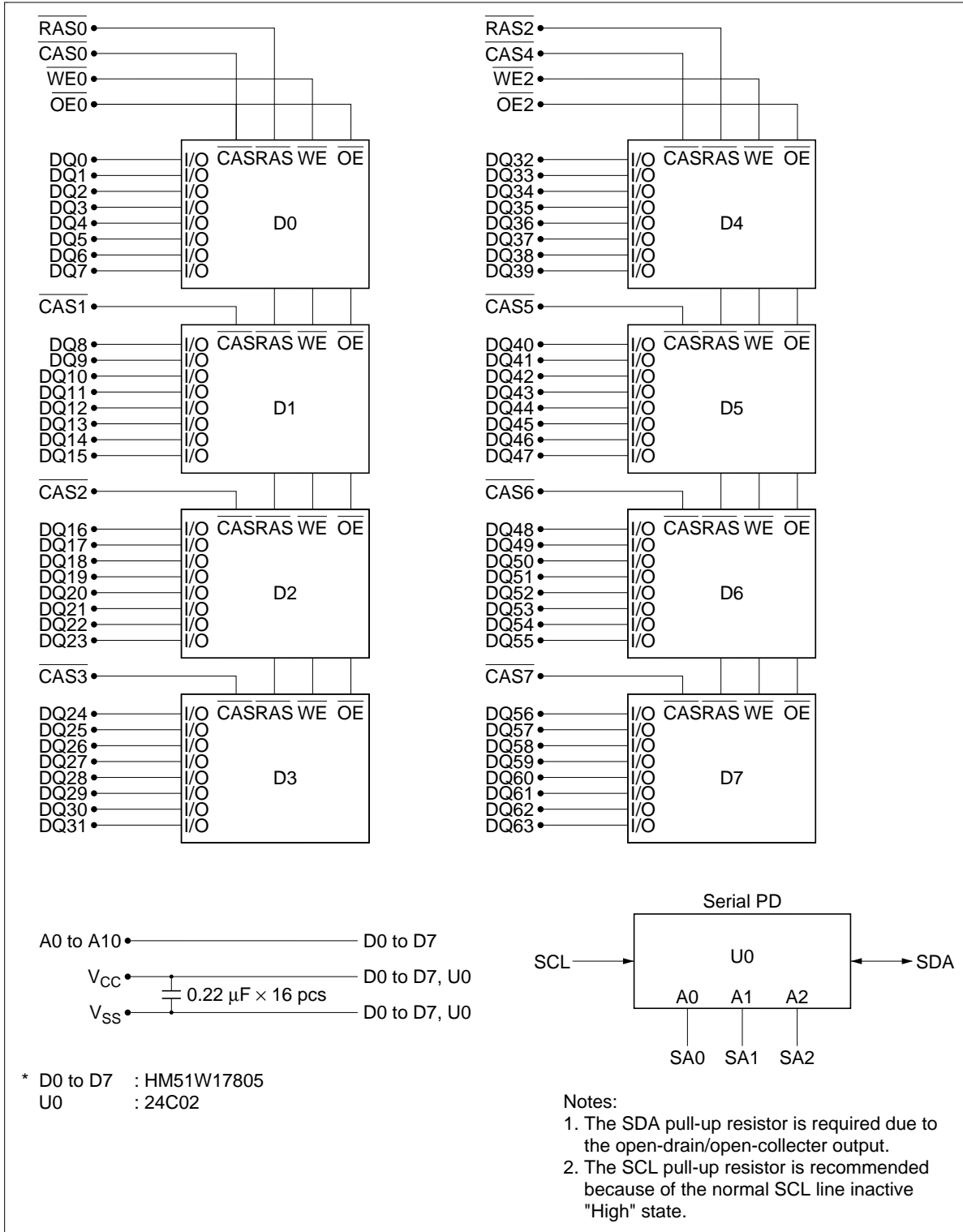
# HB56UW272EJN Series, HB56UW264EJN Series

## Block Diagram (HB56UW272EJN)



# HB56UW272EJN Series, HB56UW264EJN Series

## Block Diagram (HB56UW264EJN)



## HB56UW272EJN Series, HB56UW264EJN Series

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 to +4.6	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation (HB56UW272EJN)	Pt	9	W
Power dissipation (HB56UW264EJN)	Pt	8	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

### Recommended DC Operating Conditions ( $T_a = 0$ to $70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{SS}$	0	0	0	V	
	$V_{CC}$	3.0	3.3	3.6	V	1
Input high voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	$V_{IL}$	-0.3	—	0.8	V	1

Note: 1. All voltage referred to  $V_{SS}$ .

## HB56UW272EJN Series, HB56UW264EJN Series

DC Characteristics (Ta = 0 to 70°C, V<sub>CC</sub> = 3.3 V ± 0.3V, V<sub>SS</sub> = 0 V) (HB56UW272EJN)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I <sub>CC1</sub>	—	990	—	900	—	810	mA	t <sub>RC</sub> = min	1, 2
Standby current	I <sub>CC2</sub>	—	18	—	18	—	18	mA	TTL interface R <sub>AS</sub> , C <sub>AS</sub> = V <sub>IH</sub> Dout = High-Z	
		—	9	—	9	—	9	mA	CMOS interface R <sub>AS</sub> , C <sub>AS</sub> ≥ V <sub>CC</sub> - 0.2 V Dout = High-Z	
Standby current (L-version)	I <sub>CC2</sub>	—	1.35	—	1.35	—	1.35	mA	CMOS interface R <sub>AS</sub> , C <sub>AS</sub> ≥ V <sub>CC</sub> - 0.2 V Dout = High-Z	
R <sub>AS</sub> -only refresh current	I <sub>CC3</sub>	—	990	—	900	—	810	mA	t <sub>RC</sub> = min	2
Standby current	I <sub>CC5</sub>	—	45	—	45	—	45	mA	R <sub>AS</sub> = V <sub>IH</sub> , C <sub>AS</sub> = V <sub>IL</sub> Dout = enable	1
C <sub>AS</sub> -before-R <sub>AS</sub> refresh current	I <sub>CC6</sub>	—	990	—	900	—	810	mA	t <sub>RC</sub> = min	
EDO page mode current	I <sub>CC7</sub>	—	900	—	810	—	765	mA	t <sub>HPC</sub> = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I <sub>CC10</sub>	—	3.6	—	3.6	—	3.6	mA	CMOS interface Dout = High-Z CBR refresh: t <sub>RC</sub> = 62.5 μs t <sub>RAS</sub> ≤ 0.3 μs	4
Self refresh mode current (L-version)	I <sub>CC11</sub>	—	2.25	—	2.25	—	2.25	mA	CMOS interface R <sub>AS</sub> , C <sub>AS</sub> ≤ 0.2 V Dout = High-Z	
Input leakage current	I <sub>LI</sub>	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I <sub>LO</sub>	-10	10	-10	10	-10	10	μA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V <sub>OH</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	High Iout = -2 mA	
Output low voltage	V <sub>OL</sub>	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I<sub>CC</sub> depends on output load condition when the device is selected, I<sub>CC</sub> max is specified at the output open condition.

2. Address can be changed once or less while R<sub>AS</sub> = V<sub>IL</sub>.

3. Address can be changed once or less while C<sub>AS</sub> = V<sub>IH</sub>.

4. C<sub>AS</sub> = L (≤ 0.2 V) while R<sub>AS</sub> = L (≤ 0.2 V).

## HB56UW272EJN Series, HB56UW264EJN Series

**DC Characteristics** ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3\text{V}$ ,  $V_{SS} = 0 \text{ V}$ ) (HB56UW264EJN)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	$I_{CC1}$	—	880	—	800	—	720	mA	$t_{RC} = \text{min}$	1, 2
Standby current	$I_{CC2}$	—	16	—	16	—	16	mA	TTL interface $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$ Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z	
Standby current (L-version)	$I_{CC2}$	—	1.2	—	1.2	—	1.2	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z	
$\overline{\text{RAS}}$ -only refresh current	$I_{CC3}$	—	880	—	800	—	720	mA	$t_{RC} = \text{min}$	2
Standby current	$I_{CC5}$	—	40	—	40	—	40	mA	$\overline{\text{RAS}} = V_{IH}, \overline{\text{CAS}} = V_{IL}$ Dout = enable	1
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	$I_{CC6}$	—	880	—	800	—	720	mA	$t_{RC} = \text{min}$	
EDO page mode current	$I_{CC7}$	—	800	—	720	—	680	mA	$t_{HPC} = \text{min}$	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	$I_{CC10}$	—	3.2	—	3.2	—	3.2	mA	CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 62.5 \mu\text{s}$ $t_{RAS} \leq 0.3 \mu\text{s}$	4
Self refresh mode current (L-version)	$I_{CC11}$	—	2	—	2	—	2	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \leq 0.2 \text{ V}$ Dout = High-Z	
Input leakage current	$I_{LI}$	-10	10	-10	10	-10	10	$\mu\text{A}$	$0 \text{ V} \leq V_{in} \leq 4.6 \text{ V}$	
Output leakage current	$I_{LO}$	-10	10	-10	10	-10	10	$\mu\text{A}$	$0 \text{ V} \leq V_{out} \leq 4.6 \text{ V}$ Dout = disable	
Output high voltage	$V_{OH}$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	High Iout = -2 mA	
Output low voltage	$V_{OL}$	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

- Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected,  $I_{CC}$  max is specified at the output open condition.  
 2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .  
 3. Address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .  
 4.  $\overline{\text{CAS}} = L$  ( $\leq 0.2 \text{ V}$ ) while  $\overline{\text{RAS}} = L$  ( $\leq 0.2 \text{ V}$ ).

## HB56UW272EJN Series, HB56UW264EJN Series

### Capacitance (Ta = 25°C, V<sub>CC</sub> = 3.3 V ± 0.3 V) (HB56UW272EJN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C <sub>11</sub>	—	65	pF	1
Input capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	C <sub>12</sub>	—	55	pF	1
Input capacitance ( $\overline{\text{CAS}}$ )	C <sub>13</sub>	—	34	pF	1
I/O capacitance (DQ, CB)	C <sub>I/O</sub>	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2.  $\overline{\text{CAS}} = V_{\text{IH}}$  to disable Dout.

### Capacitance (Ta = 25°C, V<sub>CC</sub> = 3.3 V ± 0.3 V) (HB56UW264EJN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C <sub>11</sub>	—	60	pF	1
Input capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	C <sub>12</sub>	—	48	pF	1
Input capacitance ( $\overline{\text{CAS}}$ )	C <sub>13</sub>	—	27	pF	1
I/O capacitance (DQ)	C <sub>I/O</sub>	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2.  $\overline{\text{CAS}} = V_{\text{IH}}$  to disable Dout.

### AC Characteristics (Ta = 0 to 70°C, V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0 V) \*<sup>1</sup>, \*<sup>2</sup>, \*<sup>18</sup>, \*<sup>19</sup>

#### Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C<sub>L</sub> (100 pF) (Including scope and jig)

## HB56UW272EJN Series, HB56UW264EJN Series

### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	$t_{RC}$	84	—	104	—	124	—	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	30	—	40	—	50	—	ns	
$\overline{CAS}$ precharge time	$t_{CP}$	8	—	10	—	13	—	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	50	10000	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	8	10000	10	10000	13	10000	ns	
Row address setup time	$t_{ASR}$	0	—	0	—	0	—	ns	
Row address hold time	$t_{RAH}$	8	—	10	—	10	—	ns	
Column address setup time	$t_{ASC}$	0	—	0	—	0	—	ns	
Column address hold time	$t_{CAH}$	8	—	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	12	37	14	45	14	52	ns	3
$\overline{RAS}$ to column address delay time	$t_{RAD}$	10	25	12	30	12	35	ns	4
$\overline{RAS}$ hold time	$t_{RSH}$	10	—	13	—	13	—	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	35	—	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	—	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	$t_{OED}$	13	—	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	$t_{DZO}$	0	—	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	$t_{DZC}$	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	$t_T$	2	50	2	50	2	50	ns	7
Refresh period (2,048 cycles)	$t_{REF}$	—	32	—	32	—	32	ms	
Refresh period (2,048 cycles) (L-version)	$t_{REF}$	—	128	—	128	—	128	ms	

## HB56UW272EJN Series, HB56UW264EJN Series

### Read Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	50	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	13	—	15	—	18	ns	9, 10, 17
Access time from address	$t_{\text{AA}}$	—	25	—	30	—	35	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	—	13	—	15	—	18	ns	9, 21
Read command setup time	$t_{\text{RCS}}$	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	—	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	$t_{\text{RCHR}}$	50	—	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	5	—	5	—	5	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	25	—	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	$t_{\text{CAL}}$	15	—	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	0	—	0	—	0	—	ns	
Output data hold time	$t_{\text{OH}}$	3	—	3	—	3	—	ns	22
Output data hold time from $\overline{\text{OE}}$	$t_{\text{OHO}}$	3	—	3	—	3	—	ns	
Output buffer turn-off time	$t_{\text{OFF}}$	—	13	—	15	—	15	ns	13, 22
Output buffer turn-off to $\overline{\text{OE}}$	$t_{\text{OEZ}}$	—	13	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	$t_{\text{CDD}}$	13	—	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	$t_{\text{OHR}}$	3	—	3	—	3	—	ns	22
Output buffer turn-off time to $\overline{\text{RAS}}$	$t_{\text{OFR}}$	—	13	—	15	—	15	ns	22
Output buffer turn-off to $\overline{\text{WE}}$	$t_{\text{WEZ}}$	—	13	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	$t_{\text{WED}}$	13	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	$t_{\text{RDD}}$	13	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ next $\overline{\text{CAS}}$ delay time	$t_{\text{RNCD}}$	50	—	60	—	70	—	ns	

## HB56UW272EJN Series, HB56UW264EJN Series

### Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	$t_{WCS}$	0	—	0	—	0	—	ns	14
Write command hold time	$t_{WCH}$	8	—	10	—	13	—	ns	
Write command pulse width	$t_{WP}$	8	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	8	—	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	8	—	10	—	13	—	ns	
Data-in setup time	$t_{DS}$	0	—	0	—	0	—	ns	15
Data-in hold time	$t_{DH}$	8	—	10	—	13	—	ns	15

### Read-Modify-Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	$t_{RWC}$	111	—	135	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	67	—	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	30	—	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	$t_{AWD}$	42	—	49	—	57	—	ns	14
$\overline{OE}$ hold time $\overline{WE}$	$t_{OEH}$	13	—	15	—	18	—	ns	

### Refresh Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle)	$t_{CSR}$	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	$t_{CHR}$	8	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	$t_{WRP}$	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	$t_{WRH}$	8	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	5	—	5	—	5	—	ns	

## HB56UW272EJN Series, HB56UW264EJN Series

### EDO Page Mode Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EDO page mode cycle time	$t_{HPC}$	20	—	25	—	30	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	$t_{RASP}$	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	—	30	—	35	—	40	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	$t_{CPRH}$	30	—	35	—	40	—	ns	
Output data hole time from $\overline{CAS}$ low	$t_{DOH}$	3	—	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time referred $\overline{OE}$	$t_{COL}$	8	—	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	$t_{COP}$	5	—	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	$t_{RCHC}$	30	—	35	—	40	—	ns	

### EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EDO page mode read-modify-write cycle time	$t_{HPRWC}$	57	—	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	$t_{CPW}$	45	—	54	—	62	—	ns	14

### Self Refresh Mode (L-version)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ pulse width (Self refresh)	$t_{RASS}$	100	—	100	—	100	—	$\mu$ s	
$\overline{RAS}$ precharge time (Self refresh)	$t_{RPS}$	90	—	110	—	130	—	ns	
$\overline{CAS}$ hold time (Self refresh)	$t_{CHS}$	-50	—	-50	—	-50	—	ns	

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## HB56UW272EJN Series, HB56UW264EJN Series

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- Notes:
1. AC measurements assume  $t_r = 2$  ns.
  2. An initial pause of 200  $\mu$ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{\text{RAS}}$ -only refresh cycle or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles are required.
  3. Operation with the  $t_{\text{RCD}}$  (max) limit insures that  $t_{\text{RAC}}$  (max) can be met,  $t_{\text{RCD}}$  (max) is specified as a reference point only; if  $t_{\text{RCD}} \geq t_{\text{RAD}} (\text{max}) + t_{\text{AA}} (\text{max}) - t_{\text{CAC}} (\text{max})$ , then access time is controlled exclusively by  $t_{\text{CAC}}$ .
  4. Operation with the  $t_{\text{RAD}}$  (max) limit insures that  $t_{\text{RAC}}$  (max) can be met,  $t_{\text{RAD}}$  (max) is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}$  (max) limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
  5. Either  $t_{\text{OED}}$  or  $t_{\text{CDD}}$  must be satisfied.
  6. Either  $t_{\text{DZO}}$  or  $t_{\text{DZC}}$  must be satisfied.
  7.  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max).
  8. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}} (\text{max})$ . If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  exceeds the value shown.
  9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
  10. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{max})$  and  $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \geq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$ .
  11. Assumes that  $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{max})$  and  $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \leq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$ .
  12. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycles.
  13.  $t_{\text{OFF}} (\text{max})$  and  $t_{\text{OEZ}} (\text{max})$  define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
  14.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$ , and  $t_{\text{CPW}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{min})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$ , and  $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$  or  $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$  and  $t_{\text{CPW}} \geq t_{\text{CPW}} (\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  15. These parameters are referred to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in delayed write or read-modify-write cycles.
  16.  $t_{\text{RASP}}$  defines  $\overline{\text{RAS}}$  pulse width in EDO page mode cycles.
  17. Access time is determined by the longest among  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{CPA}}$ .
  18. In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device. After  $\overline{\text{RAS}}$  is reset, if  $t_{\text{OEH}} \geq t_{\text{CWL}}$ , the DQ pin will remain open circuit (high impedance);  $t_{\text{OEH}} < t_{\text{OEH}}$ , invalid data will be out at each DQ.
  19. All the  $V_{\text{CC}}$  and  $V_{\text{SS}}$  pins shall be supplied with the same voltages.
  20.  $t_{\text{HPC}} (\text{min})$  can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode  $\overline{\text{RAS}}$  cycle (EDO page mode mix cycle (1), (2)), minimum value of  $\overline{\text{CAS}}$  cycle ( $t_{\text{CAS}} + t_{\text{CP}} + 2t_r$ ) becomes greater than the specified  $t_{\text{HPC}} (\text{min})$  value. The value of  $\overline{\text{CAS}}$  cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
  21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large  $V_{\text{CC}} / V_{\text{SS}}$  line noise, which causes to degrade  $V_{\text{IH}} \text{ min.} / V_{\text{IL}} \text{ max.}$  level.
  22. Data output turns off and becomes high impedance from later rising edge of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . Hold time and turn off time are specified by the timing specifications of later rising edge of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  between  $t_{\text{OHR}}$  and  $t_{\text{OH}}$ , and between  $t_{\text{OFR}}$  and  $t_{\text{OFF}}$ .
  23. Please do not use  $t_{\text{RASS}}$  timing,  $10 \mu\text{s} \leq t_{\text{RASS}} \leq 100 \mu\text{s}$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{\text{RASS}} \geq 100 \mu\text{s}$ , then  $\overline{\text{RAS}}$  precharge time should use  $t_{\text{RPS}}$  instead of  $t_{\text{RP}}$ .

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## HB56UW272EJN Series, HB56UW264EJN Series

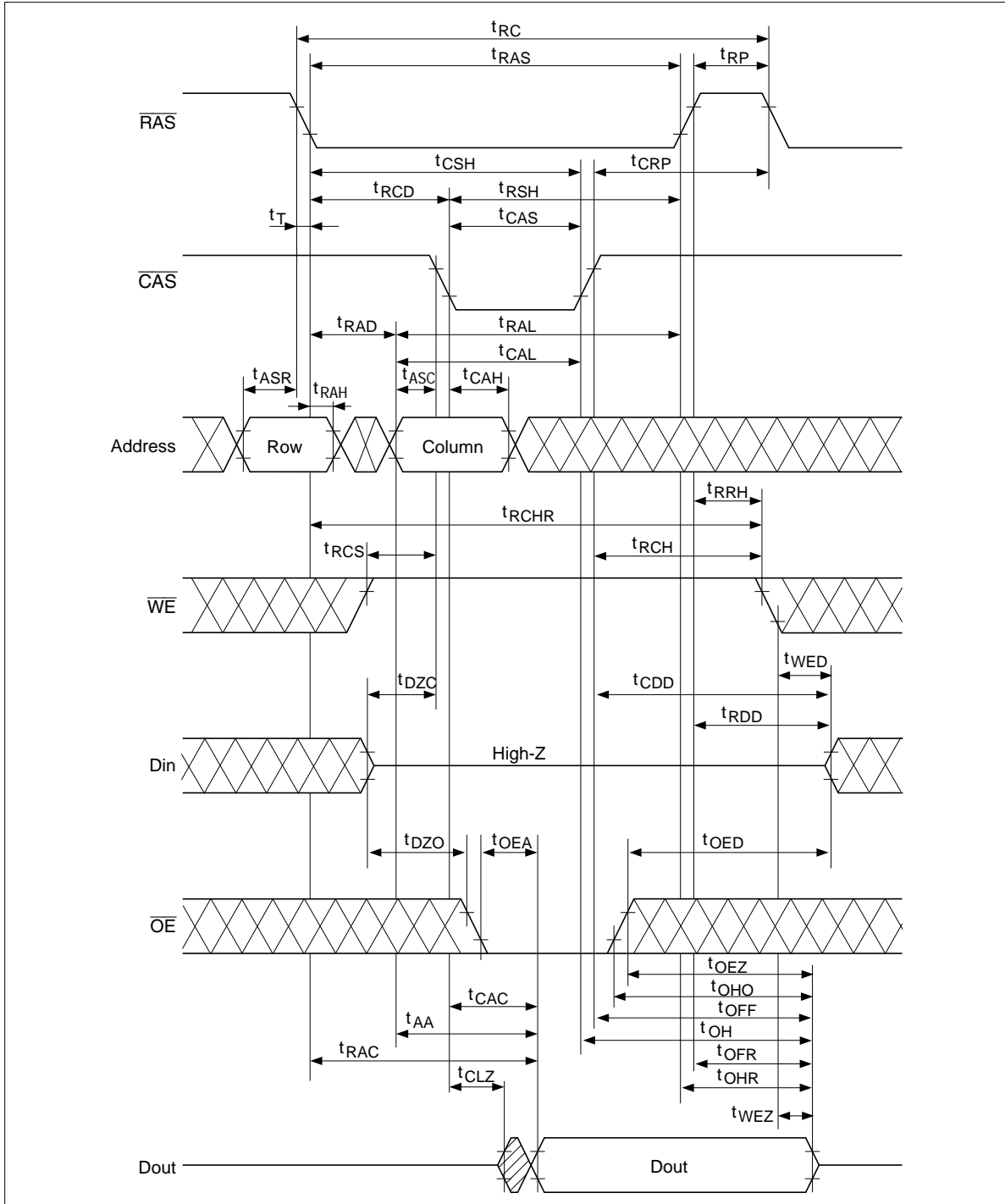
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24. If you use distributed CBR refresh mode with 15.6  $\mu\text{s}$  interval in normal read/write cycle, CBR refresh should be executed within 15.6  $\mu\text{s}$  immediately after exiting from and before entering into self refresh mode.
25. If you use  $\overline{\text{RAS}}$  only refresh or CBR burst refresh mode in normal read/write cycle, 2048 of distributed CBR refresh with 15.6  $\mu\text{s}$  interval should be executed within 32 ms immediately after exiting from and before entering into the self refresh mode.
26. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
27. XXX: H or L (H:  $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$ , L:  $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$ )  
/////: Invalid Dout  
When the address, clock and input pins are not described on timing waveforms, their pins must be applied  $V_{\text{IH}}$  or  $V_{\text{IL}}$ .

# HB56UW272EJN Series, HB56UW264EJN Series

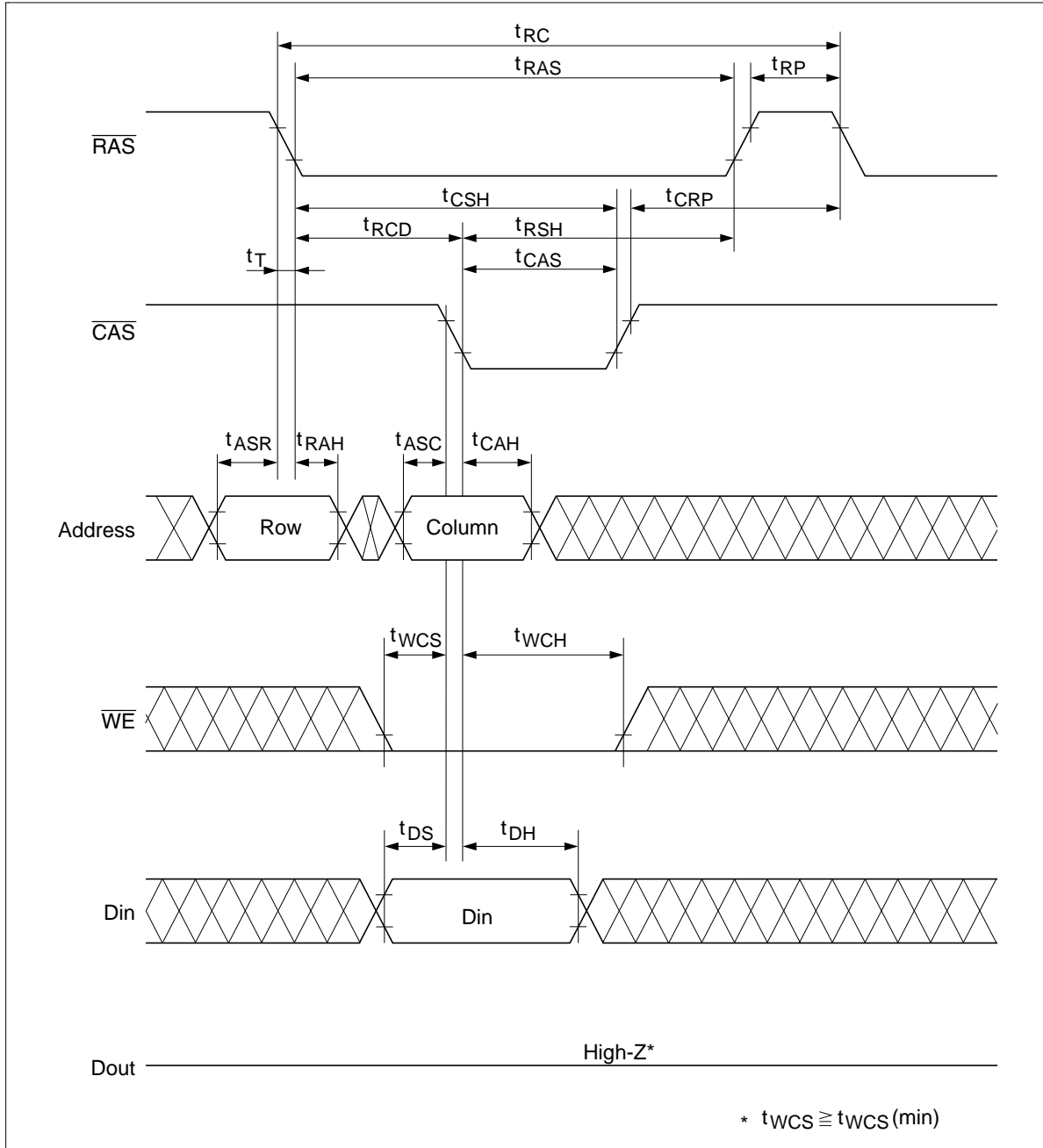
## Timing Waveforms\*27

### Read Cycle



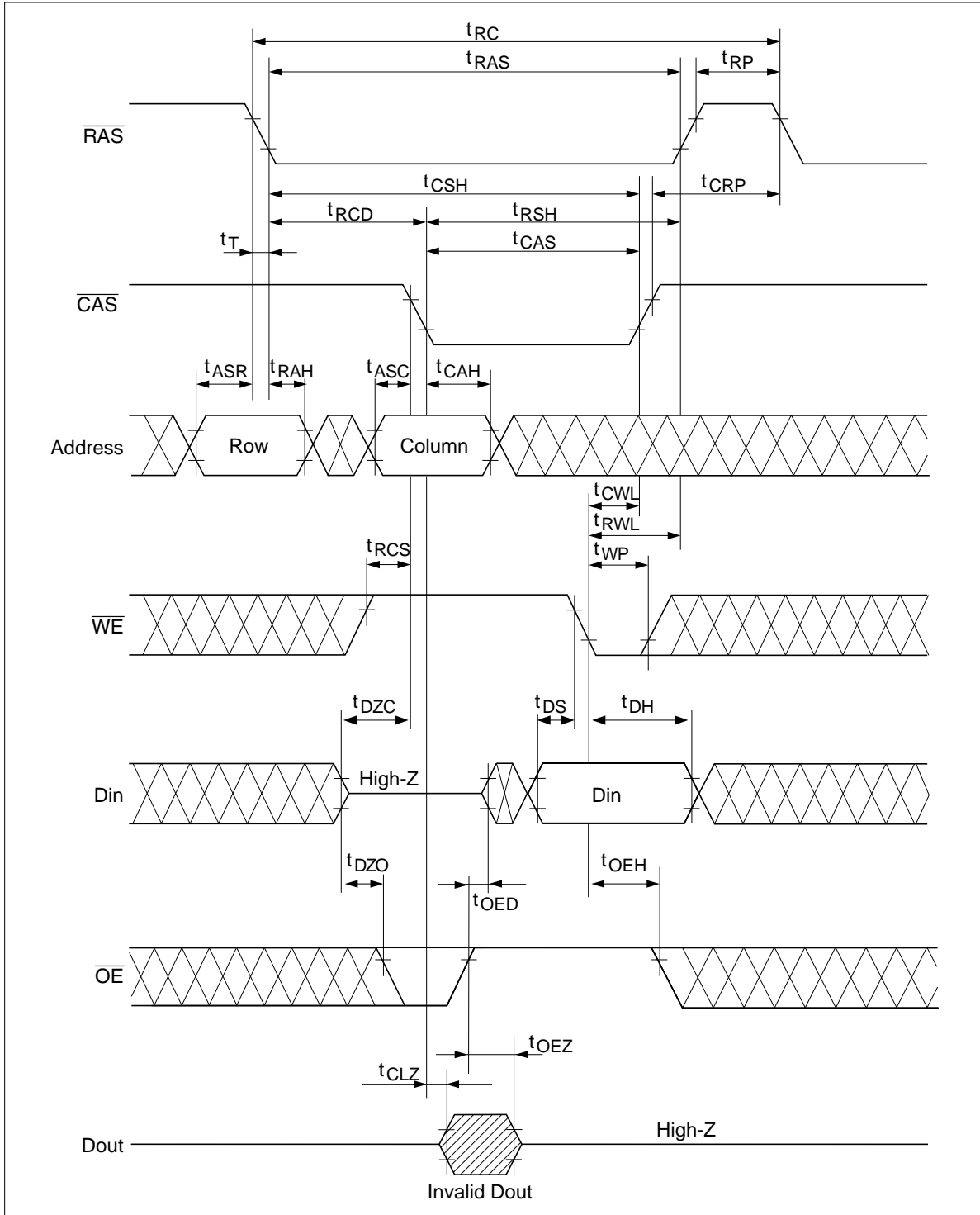
# HB56UW272EJN Series, HB56UW264EJN Series

## Early Write Cycle



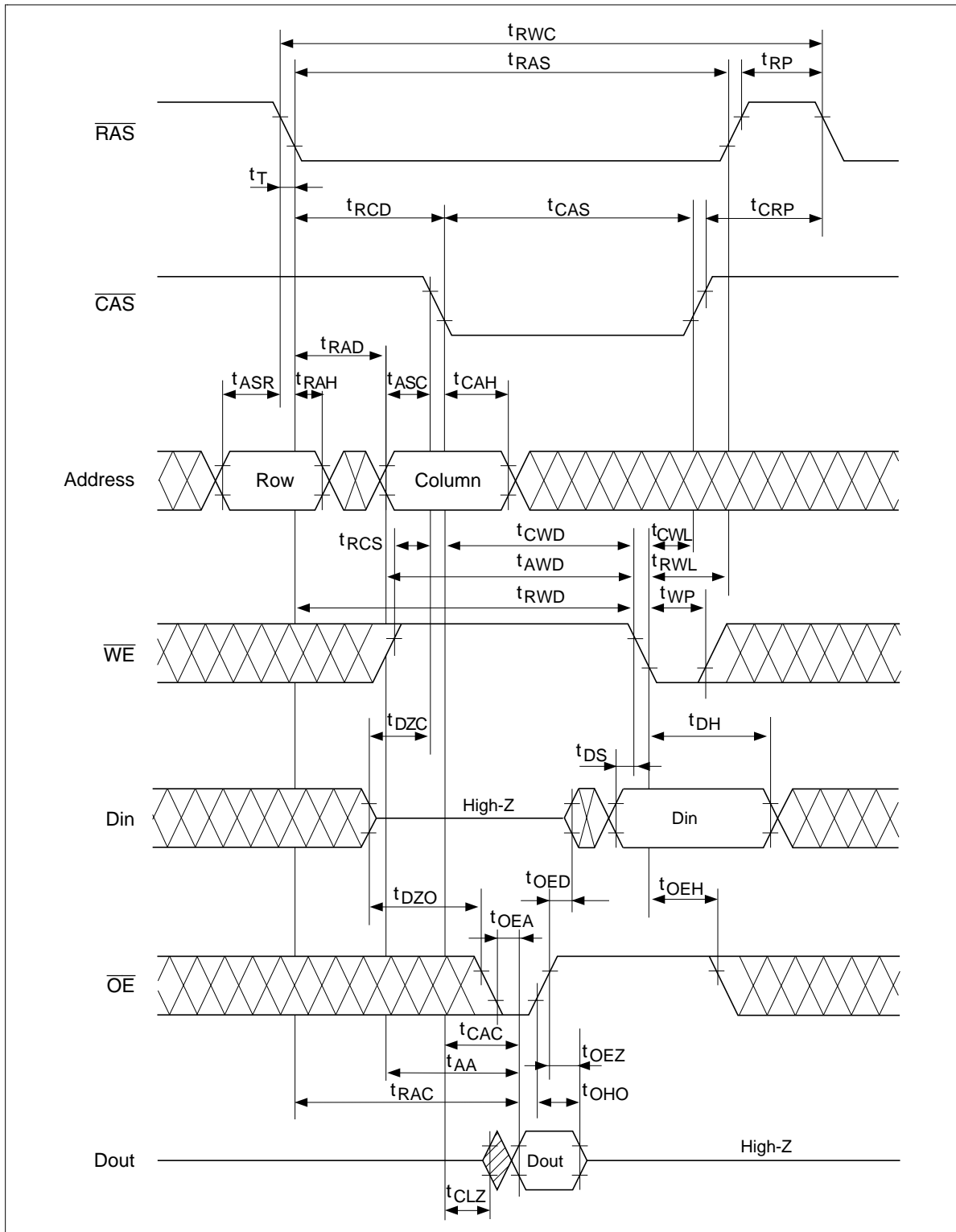
# HB56UW272EJN Series, HB56UW264EJN Series

## Delayed Write Cycle<sup>\*18</sup>



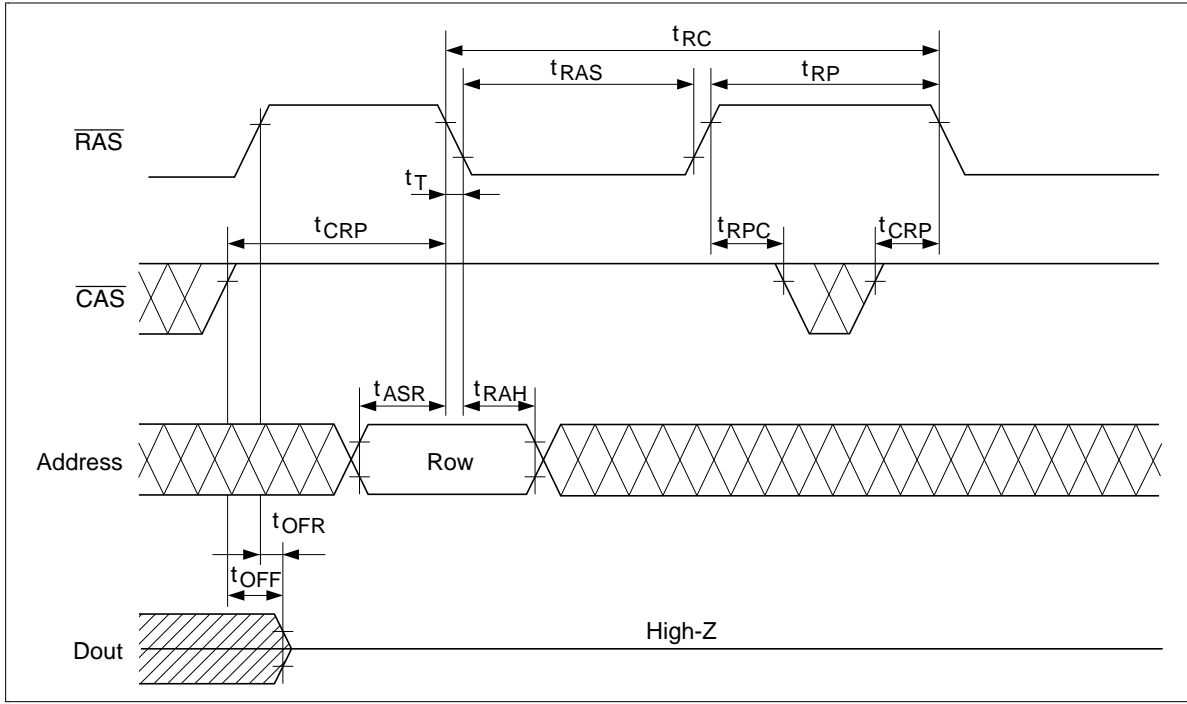
# HB56UW272EJN Series, HB56UW264EJN Series

## Read-Modify-Write Cycle\*18



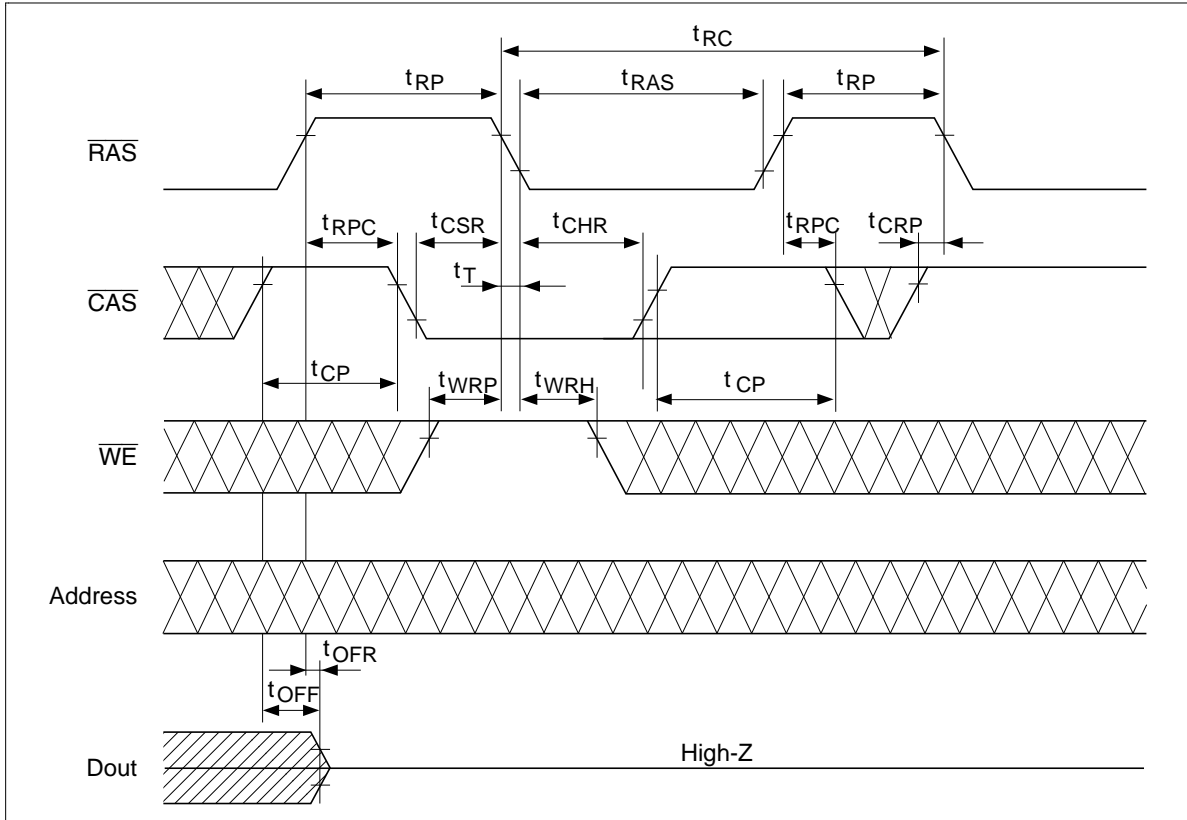
# HB56UW272EJN Series, HB56UW264EJN Series

## $\overline{\text{RAS}}$ -Only Refresh Cycle



# HB56UW272EJN Series, HB56UW264EJN Series

## $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

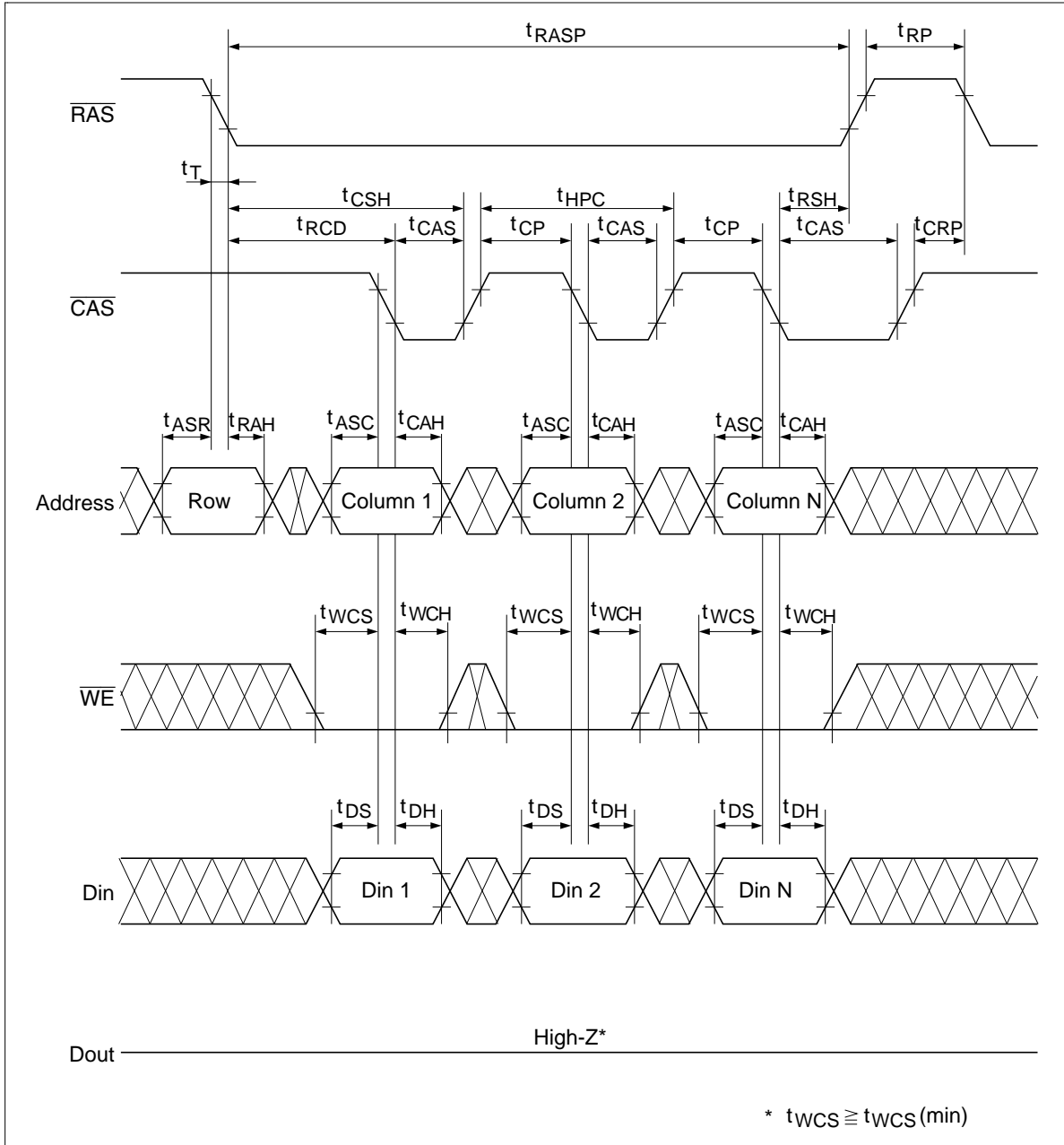






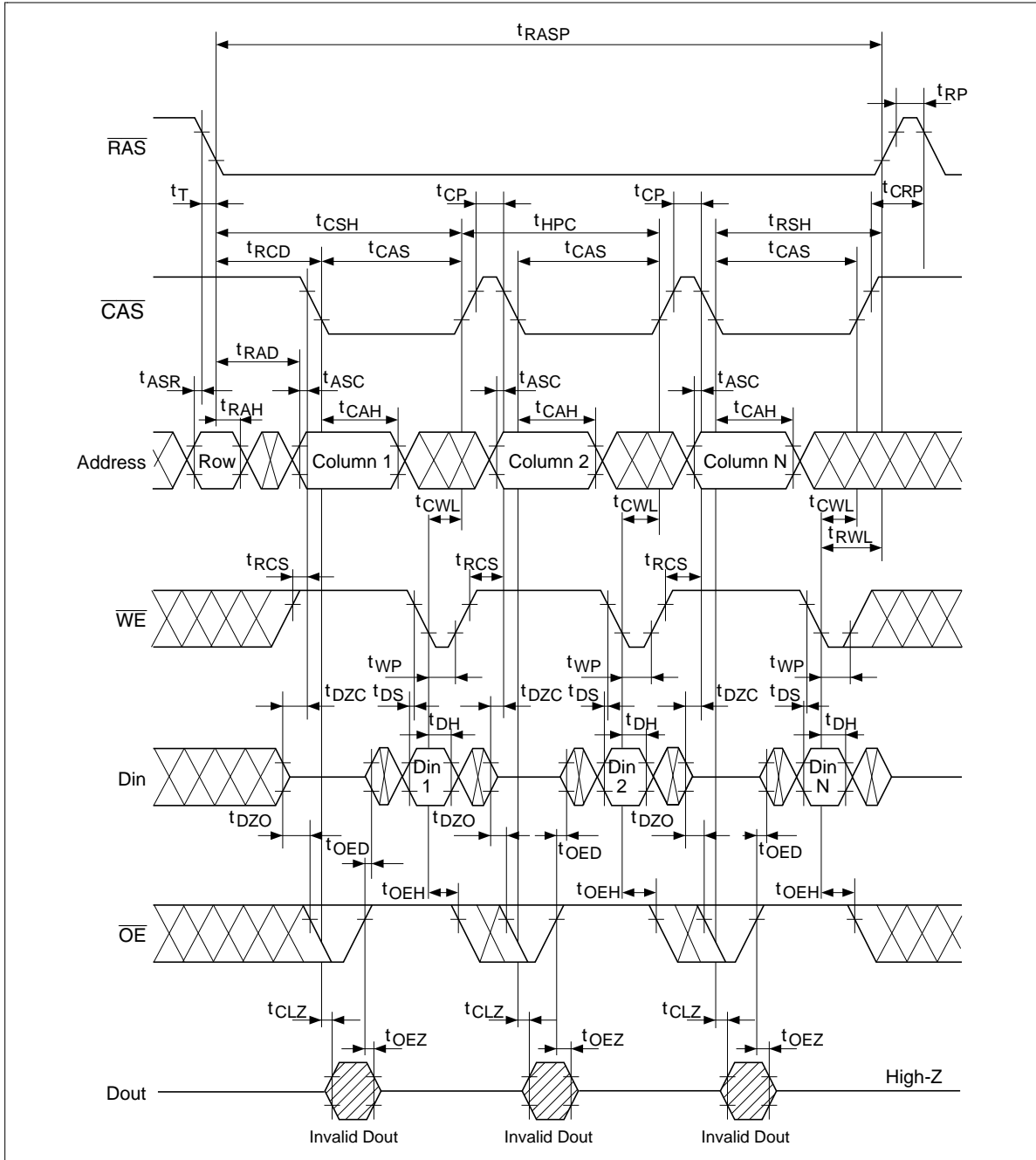
# HB56UW272EJN Series, HB56UW264EJN Series

## EDO Page Mode Early Write Cycle



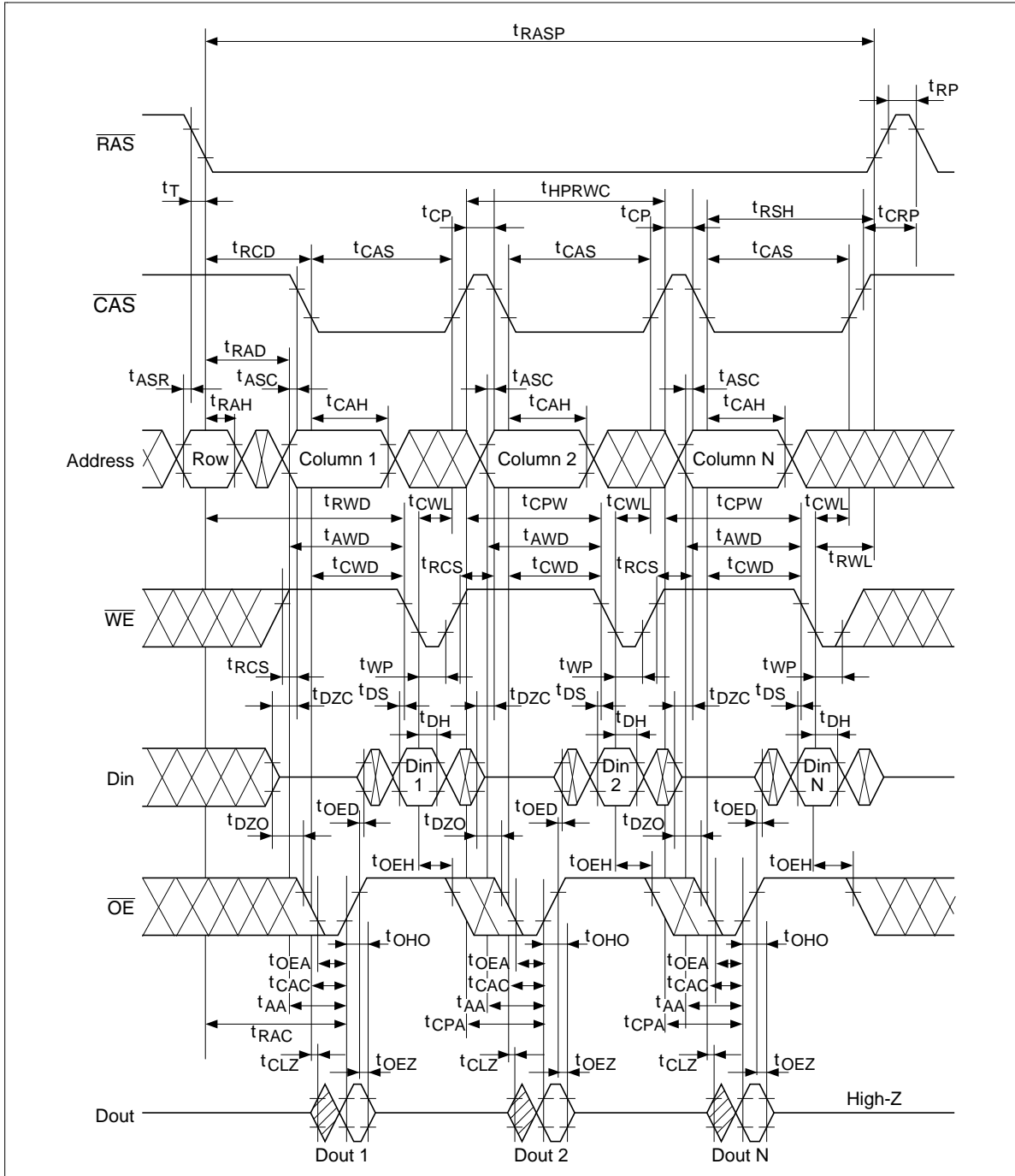
# HB56UW272EJN Series, HB56UW264EJN Series

## EDO Page Mode Delayed Write Cycle\*18



# HB56UW272EJN Series, HB56UW264EJN Series

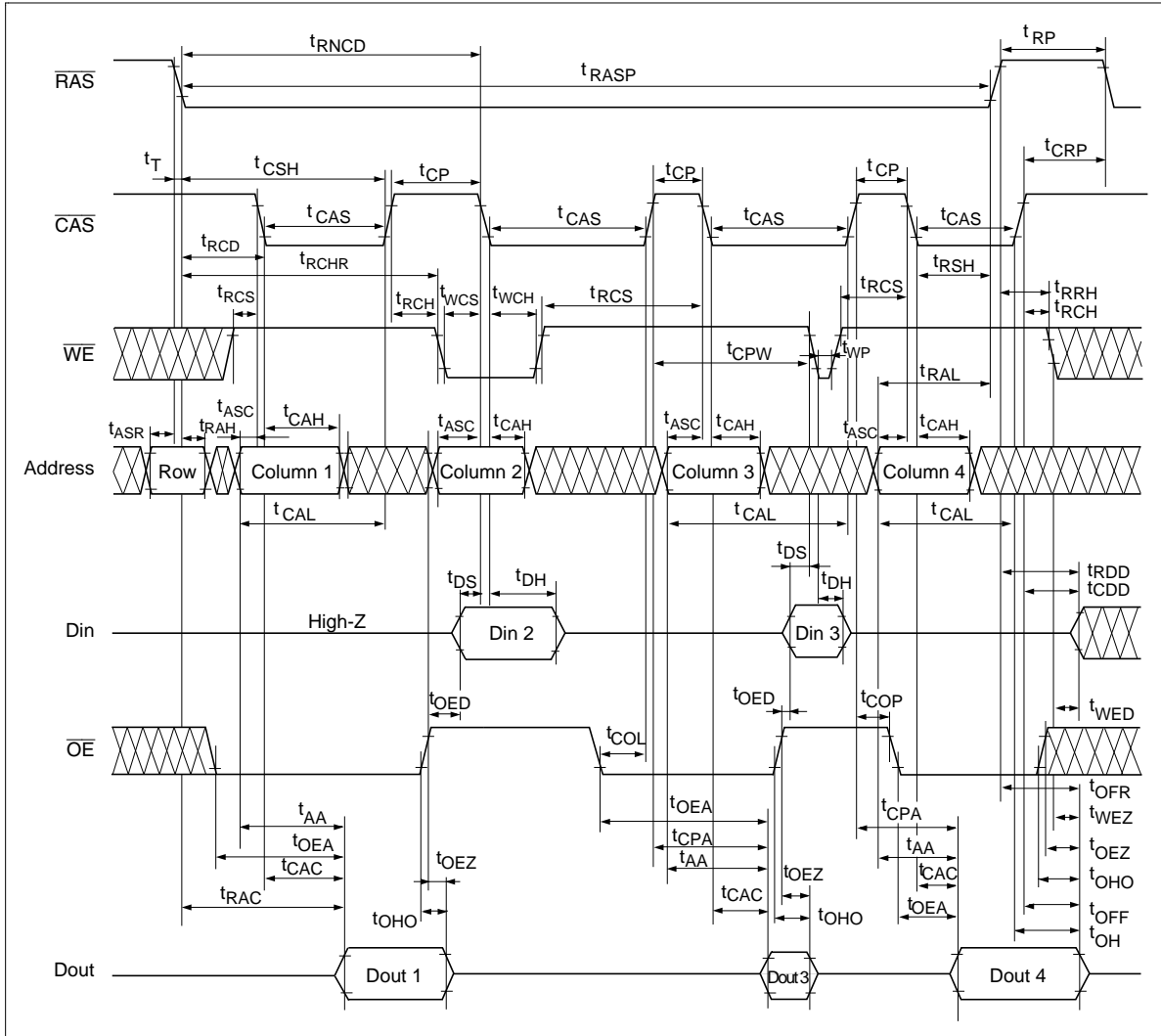
## EDO Page Mode Read-Modify-Write Cycle\*18





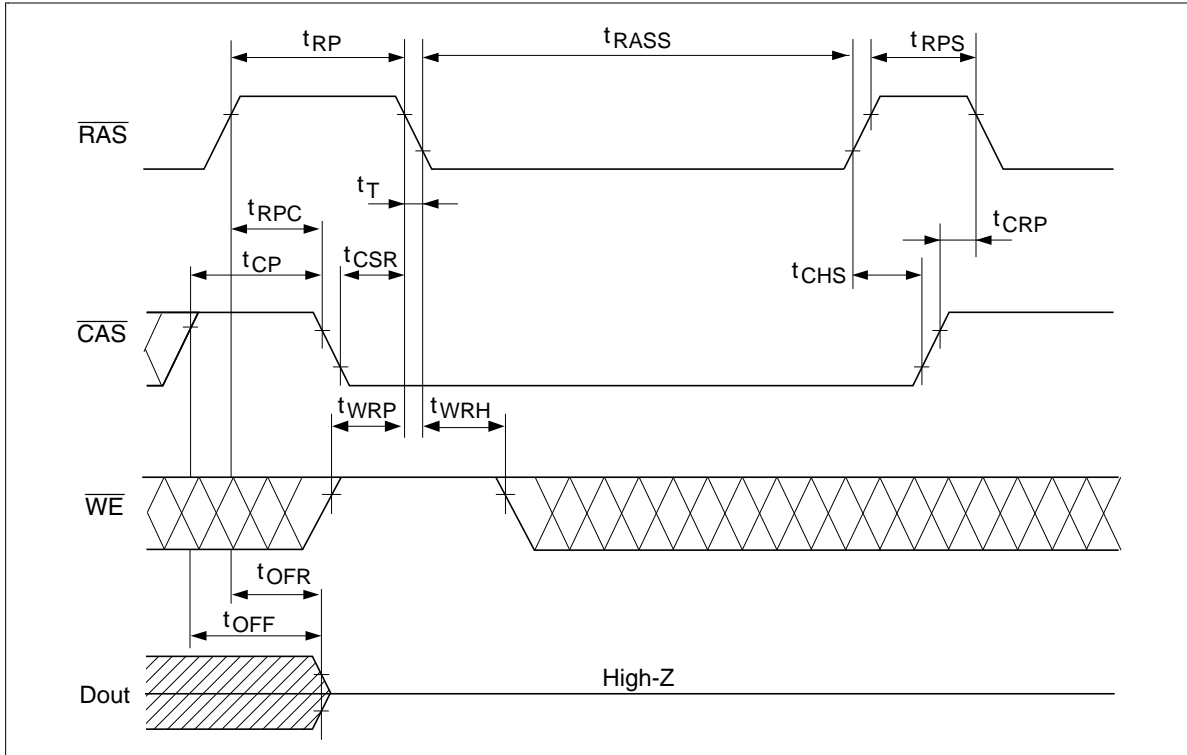
# HB56UW272EJN Series, HB56UW264EJN Series

## EDO Page Mode Mix Cycle (2)



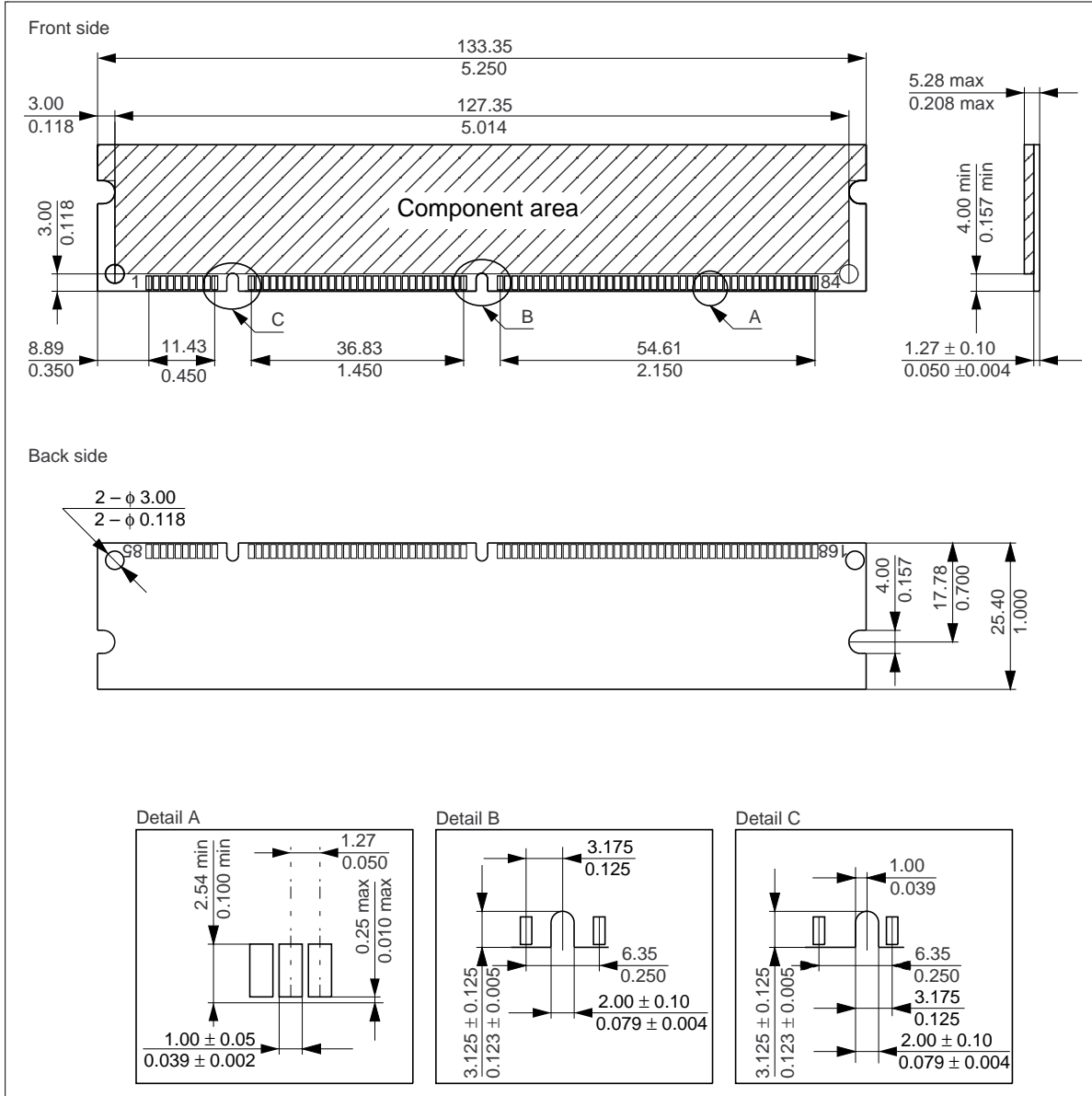
# HB56UW272EJN Series, HB56UW264EJN Series

Self Refresh Cycle (L-version) \* 23, 24, 25, 26



# HB56UW272EJN Series, HB56UW264EJN Series

**Physical Outline/ Unit: mm/inch**



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## HB56UW272EJN Series, HB56UW264EJN Series

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# HITACHI

## Hitachi, Ltd.

Semiconductor & IC Div.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan  
Tel: Tokyo (03) 3270-2111  
Fax: (03) 3270-5109

### For further information write to:

Hitachi Semiconductor  
(America) Inc.  
2000 Sierra Point Parkway  
Brisbane, CA. 94005-1897  
U S A  
Tel: 800-285-1601  
Fax: 303-297-0447

Hitachi Europe GmbH  
Continental Europe  
Dornacher Straße 3  
D-85622 Feldkirchen  
München  
Tel: 089-9 91 80-0  
Fax: 089-9 29 30-00

Hitachi Europe Ltd.  
Electronic Components Div.  
Northern Europe Headquarters  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA  
United Kingdom  
Tel: 01628-585000  
Fax: 01628-585160

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 049318  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.  
Unit 706, North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon  
Hong Kong  
Tel: 27359218  
Fax: 27306071

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## HB56UW272EJN Series, HB56UW264EJN Series

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