

V9958

(E-VDP-II)

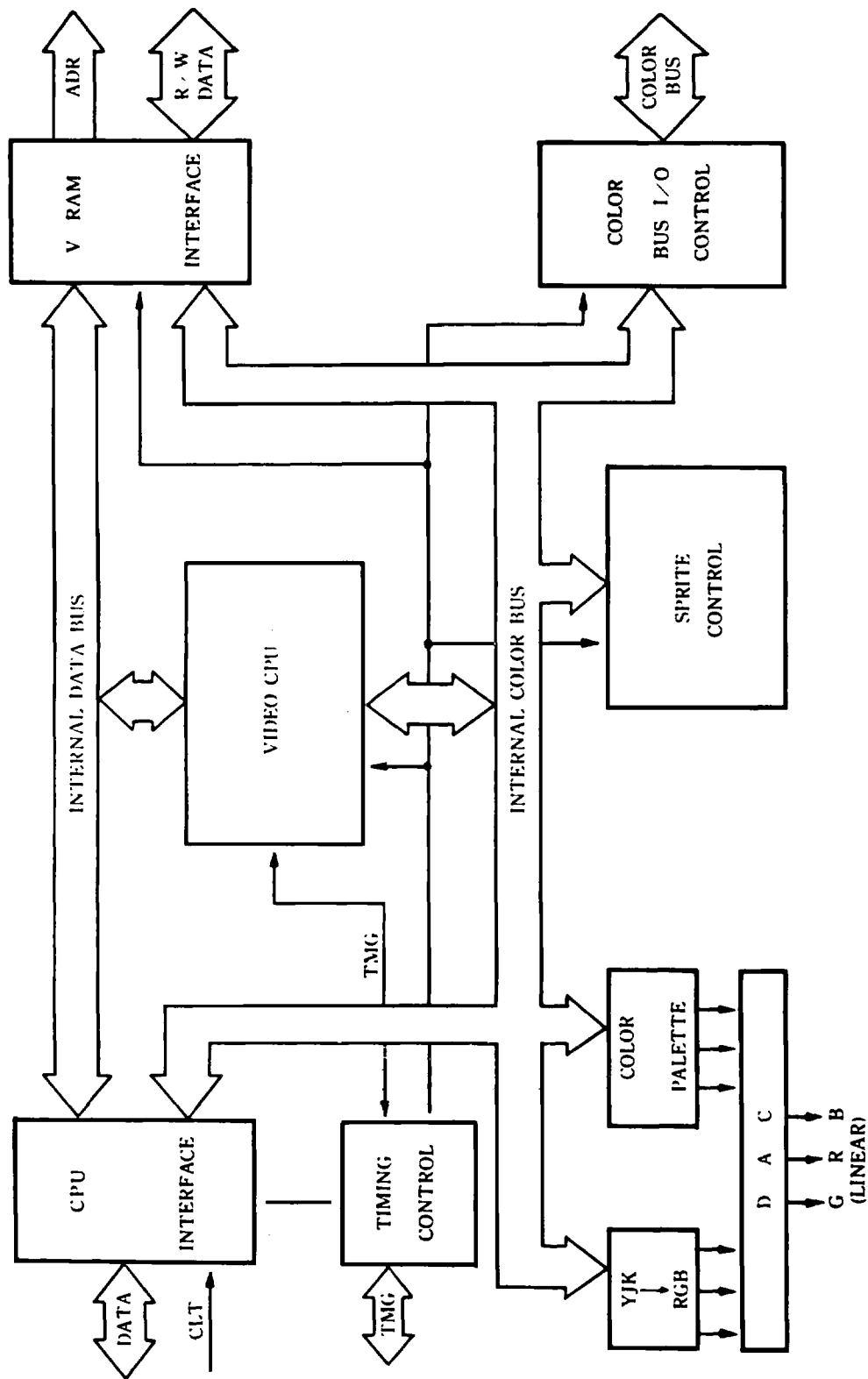
■ GENERAL DESCRIPTION

V9958 (E-VDP-II) is a video display processor (VDP) using an N-channel silicon gate MOS and a 64-pin shrink DIL plastic package. It is software compatible with TMS9918A and V9938.

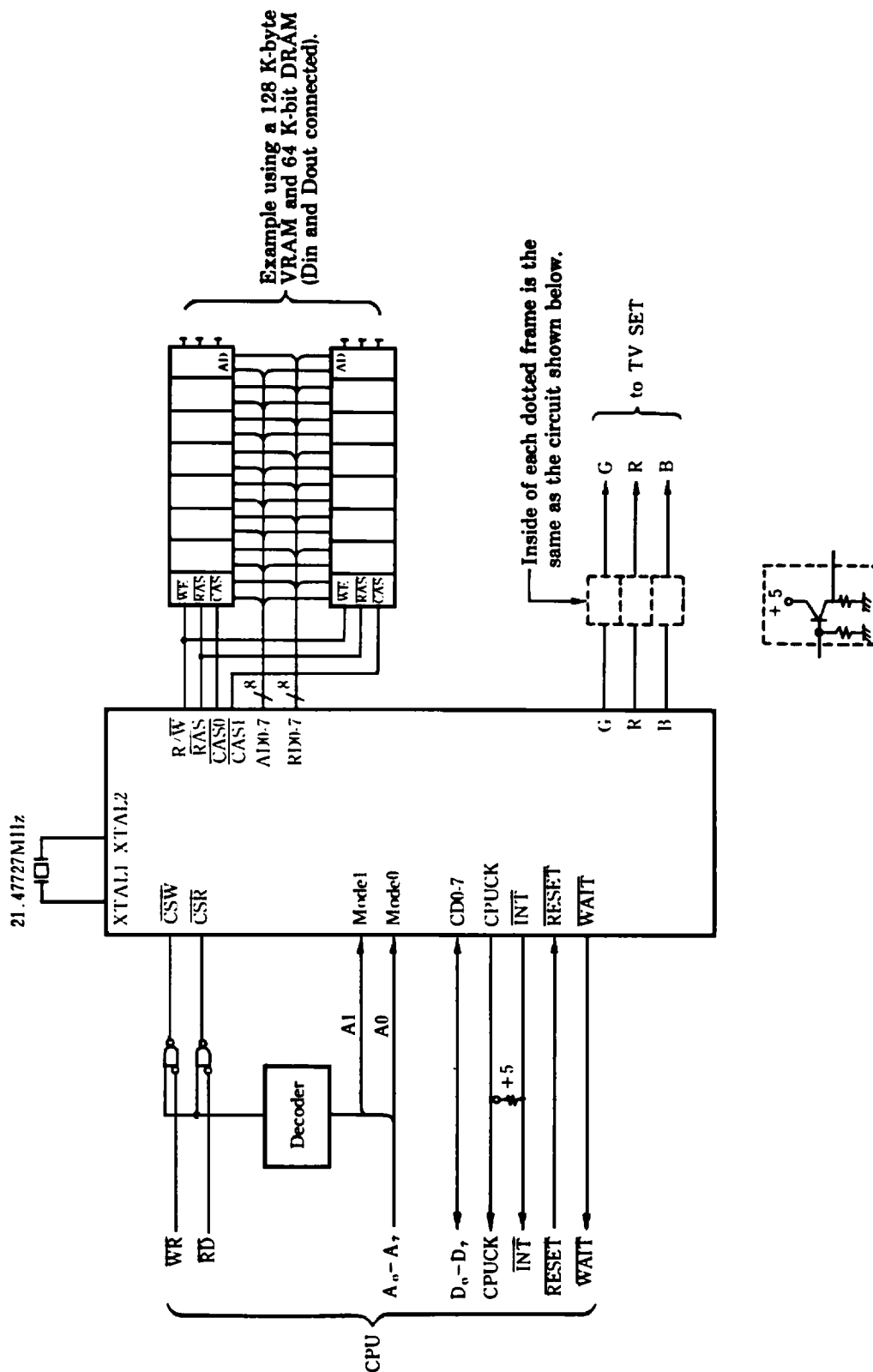
■ FEATURES

- 5V power supply.
- Outputs linear RGB.
- Built-in color palette for display in up to 512 colors.
- Capable of simultaneous display of 19268 colors by using YJK system display.
- Capable of displaying up to 512 × 424 pixels and 16 colors.
- Bit mapped graphics.
- Capable of displaying maximum of 256 colors simultaneously.
- 16K byte ~ 128K byte useable for display memory.
- 16K × 1b, 16K × 4b, 64K × 1b and 64K × 4b DRAMs are useable.
- 256 addresses, 4ms auto refresh function of DRAM.
- Expansion video memory can be connected.
- Eight sprites can be displayed for each horizontal line.
- Colors for sprites can be specified for each horizontal line.
- Area move, line, search and other commands.
- Command function usable in every display mode.
- Logical operation function.
- Addresses can be specified by coordinates.
- Capable of external synchronization.
- Capable of superimposition.
- Capable of digitization.
- Multi E-VDP-II configurations are possible.
- External color palettes can be added by utilizing color-bus output.
- Vertical and horizontal scroll function.
- Wait function to CPU.

■ E-VDP-II BLOCK DIAGRAM



■ E-VDP-II CIRCUIT DIAGRAM



■ PIN LAYOUT AND FUNCTIONS

Pin Name	Pin No.	I/O	Function
CD0 LSB	40	I/O	CPU data bus
CD1	39	I/O	"
CD2	38	I/O	"
CD3	37	I/O	"
CD4	36	I/O	"
CD5	35	I/O	"
CD6	34	I/O	"
CD7 MSB	32	I/O	"
MODE 0	29	I	CPU interface-mode select
MODE 1	28	I	"
$\overline{\text{CSR}}$	31	I	CPU-VDP read strobe
$\overline{\text{CSW}}$	30	I	CPU-VDP write strobe
RD0 LSB	41	I/O	VRAM data bus
RD1	42	I/O	"
RD2	43	I/O	"
RD3	44	I/O	"
RD4	45	I/O	"
RD5	46	I/O	"
RD6	47	I/O	"
RD7 MSB	48	I/O	"
AD0 LSB	49	O	VRAM address bus
AD1	50	O	"
AD2	51	O	"
AD3	52	O	"
AD4	53	O	"
AD5	54	O	"
AD6	55	O	"
AD7 MSB	56	O	"
$\overline{\text{RAS}}$	62	O	VRAM row address strobe
$\overline{\text{CAS 0}}$	61	O	VRAM column address strobe 0 (first half of VRAM)
$\overline{\text{CAS 1}}$	60	O	VRAM column address strobe 1 (last half of VRAM)
$\overline{\text{CAS X}}$	59	O	VRAM column address strobe X (for expansion VRAM)
$\overline{\text{R/W}}$	57	O	VRAM write strobe
G	22	O	Linear RGB signal output
R	23	O	"
B	24	O	"
$\overline{\text{YS}}$	10	O	Signal for switching between VDP RGB output and external video signals. (For superimpose) $\overline{\text{YS}}$ - High; VDP output is transparent $\overline{\text{YS}}$ - Low; VDP output is not transparent
BLEO	7	O	Indicates No. 1 field/No. 2 field blanking with 3-value output. Open drain output High ; No. 2 field and active. Middle; No. 1 field and active. Low ; Linear erase interval.

GND	1	64	XTAL 2
DHCLK	2	63	XTAL 1
DLCLK	3	62	RAS
VRESET	4	61	CAS 0
HSYNC	5	60	CAS 1
CSYNC	6	59	CAS X
BLEO	7	58	VDD
CPUCLK/VDS	8	57	R/W
RESET	9	56	AD 7
YS	10	55	AD 6
CBDP	11	54	AD 5
C7	12	53	AD 4
C6	13	52	AD 3
C5	14	51	AD 2
C4	15	50	AD 1
C3	16	49	AD 0
C2	17	48	RD 7
C1	18	47	RD 6
C0	19	46	RD 5
GND/DAC	20	45	RD 4
VDD/DAC	21	44	RD 3
G	22	43	RD 2
R	23	42	RD 1
B	24	41	RD 0
INT	25	40	CD 0
WAIT	26	39	CD 1
HRESET	27	38	CD 2
MODE 1	28	37	CD 3
MODE 0	29	36	CD 4
CSW	30	35	CD 5
CSR	31	34	CD 6
CD7	32	33	VBB

Pin Name	Pin No.	I/O	Function
HSYNC	5	O	High: Timing other than HSYNC or color burst timing. Low : HSYNC or timing other than color burst.
<u>CSYNC</u>	6	O	Composite SYNC output.
CBDR	11	O	Indicates color bus direction. High: Color bus is input Low : Color bus is output
C0 LSB	19	I/O	Color bus.
C1	18	I/O	Normally color code is output. Used as input port when digitizing.
C2	17	I/O	"
C3	16	I/O	"
C4	15	I/O	"
C5	14	I/O	"
C6	13	I/O	"
C7 MSB	12	I/O	"
<u>DHCLK</u>	2	O	Dot clock output at high resolution. Approx. 10.74MHz open drain output.
<u>DLCLK</u>	3	I/O	Dot clock output at low resolution. Approx. 5.37MHz open drain output. As input is also possible by using the mode register, it is used for multi VDP.
XTAL 1	63	I	Used for XTAL connection. Also used for input when using an externally generated clock.
XTAL 2	64	I	
CPUCLK/ VDS	8	O	1/6 of XTAL frequency is output. VRAM data select <u>VDS</u> - Low : VRAM access for display data. <u>VDS</u> - High: VRAM access for other than the above.
<u>INT</u>	25	O	CPU interrupt output, open drain output Low: Generates interrupt.
<u>RESET</u>	9	I	Each circuit in VDP is initial reset.
<u>VRESET</u>	4	I	VSYNC input.
<u>HRESET</u>	27	I	HSYNC input.
<u>WAIT</u>	26	O	Wait signal to CPU is output.
VDD	58	I	5V power supply.
GND	1	I	Ground 0V.
GND•DAC	20	I	Ground 0V.
VDD•DAC	21	I	5V power supply.
VBB	33	O	Baseboard voltage.

ELECTRICAL CHARACTERISTICS

1. Maximum Ratings

Symbol	Item	Rating	Unit
V _{DD}	Power supply voltage	-0.5 - +7.0	V
V _{in}	Input voltage	-0.5 - +7.0	V
T _{stg}	Storage temperature	-50 ~ +125	°C
Top	Operating temperature	0 - +70	°C

2. Recommended Operating Conditions

Symbol	Item	Minimum	Typical	Maximum	Unit
V _{DD}	Power supply voltage	4.75	5.00	5.25	V
V _{SS}	Power supply voltage		0		V
Top	Operating ambient temperature	0		70	°C
V _{IL 1}	Low level input voltage (group 1)	-0.3		0.8	V
V _{IL 2}	Low level input voltage (group 2)	-0.3		0.8	V
V _{IL 3}	External clock low level input voltage (group 3)	-0.3		0.8	V
V _{IH 1}	High level input voltage (group 1)	2.2		V _{DD}	V
V _{IH 2}	High level input voltage (group 2)	2.2		V _{DD}	V
V _{IH 3}	External clock high level input voltage (group 3)	3.5		V _{DD}	V

Note: Group 1 CS_R, RD0-7, C0-7, LPS, LPD, RESET, DLCLK, VRESET, HRESET
 Group 2 CD0-7, MODE 0, MODE 1, CSW
 Group 3 XTAL 1, XTAL 2

3. DC Characteristics

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
V _{OL 4}	Low level output voltage (group 4)	I _{OL} = 1.6mA			0.4	V
V _{OL 5}	Low level output voltage (group 5)	I _{OL} = 1.6mA			0.4	V
V _{OL 6}	Low level output voltage (group 6)	I _{OL} = 10mA			0.4	V
V _{OL 7}	Low level output voltage (group 7)	I _{OL} = 1.6mA			0.4	V
V _{OH 4}	High level output voltage (group 4)	I _{OH} = 100μA	2.4			V
V _{OH 5}	High level output voltage (group 5)	I _{OH} = 60μA	2.7			V
I _{LI}	Input leak current				10	μA
I _{LO}	Output leak current (when floating)				25	μA
I _{DD}	Current consumption				230	mA

Note: Group 4 CD0-7, RD0-7, AD0-7, VDS, CBDR, CPUCLK/VDS, C0-7, HSYNC, CSYNC, WAIT, YS
 Group 5 RAS, CAS 0, CAS 1, CASX, R/W
 Group 6 DLCLK, DHCLK
 Group 7 INT

4. R.G.B. Output Level

Symbol	Item	Measurement Conditions	Minimum	Typical	Maximum	Unit
VRGB 31	R.G.B. maximum output voltage	RL = 470Ω	2.8	3.1	3.5	V
VRGB 0	R.G.B. minimum output voltage (black level)		1.9	2.2	2.5	V
VP-P	R.G.B. VRGB31-VRGB0 potential difference		0.8	0.9	1.1	V
DRGB	R.G.B. VP-P deviation				5.0	%

*Typical values are given under conditions of V_{DD} = 5.00V, T_A = 25°C.

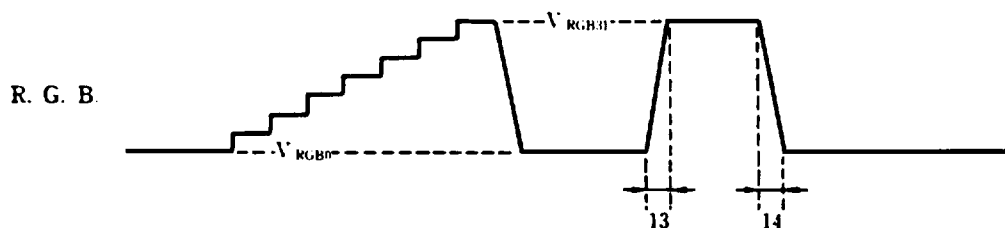
5. Sync Signal Output Level

Symbol	Item	Measurement Conditions	Minimum	Typical	Maximum	Unit
VTLVH 1	3-value output high level BLEO	RL = 1KΩ	4.5		V _{DD}	V
VTLVM 1	3-value output intermediate level BLEO		2.5		3.5	V
VTLVL 1	3-value output low level BLEO				0.4	V

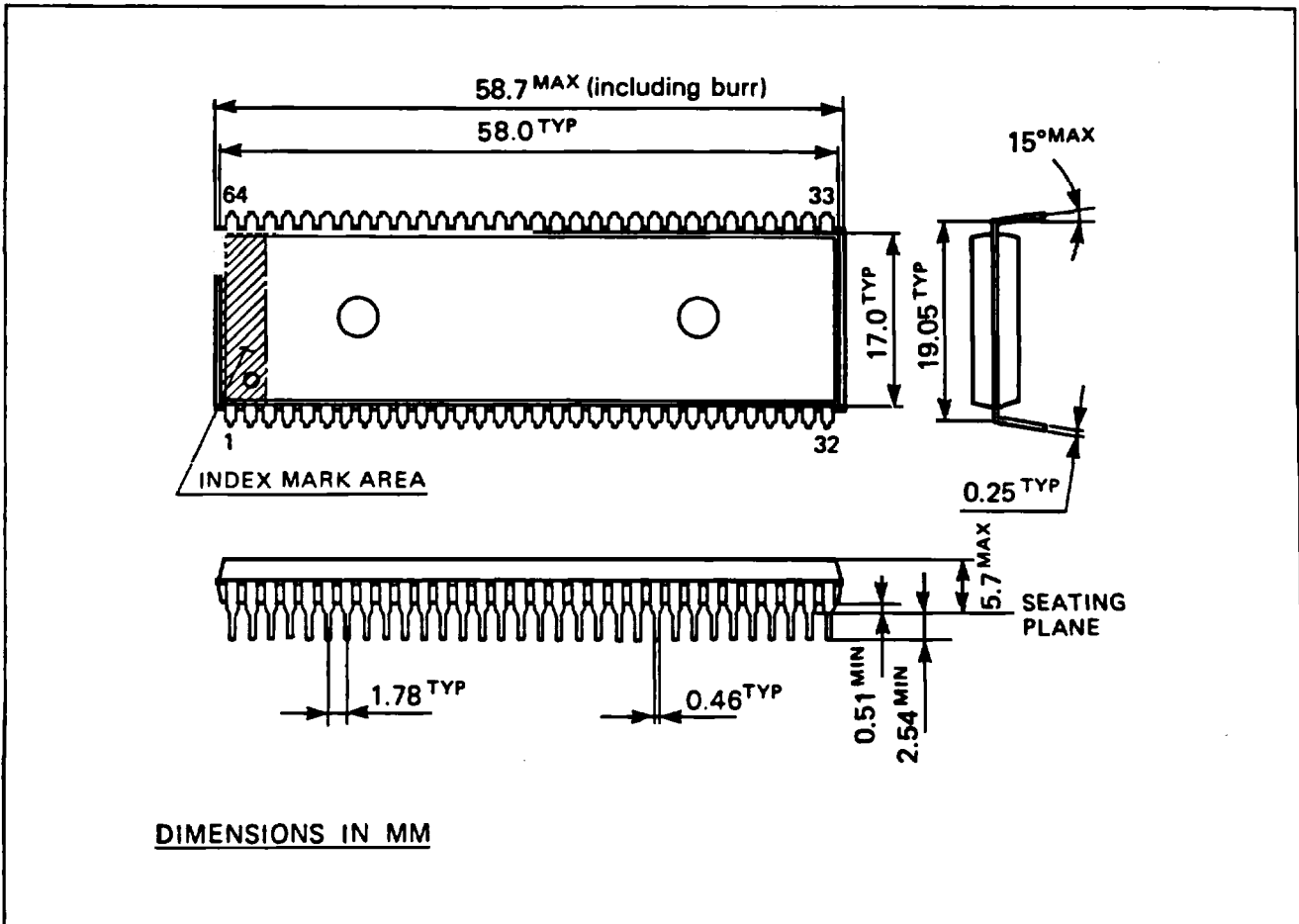
6. R.G.B. Signal AC Characteristics

No.	Symbol	Item	Measurement Conditions	Minimum	Typical	Maximum	Unit
13	TrRGB	R.G.B. signal rise time (VRGB0 → VRGB31)	RL = 470Ω CL = 150pF			60	ns
14	TfRGB	R.G.B. signal fall time (VRGB31 → VRGB0)				60	ns

Note) Measurement is 10% - 90%



■ PACKAGE DIMENSIONAL DIAGRAM



The specifications of this product are subject to improvement changes without prior notice.

AGENCY

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