

TOSHIBA MOS MEMORY PRODUCTS

1,048,576 WORD × 1 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM411000C-10

TMM411000C-12

PRELIMINARY

DESCRIPTION

The TMM411000C is the new generation dynamic RAM organized 1,048,576 words by 1 bit, it is successor to the industry standard TMM41256P. The TMM411000C utilizes TOSHIBA's N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TMM411000C to be packaged in a standard 18 pin

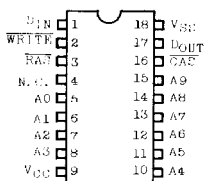
ceramic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. In addition to the \overline{RAS} only refresh mode, a \overline{CAS} before \overline{RAS} automatic refresh is available.

FEATURES

- 1,048,576 words by 1 bit organization
- Fast access time and cycle time
- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator
- Low Power :
385mW Operating(MAX.) (TMM411000C-10)
330mW Operating(MAX.) (TMM411000C-12)

- 22mW Standby(MAX.)
- Industry standard 18 pin ceramic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, \overline{CAS} before \overline{RAS} refresh, \overline{RAS} only refresh, Hidden refresh, and Page Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms

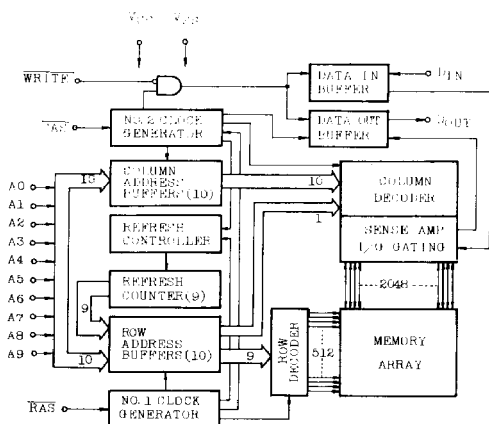
PIN CONNECTION (TOP VIEW)



PIN NAMES

A ₀ ~A ₉	Address Inputs
CAS	Column Address Strobe
DIN	Data In
DOUT	Data Out
RAS	Row Address Strobe
WRITE	Read/Write Input
V _{CC}	Power (+5V)
V _{SS}	Ground
N. C.	No Connection

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature-Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	1	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	2
V_{IL}	Input Low Voltage	1.0	—	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (Vcc=5V±10%, Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling : $t_{RC}=t_{RC\ MIN.}$)	TMM411000C-10	—	70	mA	3,4
		TMM411000C-12	—	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current (RAS=CAS= V_{IH})	—	4	mA		
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS= V_{IH} : $t_{RC}=t_{RC\ MIN.}$)	TMM411000C-10	—	55	mA	3
		TMM411000C-12	—	50		
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, PAGE Mode (RAS= V_{IL} , CAS Cycling : $t_{RC}=t_{RC\ MIN.}$)	TMM411000C-10	—	55	mA	3,4
		TMM411000C-12	—	50		
I_{CC5}	CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, CAS Before RAS Mode (RAS Cycling, CAS Before RAS : $t_{RC}=t_{RC\ MIN.}$)	TMM411000C-10	—	55	mA	3
		TMM411000C-12	—	50		
I_{IL1}	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test =0V)	-10	10	μA		
I_{OL1}	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$)	-10	10	μA		
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$)	2.4	—	V		
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$)	—	0.4	V		

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM411000C-10		TMM411000C-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read or Write Cycle Time	190	—	220	—	ns	
t _{RWC}	Read-Write Cycle Time	210	—	240	—	ns	
t _{RMW}	Read-Modify-Write Cycle Time	225	—	260	—	ns	
t _{PC}	Page Mode Cycle Time	100	—	120	—	ns	
t _{RAC}	Access Time from RAS	—	100	—	120	ns	8, 10
t _{CAC}	Access Time from CAS	—	50	—	60	ns	9, 10
t _{OFF}	Output Buffer Turn-Off Delay	5	30	5	35	ns	11
t _I	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t _{RP}	RAS Precharge Time	80	—	90	—	ns	
t _{RAS}	RAS Pulse Width	100	10,000	120	10,000	ns	
t _{RSH}	RAS Hold Time	50	—	60	—	ns	
t _{CSH}	CAS Hold Time	100	—	120	—	ns	
t _{CAS}	CAS Pulse Width	50	10,000	60	10,000	ns	
t _{RCD}	RAS to CAS Delay Time	20	50	25	60	ns	13
t _{CRP}	CAS to RAS Precharge Time	10	—	10	—	ns	
t _{CPN}	CAS Precharge Time	20	—	25	—	ns	
t _{CP}	CAS Precharge Time (Page mode only)	40	—	50	—	ns	
t _{ASR}	Row Address Set-Up Time	0	—	0	—	ns	
t _{RAH}	Row Address Hold Time	10	—	15	—	ns	
t _{ASC}	Column Address Set-Up Time	0	—	0	—	ns	
t _{CAH}	Column Address Hold Time	20	—	25	—	ns	
t _{AR}	Column Address Hold Time Reference to RAS	70	—	85	—	ns	
t _{RCS}	Read Command Set-Up Time	0	—	0	—	ns	
t _{RCH}	Read Command Hold Time Reference to CAS	0	—	0	—	ns	12
t _{RRH}	Read Command Hold Time Reference to RAS	10	—	15	—	ns	12
t _{WCH}	Write Command Hold Time	20	—	25	—	ns	
t _{WCR}	Write Command Hold Time Reference to RAS	70	—	85	—	ns	
t _{WP}	Write Command Pulse Width	20	—	25	—	ns	
t _{RWL}	Write Command to RAS Lead Time	30	—	35	—	ns	
t _{CWL}	Write Command to CAS Lead Time	30	—	35	—	ns	
t _{DS}	Data-In Set-Up Time	0	—	0	—	ns	14
t _{DH}	Data-In Hold Time	20	—	25	—	ns	14
t _{DHR}	Data-In Hold Time Reference to RAS	70	—	85	—	ns	
t _{REF}	Refresh Period	—	8	—	8	ms	
t _{WCS}	Write Command Set-Up Time	-5	—	-5	—	ns	15
t _{CWD}	CAS to WRITE Delay	35	—	40	—	ns	15
t _{RWD}	RAS to WRITE Delay	85	—	100	—	ns	15
t _{CSR}	CAS Set-up Time (CAS before RAS)	10	—	10	—	ns	
t _{CHR}	CAS Hold Time (CAS before RAS)	30	—	30	—	ns	
t _{RPC}	RAS Precharge to CAS Active Time	0	—	0	—	ns	
t _{CPT}	CAS Precharge Time (CAS before RAS Counter Test)	40	—	50	—	ns	

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CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70 C)

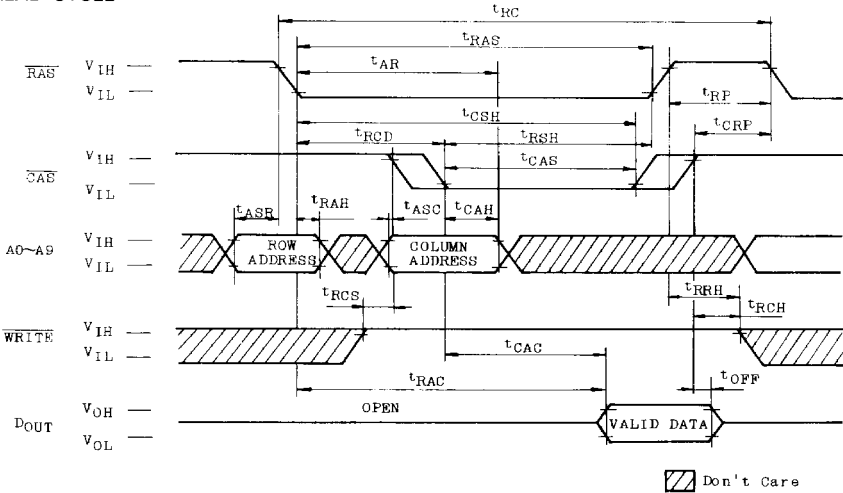
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _i	Input Capacitance (A ₀ ~A ₄ , D ₀)	—	6	pF
C _i	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WRITE}}$)	—	7	pF
C _o	Output Capacitance (D ₀ ~D ₄)	—	7	pF

NOTES:

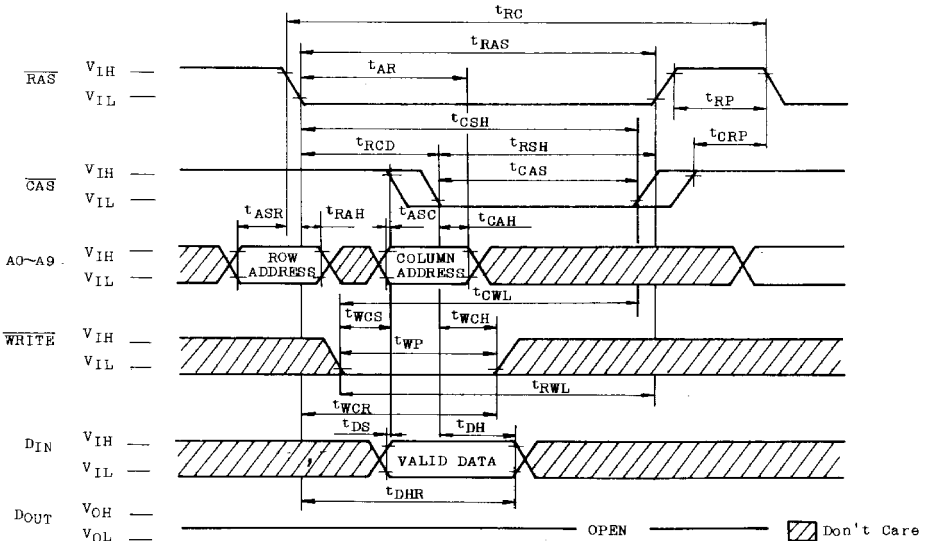
- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltages are referenced to V_{SS}.
- t_{CE1}, t_{CC3}, t_{CC4}, t_{CC5} depend on cycle rate.
- t_{CE1}, t_{CC3} depend on output loading. Specified values are obtained with the output open.
- An initial pause of 200μs is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
- AC measurements assume t_r = 5ns.
- V_{IH(min.)} and V_{IL(max.)} are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- Assumes that t_{RCO} ≤ t_{RCO(max.)}. If t_{RCO} is greater than the maximum recommended value shown in this table, t_{RCO} will increase by the amount that t_{RCO} exceeds the value shown.
- Assume that t_{RCO} ≥ t_{RCO(max.)}.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- t_{OFF(max.)} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- Operation within the t_{RCO(max.)} limit insures that t_{RCO(max.)} can be met.
t_{RCO(max.)} is specified as a reference point only: If t_{RCO} is greater than the specified t_{RCO(max.)} limit, then access time is controlled exclusively by t_{CAC}.
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in read-write or read-modify-write cycles.
- t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS(min.)}, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If t_{CWD} ≥ t_{CWD(min.)} and t_{RWD} ≥ t_{RWD(min.)}, the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

● READ CYCLE

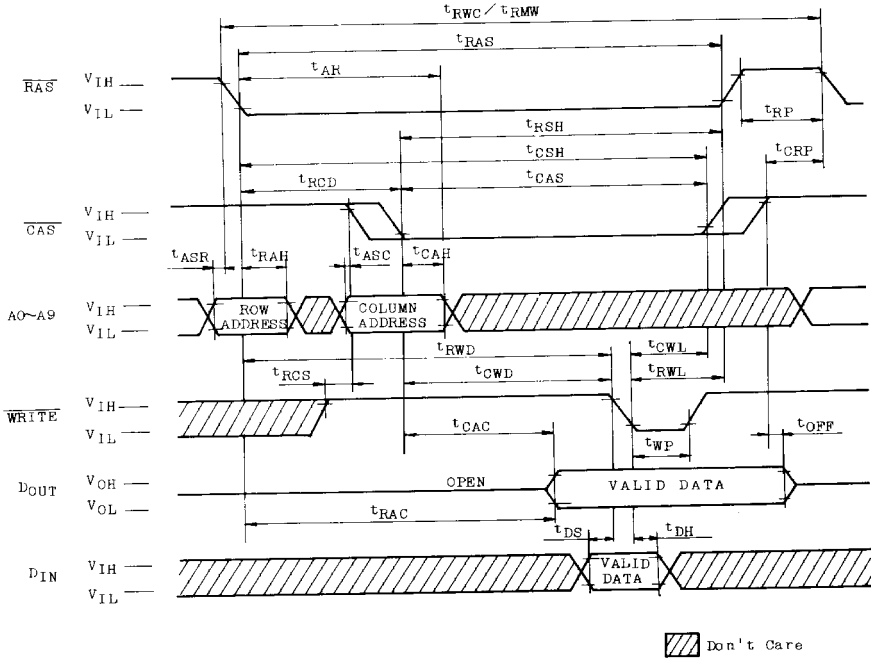


● WRITE CYCLE (EARLY WRITE)

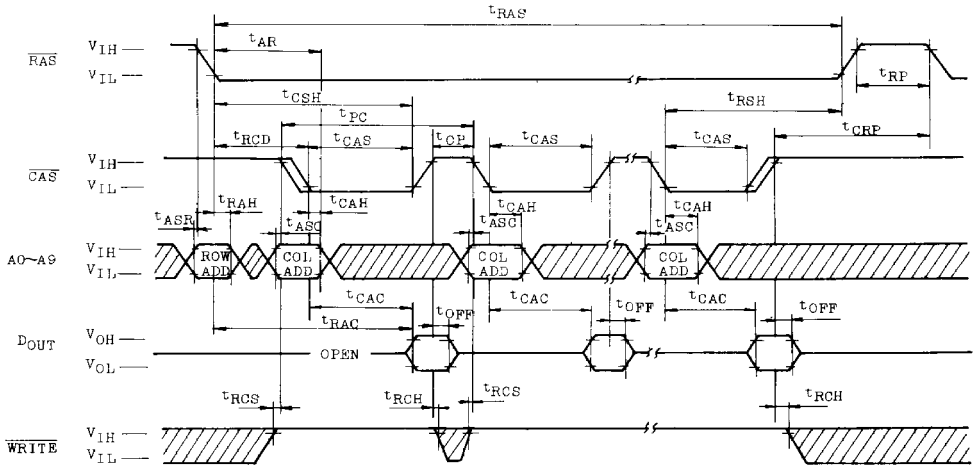


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● READ-WRITE/READ-MODIFY-WRITE CYCLE

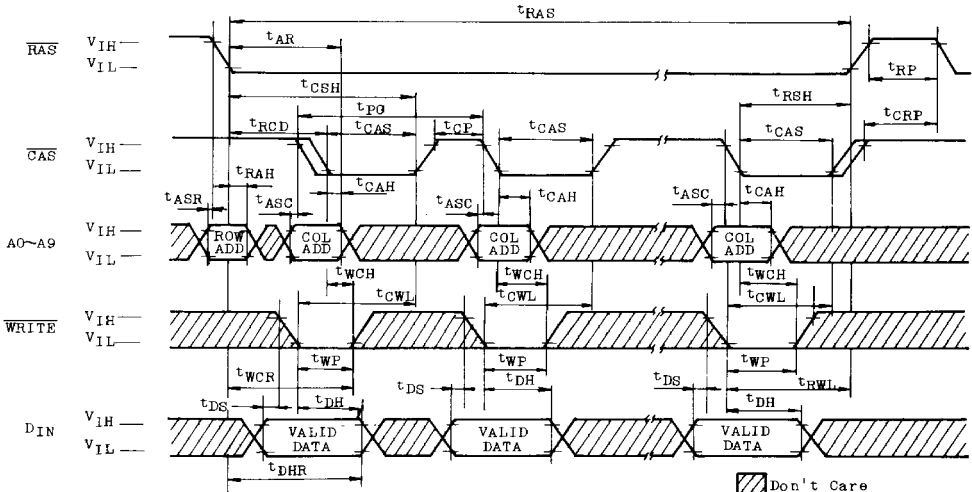


● PAGE MODE READ CYCLE



▨ Don't Care

● PAGE MODE WRITE CYCLE

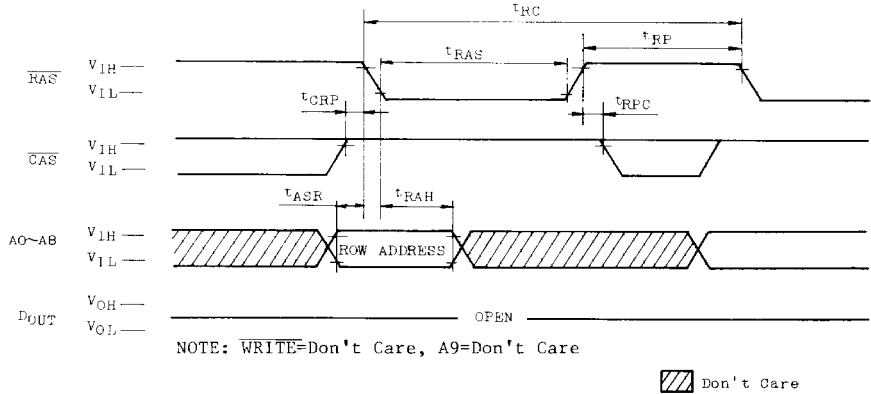


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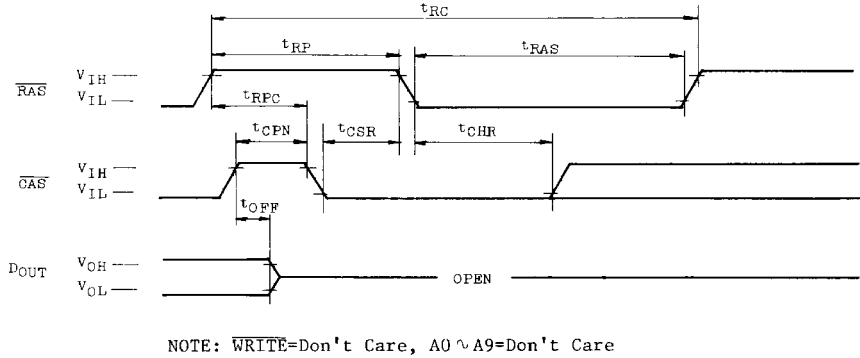
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● $\overline{\text{RAS}}$ ONLY REFRESH CYCLE



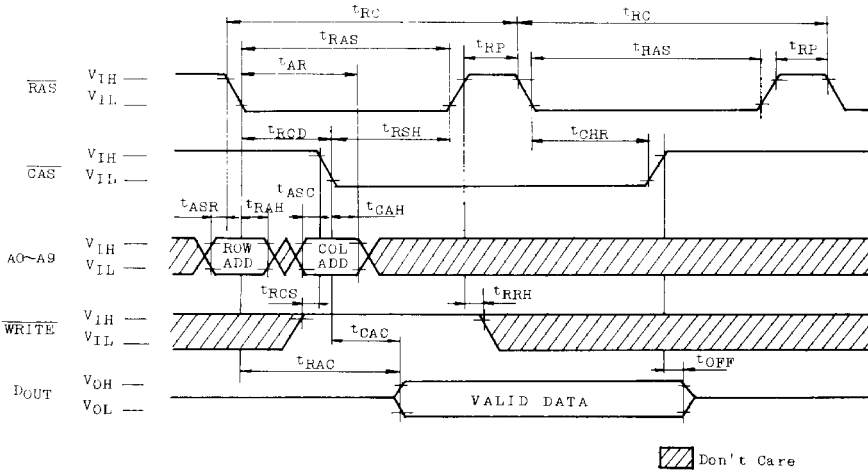
● $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



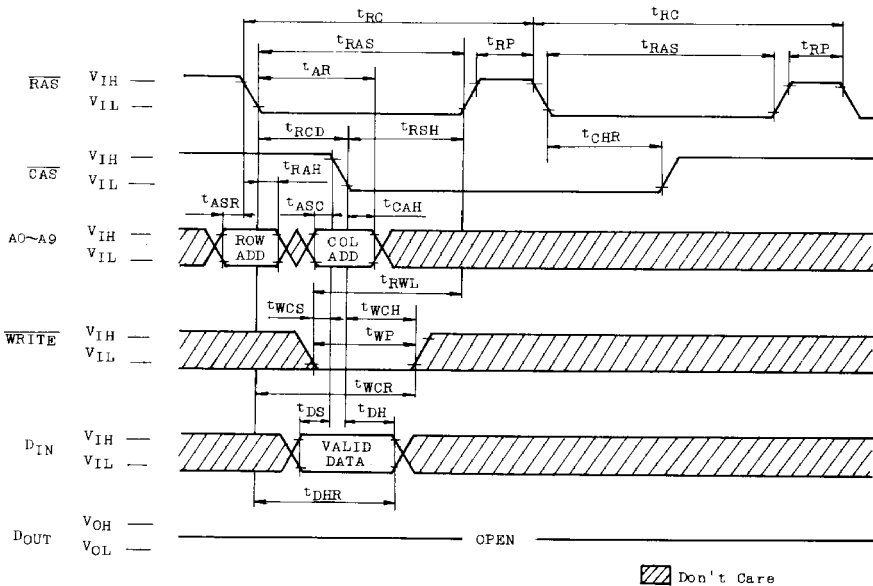
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● HIDDEN REFRESH CYCLE (READ)



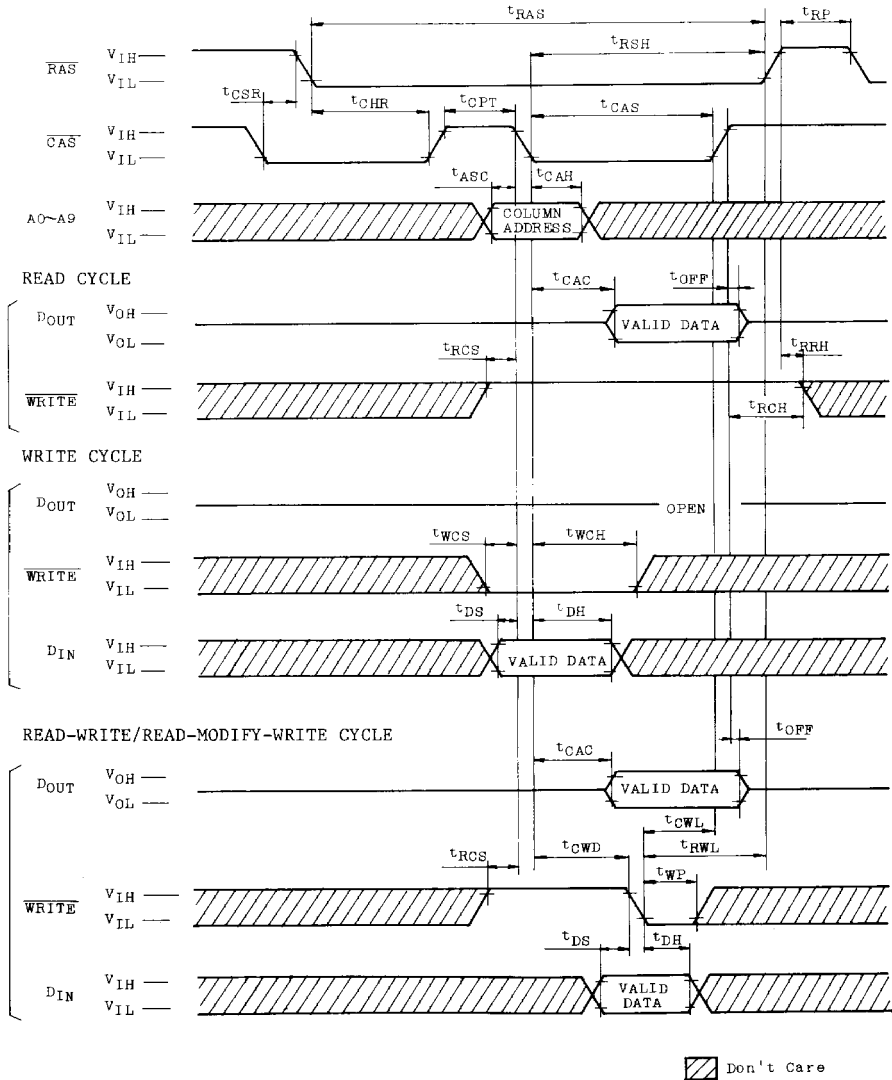
● HIDDEN REFRESH CYCLE (WRITE)



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• CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION**ADDRESSING**

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TMM411000C are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{\text{RAS}}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{\text{CAS}}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{\text{RAS}}$, and $\overline{\text{CAS}}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{\text{CAS}}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. This "gated $\overline{\text{CAS}}$ " feature allows the $\overline{\text{CAS}}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{\text{WRITE}}$ and $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ is active. The later of the signals ($\overline{\text{WRITE}}$ or $\overline{\text{CAS}}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{\text{WRITE}}$ input is brought low (active) prior to $\overline{\text{CAS}}$, the D_{IN} is strobed by $\overline{\text{CAS}}$ and the set-up and hold times are referenced to $\overline{\text{CAS}}$. If the input data is not available at $\overline{\text{CAS}}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{\text{WRITE}}$ signal will be delayed until after $\overline{\text{CAS}}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{\text{WRITE}}$ rather than $\overline{\text{CAS}}$. (To illustrate this feature, D_{IN} is referenced to $\overline{\text{WRITE}}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{\text{CAS}}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{\text{WRITE}}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{\text{CAS}}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM411000C is the high impedance (open circuit) state. This is to say, anytime $\overline{\text{CAS}}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{\text{CAS}}$ is taken back to the inactive (high level) condition.

PAGE MODE

The "Page-Mode" feature of the TMM411000C allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{\text{RAS}}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

 $\overline{\text{RAS}}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address ($\text{A}_0 \sim \text{A}_8$) within each 8 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with " $\overline{\text{RAS}}$ -only" cycles, $\overline{\text{RAS}}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

 $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

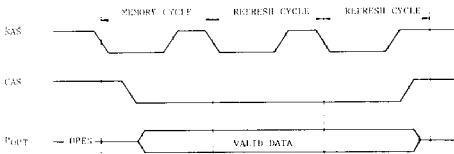
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing available on the TMM411000C offers an alternate refresh method. If $\overline{\text{CAS}}$ is held on low for the specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation.

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HIDDEN REFRESH

An optional feature of the TMM411000C is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding CAS at V_{IL} and taking RAS high and after a specified precharge period (t_{RP}), executing a CAS before RAS refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

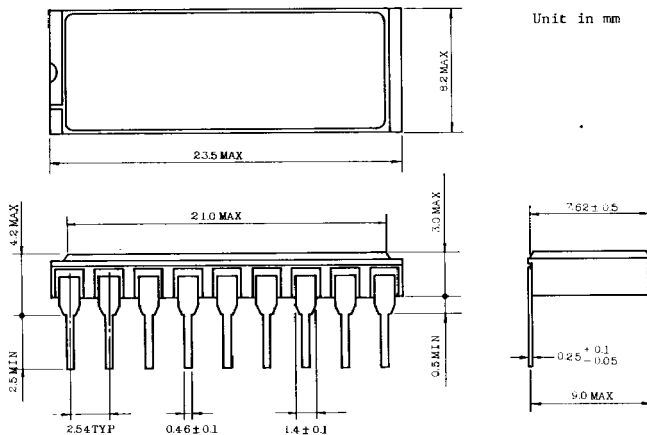
CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh operation of TMM411000C can be tested by CAS BEFORE RAS REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 CAS before RAS cycles as initialization cycles. The test procedure is as follows.

- ① Write "0" into all the memory cells at normal write mode.
- ② Select one certain column address and read "0" out and write "1" in each cell by performing CAS BEFORE RAS REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.
- ③ Check "1" out of 512 bits at normal read mode, which was written at ②.
- ④ Using the same column as ②, read "1" out and write "0" in each cell performing CAS BEFORE RAS REFRESH COUNTER TEST. Repeat this operation 512 times.
- ⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.
- ⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS



NOTE : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads. All dimensions are in millimeters.
All dimensions are in millimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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