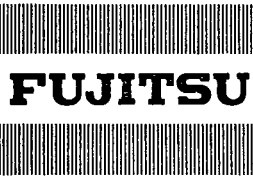


T-51-07-01



**6-CHANNEL 8-BIT
A/D CONVERTER
SUBSYSTEM**

**MB 4053
MB 4063**

May 1986
Edition 3.0

6-CHANNEL 8-BIT A/D CONVERTER SUBSYSTEM

The Fujitsu MB 4053 and MB 4063 are 6-channel, 8-bit, single-slope A/D converter subsystem designed to be used in a microprocessor based data control system. These devices provide the analog functions while the addressing, counting and timing functions are provided by a microprocessor such as the MB 8840/50, MBL 8048, MBL 8086, or MBL 8088.

The MB 4053 and MB 4063 are single monolithic bipolar IC providing a 1 of 8 address decoder, 8-channel analog multiplier, sample and hold, constant current generator, ramp integrator and comparator in a 16-pin package.

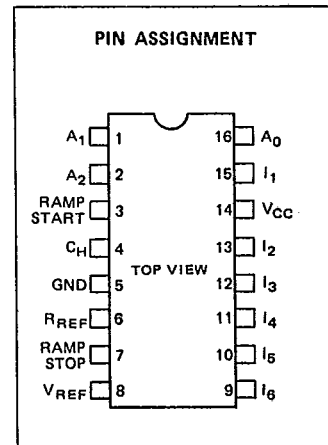
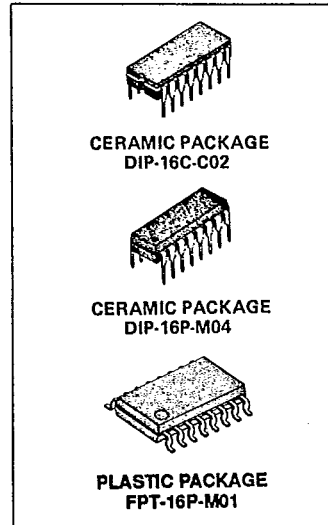
These A/D converter subsystems are suitable for a wide range of applications. The resolution required by an application can be obtained by arbitrarily selecting a suitable integration time. Also zero offset and full-scale error corrections can be made automatically (auto-zero and auto-calibration) to minimize conversion error.

- Microprocessor/TTL compatible
- Zero offset and full-scale error correction capability
- Ratiometric conversion capability
- Available in 16-pin DIP and Flat Pack
- Compatible with MC14443 and μ A9708 (DIP package)
- Single power supply : +4.75 V to +15 V
- Excellent linearity : $\pm 0.2\%$ max. error
- Fast conversion time : 300 μ s/ch typ.
- Analog input voltage : 0 V to $V_{CC} - 2$ V (5.25 V max.)
- Power Dissipation : 25 mW typ. at $V_{CC} = 5$ V
- Standard 16-pin DIP or flat package.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	
Supply Voltage	V_{CC}	18	V	
Digital Input Voltage	V_{ID}	-0.5 to +30	V	
Digital Output Voltage when Off	V_{OH}	-0.5 to +18	V	
Analog Input Voltage	V_{IA}	-0.5 to +30	V	
Output Current	I_O	10	mA	
Storage Temperature	Ceramic	T_{STG}	-55 to +150	$^{\circ}$ C
	Plastic		-55 to +125	$^{\circ}$ C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 1a - MB 4053 BLOCK DIAGRAM

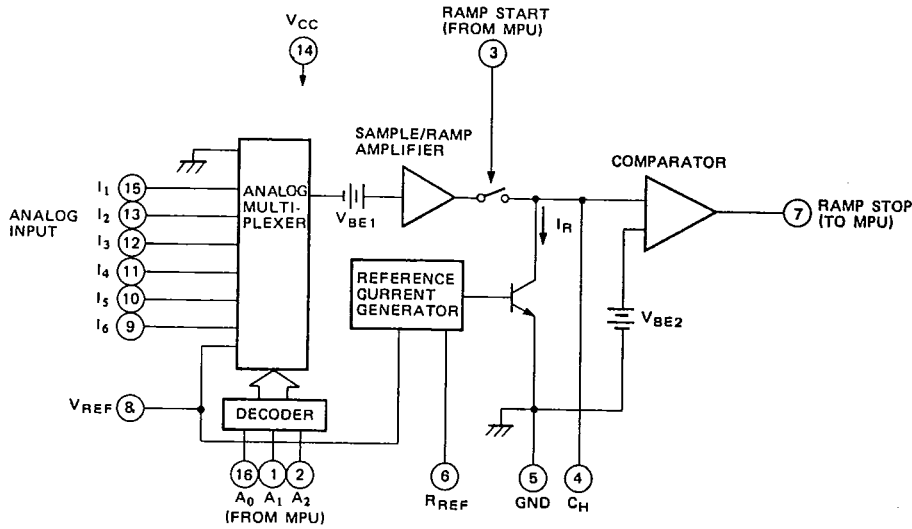
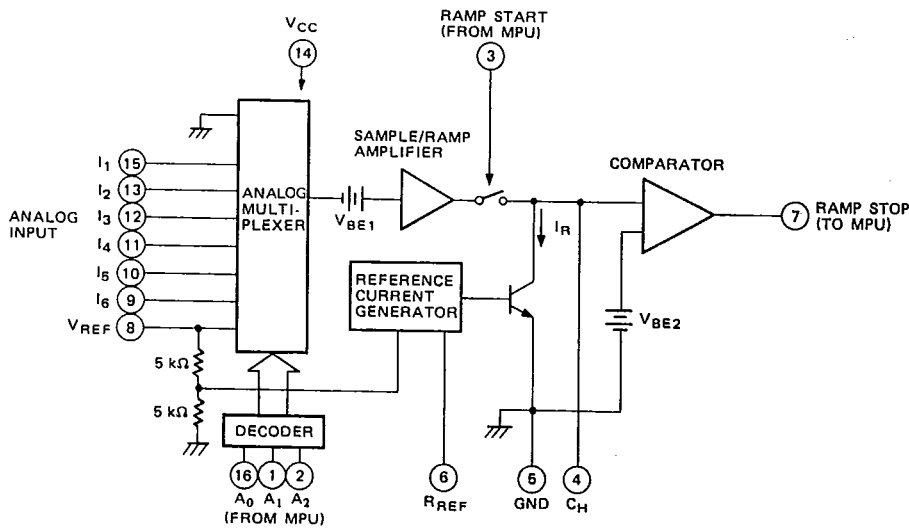


Fig. 1b - MB 4063 BLOCK DIAGRAM



T-51-07-01

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MB 4063

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition			Unit
		Min.	Typ.	Max.	
Supply Voltage	V _{CC}	4.75	5.0	15	V
Reference Voltage*	MB 4053	2.0		5.25	V
	MB 4063	2.8			
Ramp Capacity	C _H	300			pF
Reference Current	I _R	12		50	μA
Analog Input Voltage	V _{IA}	0		V _{REF}	V
Output Current	I _O			1.6	mA
Operating Temperature	T _A	-40		+85	°C

NOTE: *2V ≤ V_{REF} ≤ V_{CC} - 2V for MB 4053, 2.8V ≤ V_{REF} ≤ V_{CC} - 2V for MB 4063

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75 V to 15 V, T_A = -40°C to 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Conversion Error	E _A		±0.2	±0.3	%	†1
Linearity Error	E _R		±0.08	±0.2	%	†2
Analog Input Current	I _B		-50	-250	nA	
Crosstalk Between Any Two Channels	V _{CR}	60			dB	†3
Multiplexer Input Offset Voltage	V _{OSM}		2.0	4.0	mV	
Conversion Time	t _C		296	350	μs/ch	See test circuit Analog input: 0 thru V _{REF} C _H = 3300 pF, I _R = 50 μA
Acquisition Time	t _A		20	40	μs	See test circuit C _H = 1000 pF †4
Acquisition Current	I _A	150.			μA	
Ramp Start Delay Time	t _O		100		ns	
Multiplexer Address Time	t _M		1		μs	
Digital High Level Input Voltage	V _{IH}	2.0			V	
Digital Low Level Input Voltage	V _{IL}			0.8	V	
Digital Low Level Input Current	I _{IL}		-5	-15	μA	V _{IL} = 0.4 V
Digital High Level Input Current	I _{IH}			1	μA	V _{IH} = 5.5 V
High Level Output Current	I _{OH}			10	μA	V _{OH} = 15 V
Low Level Output Voltage	V _{OL}			0.4	V	I _{OL} = 1.6 mA
Supply Current	I _{CC}	5	10		mA	

A minus sign (-) prefixing a current value indicates that the current flows from the IC to the external circuit.

†1 Conversion error: For all channels, deviation from a straight line between two points obtained by channel addresses 000 (0 scale) and 111 (full scale).

†2 Linearity error: Deviation from a straight line between the 0 and full scale points for each channel.

†3 Crosstalk between channels: Voltage change V_{CH} of

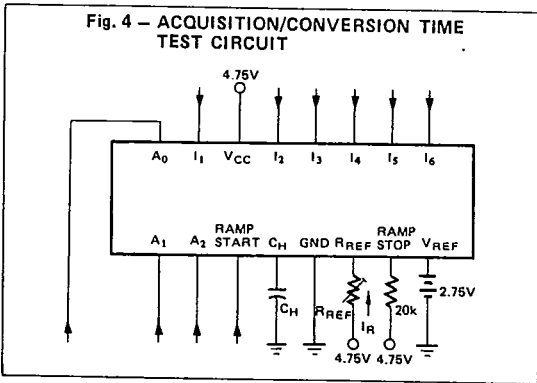
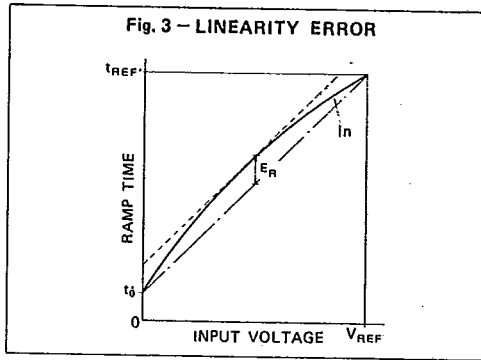
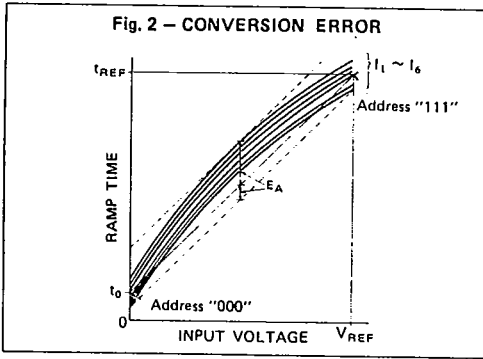
C_H terminal occurring when an input voltage of a channel is changed by ΔV_i while another channel is already charged (RAMP START = 0). This calculated by $20 \log \frac{\Delta V_{CH}}{\Delta V_i}$.

†4 Acquisition time: Sum of multiplexer delay time, RAMP START delay time, and time required to charge the selected input voltage to the ramp capacitor.



T-51-07-01

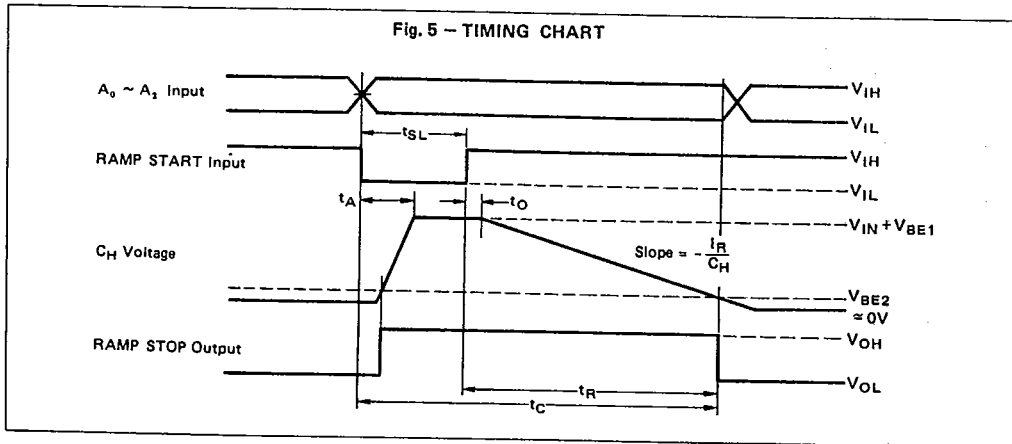
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CHANNEL SELECTION

Input address line			Selected analog input
A ₂	A ₁	A ₀	
0	0	0	GND
0	0	1	I ₁
0	1	0	I ₂
0	1	1	I ₃
1	0	0	I ₄
1	0	1	I ₅
1	1	0	I ₆
1	1	1	V _{REF}

Adjust R_{REF} in the range 40 to 200 kΩ so that I_R is 12 to 50 μA.



T-51-07-01

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OPERATION DISCRIPTION

Refer to Fig. 1 MB 4053/MB 4063 BLOCK DIAGRAM, and Fig. 5 Timing Chart. Address inputs A₀ to A₂ are used to select the analog input to be converted, (one of the six analog inputs I₁ to I₆). The RAMP START input is switched from a logic 1 to a logic zero. This causes the external ramp capacitor C_H to charge at a fixed rate. (Note 1) until it reaches the sum of the selected analog input voltage and a constant offset voltage V_{BE1}. The RAMP STOP output (open-collector switches from a logic 0 to logic 1 when the voltage on C_H reaches the comparator reference voltage V_{BE2}. The RAMP START input is switched back to a logic 1 after C_H is completely charged. This disconnects the analog input from C_H and allows it to be gin discharging at a fixed rate (Note 2). When the voltage on C_H reaches the comparator reference voltage V_{BE2} the RAMP STOP output switches back to a logic 0. This completes a conversion cycle for 1 channel.

The time between the RAMP START input switching (0→1) and RAMP STOP output switching (1→0) is the RAMP TIME t_R. This would be directly proportional to the analog input voltage for the ideal situation where there was no comparator switching level error, leakage, switching delay times or effect of the impedance of the internal reference current source. t_R can be calculated for the ideal case as follows:

$$t_R = V_{IN} \times \frac{C_H}{I_R}$$

- Where: V_{IN} = Analog input voltage to be measured
 C_H = External ramp capacitor
 $I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$ for MB 4053
 $I_R = \frac{V_{REF}}{2 - R_{REF}}$ for MB 4063

This ramp time is converted to a digital representation by counting t_R with the microprocessor. If a small error can be tolerated, the A/D conversion software can be reduced and the conversion time minimized by omitting corrections.

NOTE:

*1 Charge slope = $\frac{I_A - I_R}{C_H} \geq \frac{150\mu A - I_R}{C_H}$

Where: I_A is the acquisition current whose value is determined from the circuit constant in the IC.

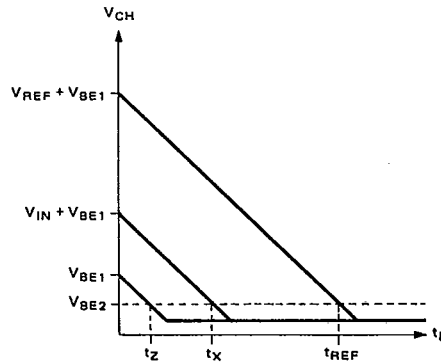
*2 Discharge slope = $-\frac{I_R}{C_H}$

ZERO OFFSET AND FULL-SCALE FACTOR CORRECTIONS

High precision conversions can be achieved by correcting for zero offset and full scale factor as follows:

The channel select address (A₀ to A₂) is set to 000. Ground (GND) is selected (internally) as the analog input and converted. This results in ramp time t_R. Next the address is set to 111. V_{REF} is selected (internally) and converted. This results in ramp time, t_{REF}. Finally the desired analog input (one of I₁ to I₆) is selected and converted. This results in ramp time t_X. This conversion sequence is arbitrary and the GND and V_{REF} conversions are not needed each time a channel is converted but only as required for calibration. The relationships between the inputs and ramp times are shown below.

$$\begin{aligned} (V_{BE1})_C &= t_z \\ (V_{REF} + V_{BE1})_C &= t_{REF} \\ (V_{IN} + V_{BE1})_C &= t_X \\ (V_{REF})_C &= t_{REF} - t_z \\ (V_{IN})_C &= t_X - t_z \\ \frac{(V_{IN})_C}{(V_{REF})_C} &= \frac{t_X - t_z}{t_{REF} - t_z} \end{aligned}$$



The conversion error can then be minimized by using the above results in the expression below to calculate the corrected analog input voltage.

$$(V_{IN})_C = (V_{REF})_C \times \frac{t_X - t_z}{t_{REF} - t_z}$$

- Where: V_{IN} = Analog input voltage to be measured
 V_{REF} = Reference voltage
 V_{BE1} = Shift voltage in sample/ramp amplifier
 V_{BE2} = Threshold voltage of comparator
 V_{CH} = C_H voltage

The GND and V_{REF} conversion sequence is arbitrary, the GND and V_{REF} conversions not being needed each time a channel (I₁ to I₆) is converted.

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PIN DESCRIPTION

Pin number	Name	Symbol	Function
9 ~ 13 15	Analog input	I_1 thru I_6	Analog inputs for the six channels. One of the 6 is selected by a specific bit pattern on A_0 to A_2 .
16 1 2	Channel selection input	A_0 A_1 A_2	Inputs for selecting an analog input channel. Either GND, one of channels I_1 to I_6 or V_{REF} is selected by a specific bit pattern on the 3 inputs.
3	RAMP START signal input	RAMP START	A/D conversion start signal input. RAMP START (1 → 0) Ramp time start signal input. RAMP START (0 → 1)
7	RAMP STOP signal output	RAMP STOP	Indicates that C_H is charged over comparator reference voltage V_{BE2} . RAMP STOP (0 → 1) A/D conversion end signal (C_H discharged to comparator reference voltage). RAMP STOP (0 → 1)
4	Ramp capacitor pin	C_H	Pin for externally connecting the ramp capacitor. The value of C_H in conjunction with V_{REF} and R_{REF} establishes the ramp time.
8	Reference voltage supply pin	V_{REF}	Reference voltage supply pin. This is the reference voltage source for determining the discharge current and the analog reference voltage for full-scale factor correction. When the channel selection input is set to 111, this pin is selected for channel conversion. The full-scale factor is corrected using the conversion results. The voltage at this pin must be set to (GND + 2 V) to ($V_{CC} - 2 V$) and 5.25 V or less.
6	Reference resistance pin	R_{REF}	Pin for external reference resistance for setting the discharge current. MB 4053: The external resistance is connected between the power source pin (V_{CC}) and the reference resistance pin (R_{REF}). The discharge current is, then, $I_R = (V_{CC} - V_{REF})/R_{REF}$. MB 4063: The external resistance is connected between the reference voltage supply pin (V_{REF}) and the reference resistance pin (R_{REF}). The discharge current is, then $I_R = V_{REF}/2R_{REF}$.
14	Power supply	V_{CC}	Power supply pin
5	Ground	GND	Ground pin This pin is grounded. When the channel selection input is set to 000, this terminal is selected for channel conversion. The zero offset is corrected using the conversion results.



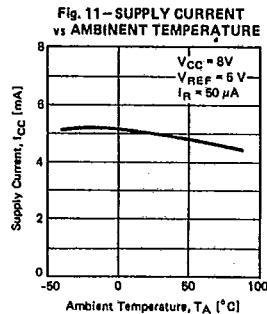
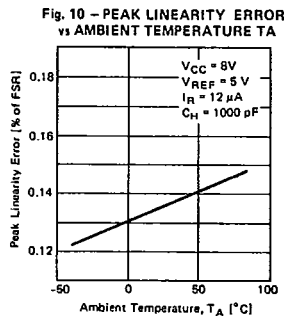
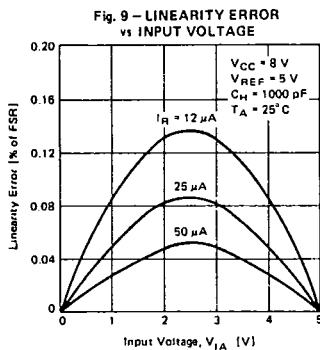
T-51-07-01

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NOTES ON USE

1. Since the impedance of the ramp capacitor pin is approximately 30 MΩ (high), a resistance must not be connected in parallel with this input. A ramp capacitor with no leakage must be used.
2. At $V_{IN} = 0 V$, t_R has a finite value.
3. Since RAMP STOP is an open collector output, an external pull-up resistor is required. (For example, when a 20 KΩ external pull-up resistor is used.)
4. All digital inputs/output are TTL compatible.
5. The time from RAMP START input switching (0 → 1) to RAMP STOP output switching (1 → 0) is ramp time t_R .
6. $t_{SL} \geq t_A (\max) = \frac{C_H}{150 \mu A - I_R} \times (V_{REF} + 0.7 V)$
7. $t_R \approx \frac{C_H}{I_R} \times V_{IN}$, $t_R (\max) \approx \frac{C_H}{I_R} \times V_{REF}$
8. $I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$ for MB 4053, $I_R = \frac{V_{REF}}{2 - R_{REF}}$ for MB 4063
9. $2 V \leq V_{REF} \leq (V_{CC} - 2 V)$ and $V_{REF} \leq 5.25 V$ for MB 4053
 $2.8 V \leq V_{REF} \leq (V_{CC} - 2 V)$ and $V_{REF} \leq 5.25 V$ for MB 4063
10. While analog input voltage is being sampled, channel selection signals A_0 , A_1 , and A_2 must not be changed for (t_{SL}) .

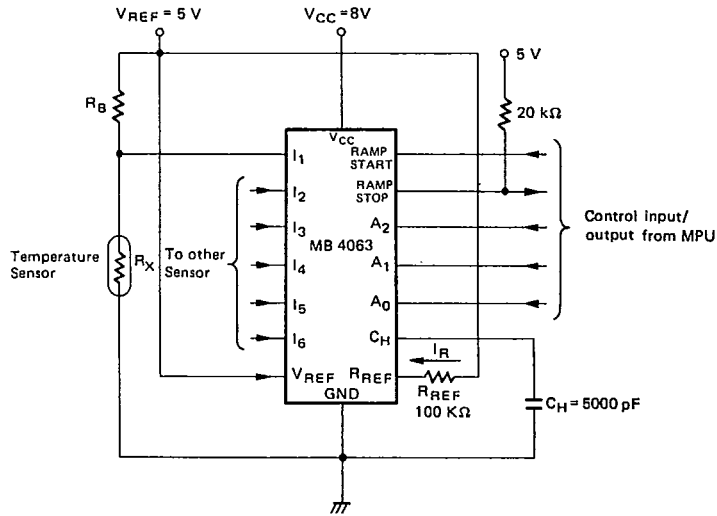
TYPICAL CHARACTERISTIC CURVES



T-51-07-01

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Fig. 8 - Application Example of MB 4063



Ramp Current: $I_R = \frac{V_{REF}}{2R_{REF}}$ 8-1

Input Voltage: $V_{IN} = \frac{R_X}{R_X + R_B} \cdot V_{REF}$ 8-2

Ramp Time: $t_R \cong V_{IN} \cdot \frac{C_H}{I_R}$

$= \frac{R_X}{R_X + R_B} \cdot C_H \cdot 2R_{REF}$ 8-3

$I_R = \frac{V_{REF}}{2R_{REF}} = \frac{5V}{2 \times 100k\Omega} = 25\mu A$

$t_{SL} \cong \frac{C_H \times V_{REF}}{I_A (min) - I_R} = \frac{5000pF \times (5V + 0.7V)}{150\mu A - 25\mu A} = 228\mu s$

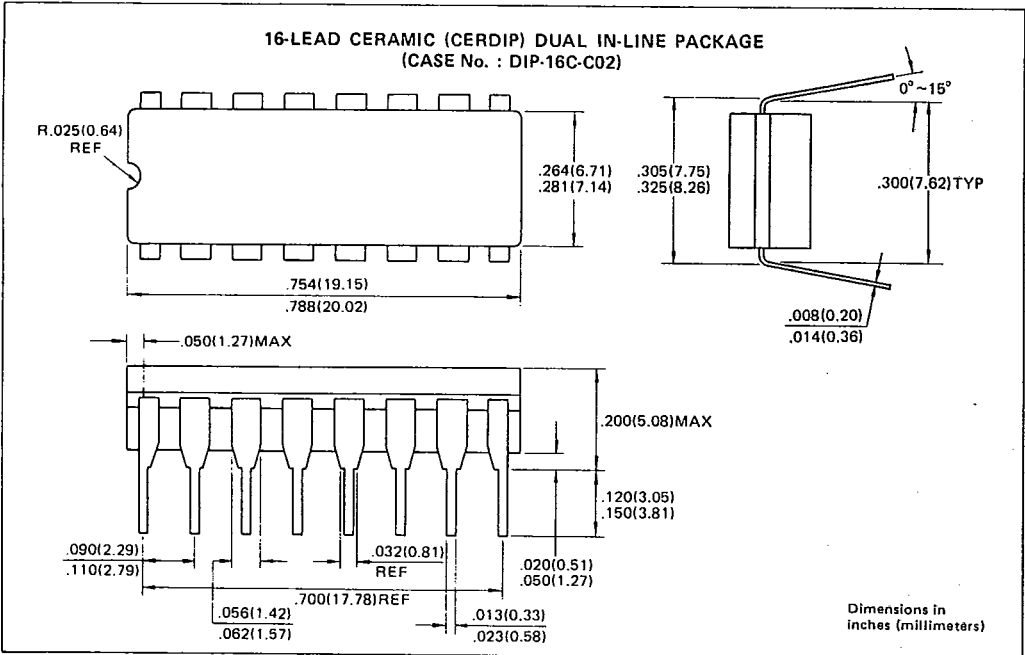
$t_{Rmax} \cong \frac{C_H \times V_{REF}}{I_R} = \frac{5000pF \times 5V}{25\mu A} = 1000\mu s$

If the ramp time is counted with a 1 MHz clock, the following resolution is obtained.

$\frac{1000\mu s}{1\mu s} = 1000 \cong 2^{10}$

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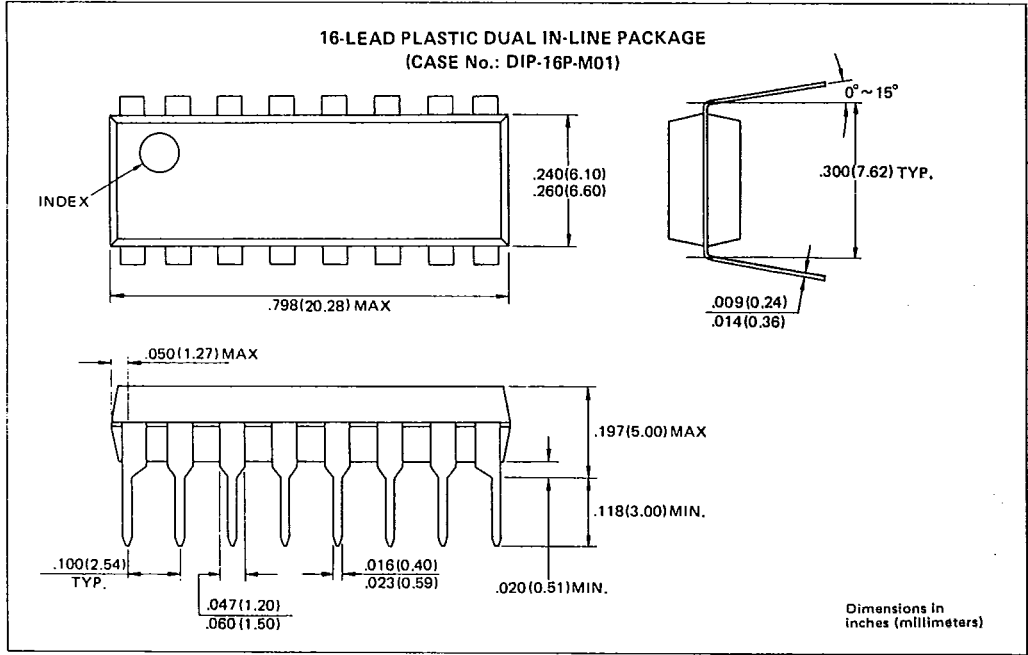
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