

# UT54ACS109E

## Dual J-K Flip-Flops

October 2008

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### FEATURES

- 0.6µm CRH CMOS Process
  - Latchup immune
- High speed
- Low power consumption
- Wide operating power supply of 3.0V to 5.5V
- Available QML Q or V processes
- 16-lead flatpack

### DESCRIPTION

The UT54ACS109E is a dual J- $\bar{K}$  positive triggered flip-flop. A low level at the preset or clear inputs sets or resets the outputs regardless of the other input levels. When preset and clear are inactive (high), data at the J and  $\bar{K}$  input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Following the hold time interval, data at the J and  $\bar{K}$  input can be changed without affecting the levels at the outputs. The flip-flops can perform as toggle flip-flops by grounding  $\bar{K}$  and tying J high. They also can perform as D flip-flops if J and  $\bar{K}$  are tied together.

The devices are characterized over full HiRel temperature range of -55°C to +125°C.

### FUNCTION TABLE

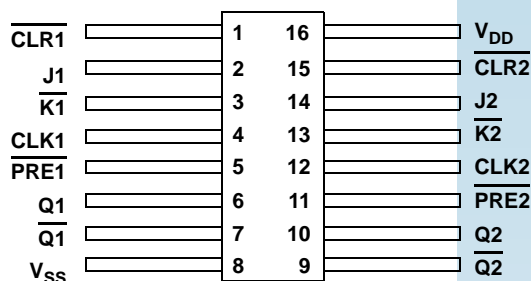
INPUTS					OUTPUT	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>1</sup>	H <sup>1</sup>
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	No Change	
H	H	↑	H	H	H	L
H	H	L	X	X	No Change	

Note:

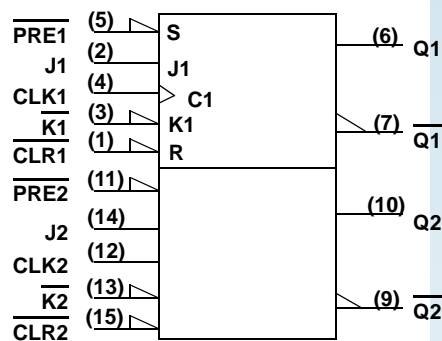
1. The output levels in this configuration are not guaranteed to meet the minimum levels for  $V_{OH}$  if the lows at preset and clear are near  $V_{IL}$  maximum. In addition, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

### PINOUTS

#### 16-Lead Flatpack Top View



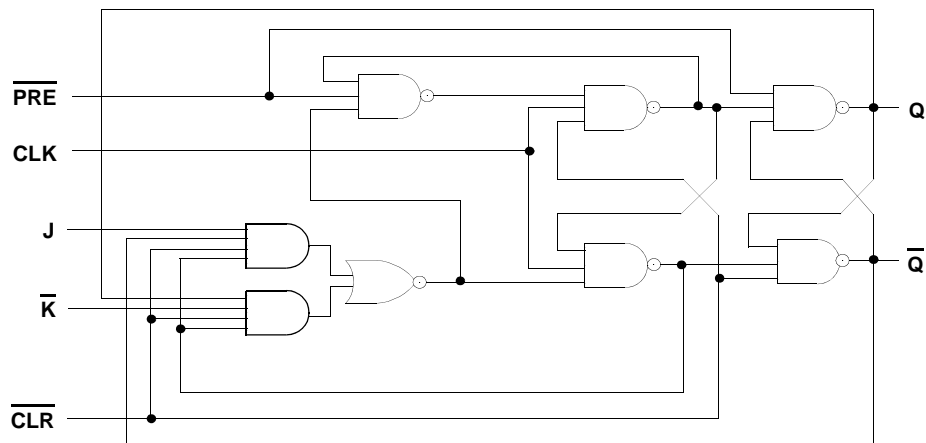
### LOGIC SYMBOL



Note:

1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



OPERATIONAL ENVIRONMENT<sup>1</sup>

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold <sup>2</sup>	80	MeV-cm <sup>2</sup> /mg
SEL Threshold	120	MeV-cm <sup>2</sup> /mg
Neutron Fluence	1.0E14	n/cm <sup>2</sup>

**Notes:**  
1. Logic will not latchup during radiation exposure within the limits defined in the table.  
2. Device storage elements are immune to SEU affects.

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
$V_{DD}$	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to $V_{DD} + .3$	V
$T_{STG}$	Storage Temperature range	-65 to +150	°C
$T_J$	Maximum junction temperature	+175	°C
$T_{LS}$	Lead temperature (soldering 5 seconds)	+300	°C
$\Theta_{JC}$	Thermal resistance junction to case	20	°C/W
$I_I$	DC input current	$\pm 10$	mA
$P_D$	Maximum power dissipation	1	W

**Note:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
$V_{DD}$	Supply voltage	3.0 to 5.5	V
$V_{IN}$	Input voltage any pin	0 to $V_{DD}$	V
$T_C$	Temperature range	-55 to + 125	°C

## DC ELECTRICAL CHARACTERISTICS FOR THE UT54ACS109E<sup>7</sup>

( $V_{DD} = 3.0V$  to  $5.5V$ ;  $V_{SS} = 0V^6$ ;  $-55^{\circ}C < T_C < +125^{\circ}C$ )

SYMBOL	Description	CONDITION	VDD	MIN	MAX	UNIT
$V_{IL}$	Low-level input voltage <sup>1</sup>		3.0V		0.9	V
			5.5V		1.65	
$V_{IH}$	High-level input voltage <sup>1</sup>		3.0V	2.1		V
			5.5V	3.85		
$I_{IN}$	Input leakage current	$V_{IN} = V_{DD}$ or $V_{SS}$	5.5V	-1	1	$\mu A$
$V_{OL}$	Low-level output voltage <sup>3</sup>	$I_{OL} = 100\mu A$	3.0V		0.25	V
			4.5V		0.25	
$V_{OH}$	High-level output voltage <sup>3</sup>	$I_{OH} = -100\mu A$	3.0V	2.75		V
			4.5V	4.25		
$I_{OS}$	Short-circuit output current <sup>2,4</sup>	$V_O = V_{DD}$ and $V_{SS}$	3.0V	-100	100	mA
			5.5V	-200	200	
$I_{OL}$	Low level output current <sup>9</sup>	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OL} = 0.4V$	3.0V	6		mA
			5.5V	8		
$I_{OH}$	High level output current <sup>9</sup>	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OH} = V_{DD}-0.4V$	3.0V		-6	mA
			5.5V		-8	
$P_{total}$	Power dissipation <sup>2, 8</sup>	$C_L = 50pF$	5.5V		2.9	mW/ MHz
			3.0V		0.8	
$I_{DDQ}$	Quiescent Supply Current	$V_{IN} = V_{DD}$ or $V_{SS}$	5.5V		10	$\mu A$
$C_{IN}$	Input capacitance <sup>5</sup>	$f = 1MHz$	0V		15	pF
$C_{OUT}$	Output capacitance <sup>5</sup>	$f = 1MHz$	0V		15	pF

### Notes:

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH(min)} + 20\%$ ,  $-0\%$ ;  $V_{IL} = V_{IL(max)} + 0\%$ ,  $-50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH(min)}$  and  $V_{IL(max)}$ .
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-PRF-38535, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose  $\leq 1E6$  rads(Si) per MIL-STD-883 Method 1019 Condition A and section 3.11.2.
- Power dissipation specified per switching output.
- This value is guaranteed based on characterization data, but not tested.

## AC ELECTRICAL CHARACTERISTICS FOR THE UT54ACS109E<sup>2</sup>

( $V_{DD} = 3.0V$  to  $5.5V$ ;  $V_{SS} = 0V$ <sup>1</sup>,  $-55^{\circ}C < T_C < +125^{\circ}C$ )

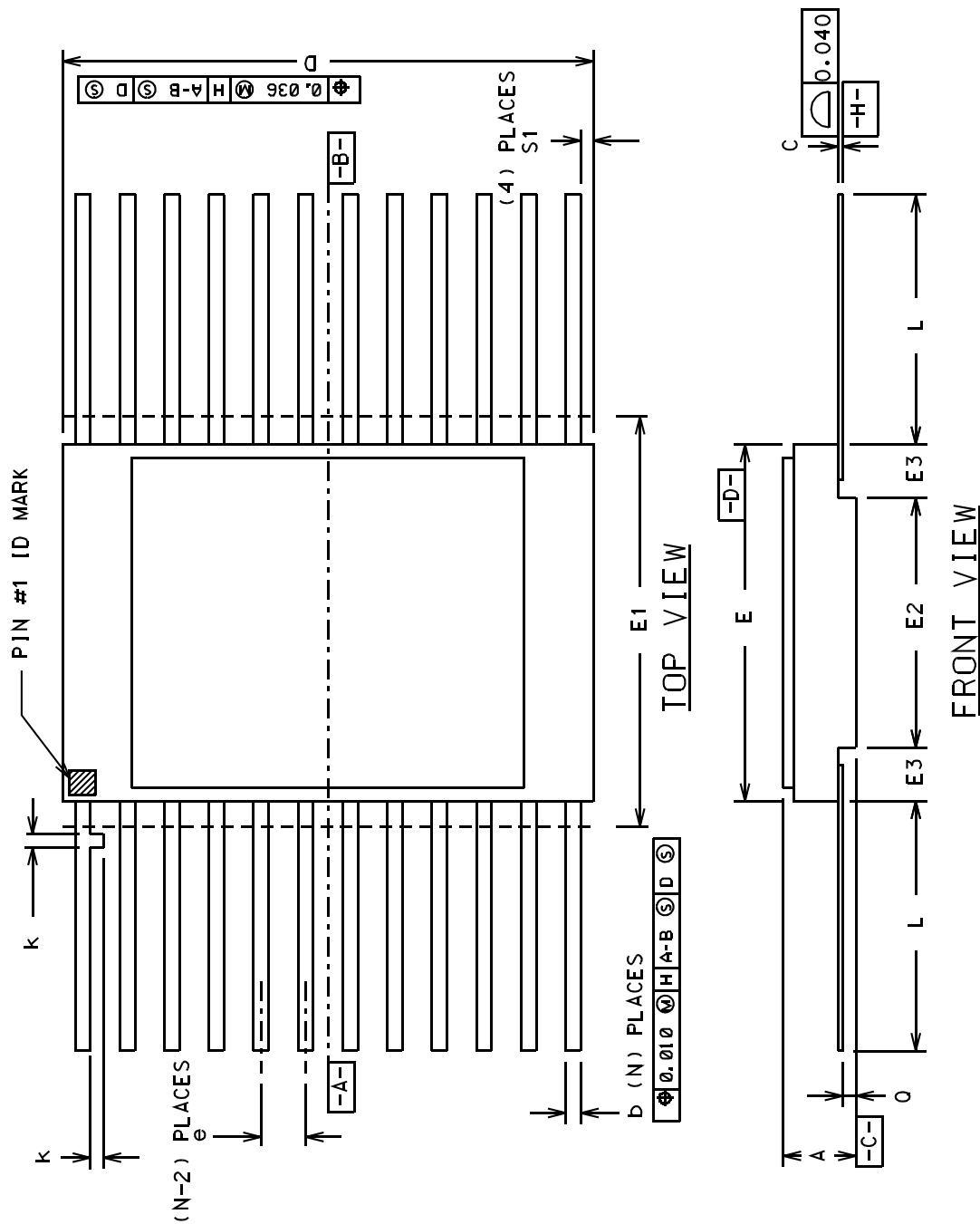
SYMBOL	PARAMETER		$V_{DD}$	MINIMUM	MAXIMUM	UNIT
$t_{PLH1}$	CLK to Q, $\overline{Q}$	$C_L = 30pF$	3.0V & 3.6V	4	23	ns
			4.5V & 5.5V	4	19	
		$C_L = 50pF$	3.0V & 3.6V	4	27	ns
			4.5V & 5.5V	4	23	
$t_{PHL1}$	CLK to Q, $\overline{Q}$	$C_L = 30pF$	3.0V & 3.6V	5	27	ns
			4.5V & 5.5V	5	23	
		$C_L = 50pF$	3.0V & 3.6V	5	31	ns
			4.5V & 5.5V	5	27	
$t_{PLH2}$	$\overline{PRE}$ to Q	$C_L = 30pF$	3.0V & 3.6V	1	16	ns
			4.5V & 5.5V	1	12	
		$C_L = 50pF$	3.0V & 3.6V	1	20	ns
			4.5V & 5.5V	1	16	
$t_{PHL2}$	$\overline{PRE}$ to $\overline{Q}$	$C_L = 30pF$	3.0V & 3.6V	1	19	ns
			4.5V & 5.5V	1	15	
		$C_L = 50pF$	3.0V & 3.6V	1	23	ns
			4.5V & 5.5V	1	19	
$t_{PLH3}$	$\overline{CLR}$ to $\overline{Q}$	$C_L = 30pF$	3.0V & 3.6V	2	16	ns
			4.5V & 5.5V	2	12	
		$C_L = 50pF$	3.0V & 3.6V	2	20	ns
			4.5V & 5.5V	2	16	
$t_{PHL3}$	$\overline{CLR}$ to Q	$C_L = 30pF$	3.0V & 3.6V	2	19	ns
			4.5V & 5.5V	2	15	
		$C_L = 50pF$	3.0V & 3.6V	2	23	ns
			4.5V & 5.5V	2	19	
$f_{MAX}$	Maximum clock frequency	$C_L = 50pF$	3.0V, 4.5V, and 5.5V		62	MHz
$t_{SU1}$	$\overline{PRE}$ or $\overline{CLR}$ inactive setup time before CLK $\uparrow$	$C_L = 50pF$	3.0V, 4.5V, and 5.5V	5		ns

$t_{SU2}$	Data setup time before CLK $\uparrow$	$C_L = 50\text{pF}$	3.0V, 4.5V, and 5.5V	5		ns
$t_H^3$	Data hold time after CLK $\uparrow$	$C_L = 50\text{pF}$	3.0V, 4.5V, and 5.5V	3		ns
$t_W$	Minimum pulse width $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low CLK high CLK low	$C_L = 50\text{pF}$	3.0V, 4.5V, and 5.5V	8		ns

**Notes:**

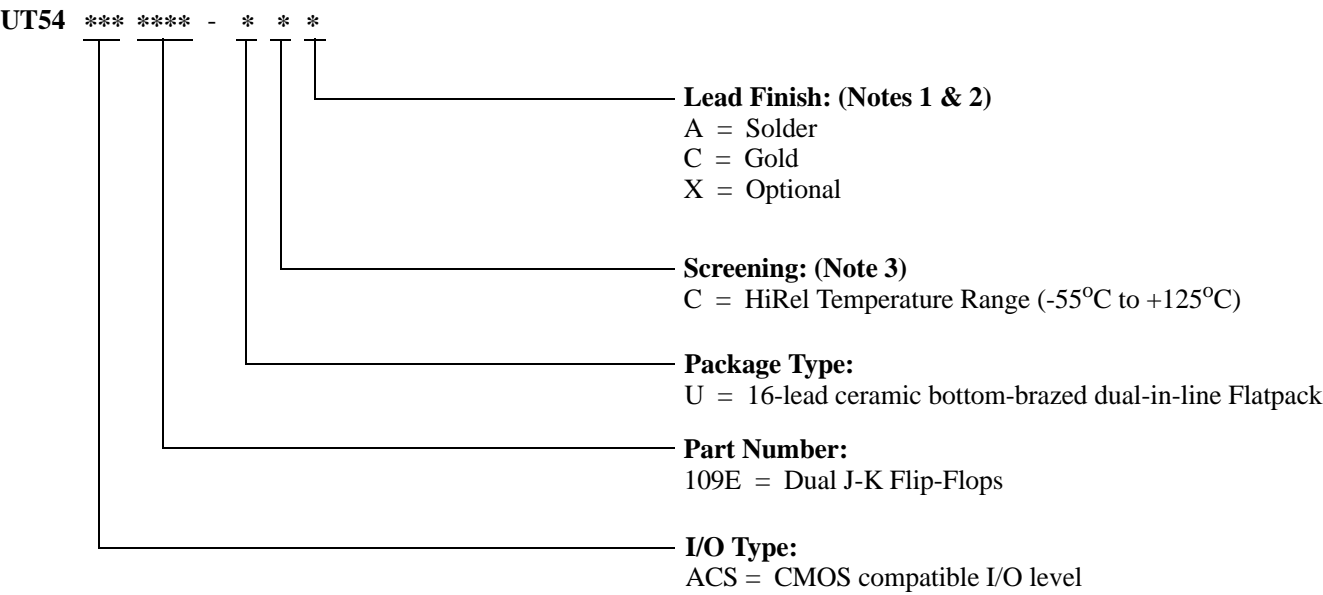
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose  $\leq 1\text{E}6$  rads(Si) per MIL-STD-883 Method 1019 Condition A and section 3.11.2.
3. Based on characterization, hold time ( $t_H$ ) of 0ns can be assumed if data setup time ( $t_{SU2}$ ) is  $\geq 10\text{ns}$ . This is guaranteed, but not tested

## Packaging



PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS											
			A	b	c	D	E	E1	E2	E3	e	k	L	Q
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 -----	0.260 0.235	0.290 -----	----- 0.130	----- BSC	0.015 0.008	0.370 0.270	0.045 0.026	----- 0.005
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 -----	0.285 0.245	0.315 -----	----- 0.130	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.005
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 -----	0.300 0.245	0.330 -----	----- 0.130	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.000

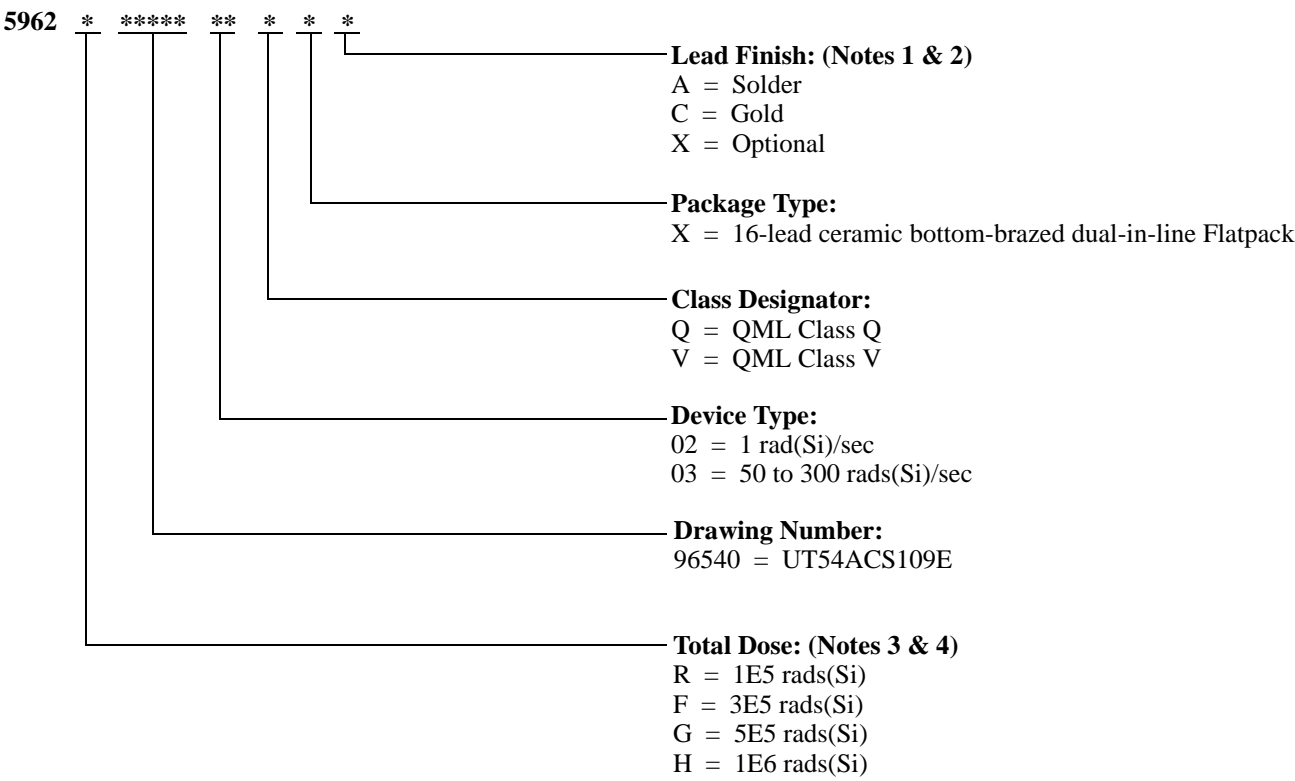
Ordering Information UT54ACS109E



- Notes:
1. Lead finish (A, C, or X) must be specified.
  2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
  3. HiRel Temperature Range flow per Aeroflex Manufacturing Flows Document. Devices have 48 hours of burn-in and are test at -55°C, room temperature, and 125°C. Radiation characteristics are neither tested nor guaranteed and may not be specified.



UT54ACS109E: SMD



- Notes:
1. Lead finish (A,C, or X) must be specified.
  2. If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
  3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
  4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

## ***Aeroflex Colorado Springs - Datasheet Definition***

**Advanced Datasheet - Product In Development**

**Preliminary Datasheet - Shipping Prototype**

**Datasheet - Shipping QML & Reduced HiRel**

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