Signetics

8X02A
Control Store Sequencer

Product Specification

Logic Products

FEATURES

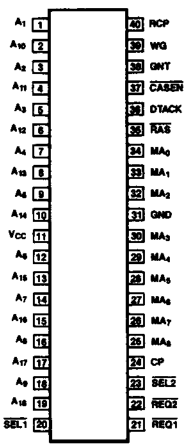
- **10-Bit Address Generator (1024 Microinstruction Addressability)**
- **Operating Frequency Exceeding 12 MHz**
- **Direct Branching Over Full Address Range**
- **Conditional Branching**
- **Subroutine Branching Capability**
- **4-Level Stack Register File**
- **Loop Control Facility Using Stack**
- **Three-State Address Outputs**

PRODUCT DESCRIPTION

The Signetics 8X02A Control Store Sequencer generates addresses to access instructions from a microprogram memory (control store). This high-speed device provides an efficient means of controlling the flow through a microprogram with a powerful set of sequencing functions. The 8X02A can directly address up to 1024 microinstructions; however, the total address space can be expanded by adding conventional paging techniques. Combined with memory, the 8X02A forms a powerful control section for CPU's, controllers, test equipment, and other microprogram-controlled systems.

8X02A PACKAGE AND PIN DESIGNATIONS

N PACKAGE



ORDER NUMBER

N8X02AN

PIN NO.	IDENTIFIER	FUNCTION
1, 28, 27	$AC_2 - AC_0$	Inputs used to select any one of eight Address Control Functions - see Table 1.
2	$\overline{EN}$	Enable three-state address outputs ($A_0 - A_9$); active-low input.
3 - 6, 8 - 13	$A_0 - A_9$	Three-state address outputs used to specify microprogram address; (A_0 = LSB, A_9 = MSB).
7	GND	Ground
14 - 21, 23, 24	$B_0 - B_9$	Branch address inputs: (B_0 = LSB, B_9 = MSB).
22	V_{CC}	Supply voltage.
25	CLK	Clock input (positive edge used for all triggering).
26	TEST	Active-high condition input used to determine conditional skips, branches, subroutine calls, and loop termination.

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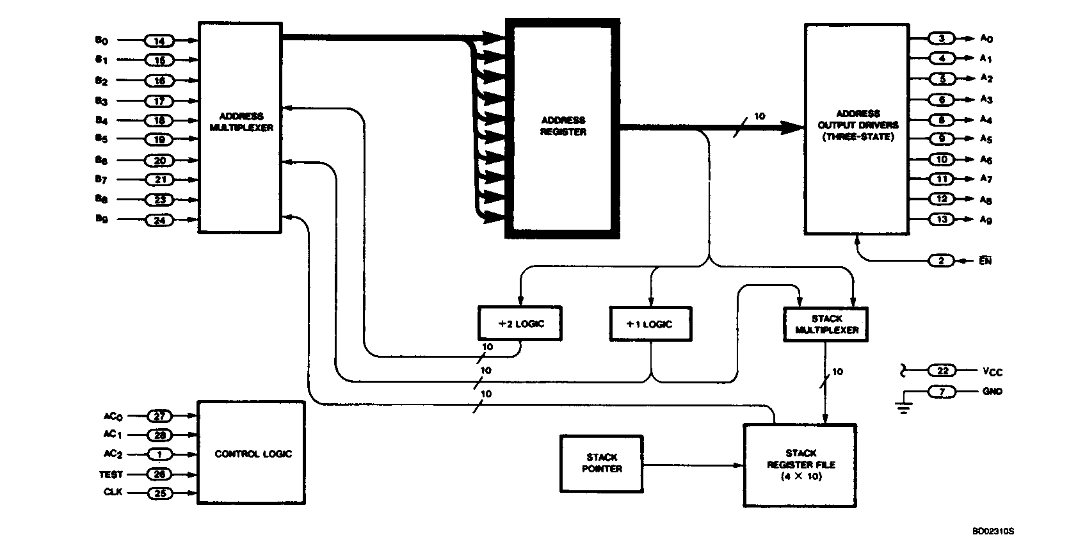

Figure 1. 8X02A Control Store Sequencer — Functional Block Diagram

FUNCTIONAL OPERATION

As shown in Figure 1, the data appearing on the address output pins ($A_0 - A_9$) is the contents of the 10-bit Address Register. On the rising edge of the clock input pulse (CLK), a new address is latched into the Address Register. This new address is supplied via the Address Multiplexer which selects one of five sources:

- Branch Address Input ($B_0 - B_9$)
- Current Address + 1
- Current Address + 2 (for the SKIP function)
- Stack Register File (most recent entry)
- All Zeroes (RESET)

The selection of the next address is determined by the "Address Control Function" specified by inputs $AC_0 - AC_2$ and the TEST input. Table 1 defines the eight Address Control Functions.

The "Reset" (RST) Address Control Function unconditionally forces all Address Register bits to zero on the rising edge of CLK. Sequential microprogram flow is provided by the "Increment" (INC) function which unconditionally increments the Address Register by one for each clock cycle. The Address Register automatically wraps around from the highest address (all "1s") to the lowest address (all "0s").

As shown in Table 1, the TEST input is used to conditionally execute four of the eight Address Control Functions. If the TEST input is **low** (false), the Address Register is simply incremented by one — (for the BLT function, the Stack Pointer is also decremented). If the TEST input is **high** (true), the sequencer executes one of the following:

- Skip (TSK) — the Address Register is incremented by two.
- Branch (BRT) — the Address Register is loaded from the Branch Address Inputs.
- Branch-to-Subroutine (BSR).
- Branch-to-Loop (BLT).

The Stack Register File holds up to four 10-bit addresses and operates in the Last-In/First-Out (LIFO) mode. A Stack Pointer keeps track of the next register of the Stack File to be written into; the pointer is incremented after each "push" and decremented after each "pop" — see Table 1. When branching to a subroutine (BSR), the return address (current address + 1) is "pushed" onto the stack and the branch address input is loaded into the Address Register. To return from a subroutine, the "POP" function pops the return address off the stack and loads it into the Address Register.

The "Push-for-Looping" (PLP) function may be specified in the first instruction of a loop to "push" the current address onto the stack: the Address Register is incremented. A "Branch-to-Loop" (BLT) function placed at the end of the loop "pops" the stack and conditionally branches to the top-of-loop address, depending on the TEST input. If the test for repeating the loop is satisfied (TEST input **high**), the sequencer causes a branch back to the first instruction of the loop in which the top-of-loop address is "pushed" back onto the stack. If the test fails (TEST input **low**), the top-of-loop address is discarded, the stack pointer is decremented and the Address Register is incremented. A combination of subroutines and loops may be nested up to four levels deep.

In abnormal circumstances, the Stack Pointer will wraparound from the fourth to the first register of the Stack File and vice-versa. If the stack is full (four addresses currently stored), an additional "push" causes the first (oldest) entry to be overwritten — (the four most recent entries are always maintained). If the stack is empty, a "pop" will access the fourth register of the Stack File; however, the contents of this register may be unpredictable.

The three-state address outputs ($A_0 - A_9$) are controlled by a common enable input ($\overline{EN}$). When the enable input is **high**, the output drivers are placed in the high-impedance state allowing alternative access to the microprogram memory. Other circuit functions are unaffected by $\overline{EN}$.

NOTE

To implement a RESET externally it is necessary to force all Address Control Inputs ($AC_0 - AC_2$) to the **high** state until at least one rising edge of CLK has occurred. If the AC inputs are supplied directly from the microprogram memory, a RESET may be accomplished by disabling the memory outputs. Pullup resistors should be provided to achieve the required high voltage level.

Table 1. Address Control Functions

MNEMONIC AND DESCRIPTION	CONTROL LINES				NEXT ADDRESS	STACK OPERATION	STACK POINTER
	AC_2	AC_1	AC_0	Test			
TSK – Test and skip	0 0	0 0	0 0	0 1	Current address + 1 Current address + 2	No change No change	No change No change
INC – Increment	0	0	1	X	Current address + 1	No change	No change
BLT – Branch to loop if test condition is true	0 0	1 1	0 0	0 1	Current address + 1 From stack register file	POP (ignore data) POP (read)	Decrement by 1 Decrement by 1
POP – Pop stack (return from subroutine)	0	1	1	X	From stack register file	POP (read)	Decrement by 1
BSR – Branch to subroutine if test condition is true	1 1	0 0	0 0	0 1	Current address + 1 Branch address inputs $B_0 - B_9$	No change PUSH (write current address + 1)	No change Increment by 1
PLP – Push for looping	1	0	1	X	Current address + 1	PUSH (write current address)	Increment by 1
BRT – Branch if test condition is true	1 1	1 1	0 0	0 1	Current address + 1 Branch address inputs $B_0 - B_9$	No change No change	No change No change
RST – Reset address to zero	1	1	1	X	All zeroes	No change	No change

X = Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS **Conditions:** Commercial – V_{CC} = 5.0V (±5%), 0°C ≤ T_A ≤ 70°C

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS Min	Typ[1]	Max	UNIT
V_{IH}	High level input voltage	V_{CC} = Min	2			V
V_{IL}	Low level input voltage	V_{CC} = Min			0.8	V
V_{IC}	Input clamp voltage	V_{CC} = Min; I_I = -18mA			-1.5	V
V_{OH}	High level output voltage	V_{CC} = Min; I_{OH} = -2.6mA	2.4	3.4		V
V_{OL}	Low level output voltage	V_{CC} = Min; I_{OL} = 8mA		0.42	0.5	V
I_I	Input current at maximum input voltage	V_{CC} = Max; V_I = 5.5V		1	100	µA
I_{IH}	High level input current: $AC_2 - AC_0$, TEST, CLK	V_{CC} = Max; V_{IH} = 2.7V		< 0.1	40	µA
	$B_9 - B_0$, $\overline{EN}$			< 0.1	20	
I_{IL}	Low level input current: $AC_2 - AC_0$, TEST, CLK	V_{CC} = Max; V_{IL} = 0.4V		-24	-800	µA
	$B_9 - B_0$, $\overline{EN}$			-12	-400	
I_{OS}	Short circuit output current[2]	V_{CC} = Max	-15	-60	-100	mA
I_{OZH}	High-Z state output current – high level	V_{CC} = Max; V_{OH} = 2.7V			20	µA
I_{OZL}	High-Z state output current – low level	V_{CC} = Max; V_{OL} = 0.4V			-20	µA
I_{CC}	Supply current	V_{CC} = Max		170	250	mA

NOTES:
1. Typical limits are: V_{CC} = 5.0V and T_A = 25°C.
2. For purposes of testing, not more than one output should be shorted at a time.

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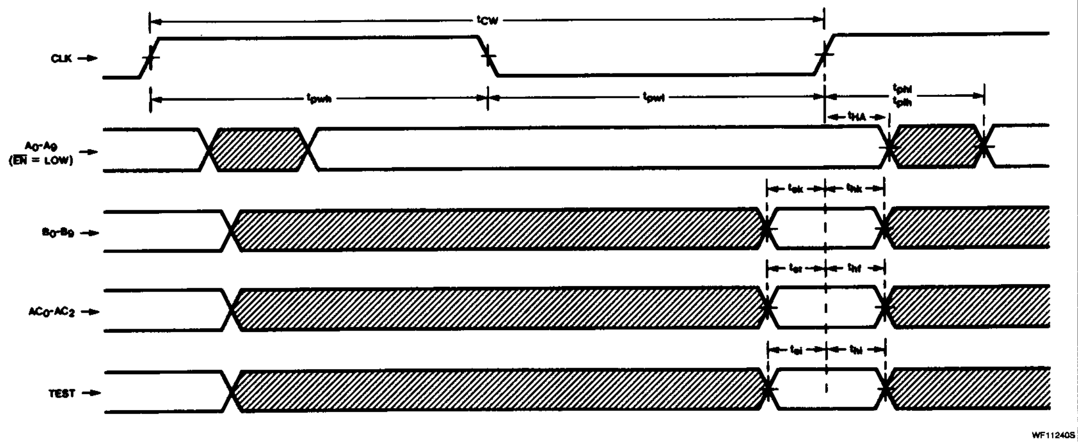
AC ELECTRICAL CHARACTERISTICS **Conditions:** Commercial – V_{CC} = 5.0V (±5%), 0°C ≤ T_A ≤ 70°C
Loading – See Test Loading Circuit

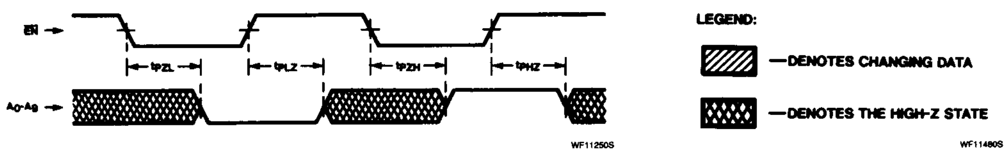
PARAMETERS[1]		REFERENCES		LIMITS[4]			UNIT
		From	To	Min	Typ[2]	Max	
Pulse width:							
t_{CW}	Clock cycle time	↑ CLK	↑ CLK	80			ns
t_{PWH}	Clock high	↑ CLK	↓ CLK	35	24		ns
t_{PWL}	Clock low	↓ CLK	↑ CLK	15	9		ns
Propagation delay:							
t_{PLZ}	Low to high-Z	↑ $\overline{EN}$	$A_0 - A_9$		14	20	ns
t_{PHZ}	High to high-Z	↑ $\overline{EN}$	$A_0 - A_9$		35	42	ns
t_{PZL}	High-Z to low	↓ $\overline{EN}$	$A_0 - A_9$		10	20	ns
t_{PZH}	High-Z to high	↓ $\overline{EN}$	$A_0 - A_9$		20	30	ns
t_{PHL}	High to low	↑ CLK	↓ $A_0 - A_9$		25	45	ns
t_{PLH}	Low to high	↑ CLK	↑ $A_0 - A_9$		25	45	ns
t_{HA}	Address output hold time[3]	↑ CLK	$A_0 - A_9$	13			ns
Set-up/hold times:							
t_{SF}	Function set-up time	$AC_0 - AC_2$	↑ CLK	20	18		ns
t_{SK}	Branch set-up time	$B_0 - B_9$	↑ CLK	15	7		ns
t_{SI}	Test set-up time	TEST	↑ CLK	20	15		ns
t_{HF}	Function hold time	↑ CLK	$AC_0 - AC_2$	20	2		ns
t_{HK}	Branch hold time	↑ CLK	$B_0 - B_9$	15	9		ns
t_{HI}	Test hold time	↑ CLK	TEST	12	-2		ns

NOTES:
1. Parameter definitions are illustrated in the Timing Diagrams – See Figure 2.
2. Typical limits are: V_{CC} = 5.0V and T_A = 25°C.
3. t_{HA} is the minimum time the current address outputs remain stable before changing. This delay may be used to provide some of the hold times required for the AC, B, and TEST inputs, if these inputs are determined by the microprogram memory addressed by the 8X02A.
4. This data supercedes the November, 1980 edition of this data sheet.

TIMING DIAGRAM



a. Clock Synchronization

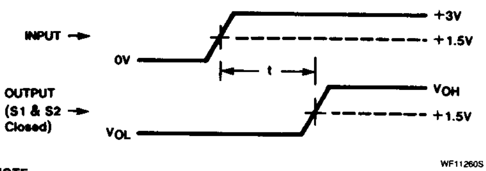


b. Output Enable

Figure 2. Timing Diagrams

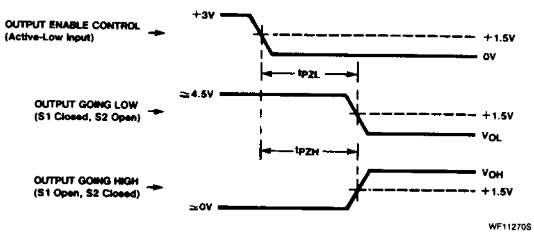
AC VOLTAGE WAVEFORMS AND TEST LOADING

PROPAGATION DELAY (Typical Example):

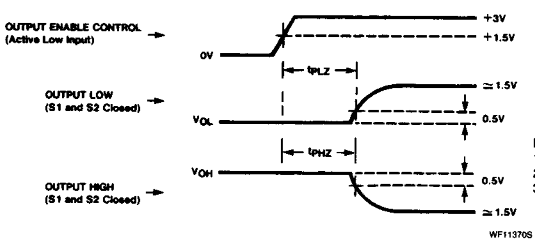


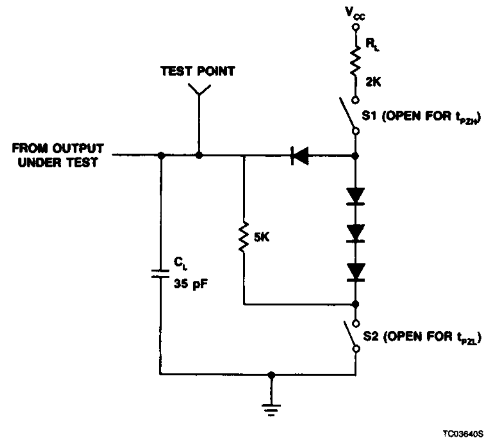
NOTE:
Pulse widths and setup/hold times are measured using the same reference points shown in the above waveforms.

OUTPUT ENABLE TIMES (Three-state outputs):



OUTPUT DISABLE TIMES (Three-state outputs):





NOTES:
1. C_L includes probe and jig capacitance.
2. All diodes are 1N3064 or equivalent.
3. Switches S1 and S2 are both closed for all measurements except Output Enable times — See AC VOLTAGE WAVEFORMS.

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APPLICATION

FUNCTIONAL DESCRIPTION

Figure 3 shows a typical configuration of an 8X02A-based control section in a CPU application. Microinstructions read from the memory are used to produce control signals for the CPU and to determine the next microinstruction via the 8X02A Address Control inputs ($AC_0 - AC_2$). In the case of a conditional branch or skip, the status condition applied to the 8X02A TEST input is selected according to the microinstruction. In a branch-type microinstruction, a branch field typically supplies the 8X02A Branch Address inputs ($B_0 - B_9$). (In non-branching instructions, this field may contain other CPU control information.) When a macroinstruction is presented to the CPU, the starting address of the microprogram routine which executes the macroinstruction is presented to the Branch Address inputs. Similar configurations may be used for other applications in which the Branch Address inputs are typically supplied directly from the microprogram memory.

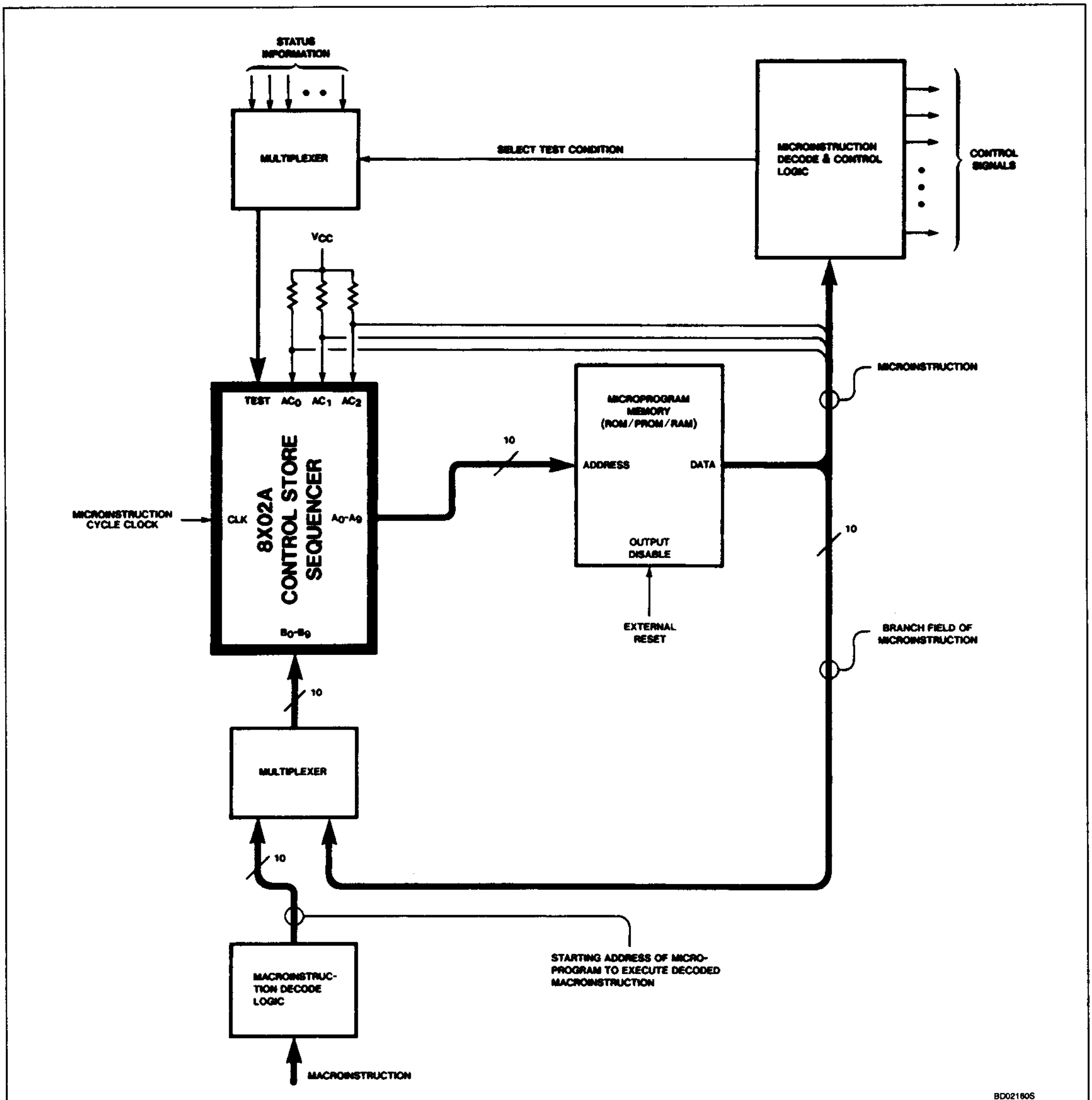

Figure 3. Control Section of a Microprogrammed CPU

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