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Memory Products	

FAST 74F189A

64-bit TTL bipolar RAM, inverting (3-State)

FEATURES

- High speed performance
- Replaces 74F189
- Address access time: 8ns max vs 28ns for 74F189
- Power dissipation: 4.3mW/bit
- Schottky clamp TTL
- One chip enable
- Inverting outputs (for non-inverting outputs see 74F219A)
- Buffered PNP inputs
- 3-state outputs
- 74F189A in 150 mil wide SO is preferred options for new designs
- C3F189A in 300 mil wide SOL replaces 74F189 in existing designs

DESCRIPTION

The 74F189A is a high speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on chip. The outputs are in high impedance state whenever the chip enable (CE) is high. The outputs are active only in the READ mode (WE = high) and the output data is the complement of the stored data.

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F189A	5.0ns	55mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$
16-pin plastic DIP	N74F189AN
16-pin plastic SO (150mil)	N74F189AD
16-pin plastic SOL (300mil)	C3F189AD

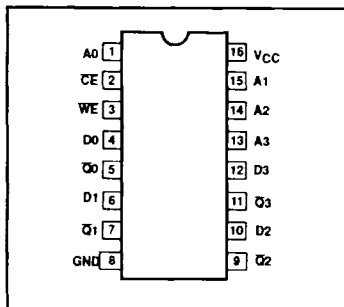
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Data inputs	1.0/1.0	20 μ A/0.6mA
A0 - A3	Address inputs	1.0/1.0	20 μ A/0.6mA
CE	Chip enable input (active low)	1.0/2.0	20 μ A/1.2mA
WE	Write enable input (active low)	1.0/2.0	20 μ A/1.2mA
Q0 - Q3	Data outputs	150/40	3mA/24mA

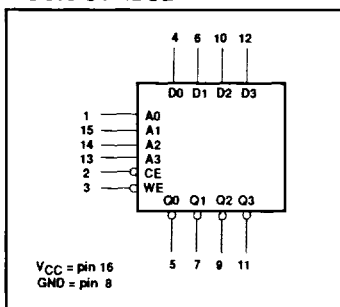
Notes to input and output loading and fan out table

- One (1.0) FAST unit load is defined as: 20 μ A in the high state and 0.6mA in the low state.

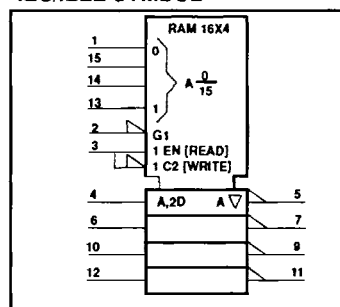
PIN CONFIGURATION



LOGIC SYMBOL



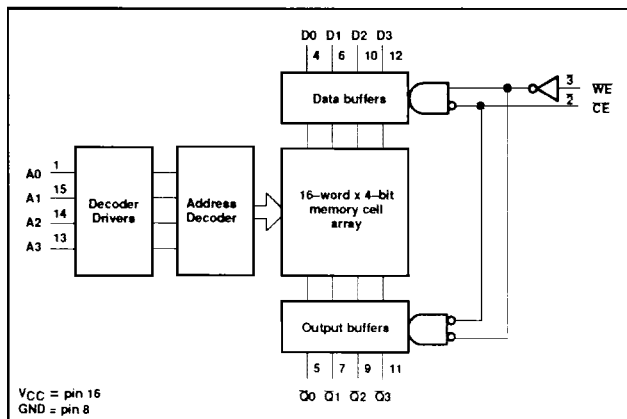
IEC/IEEE SYMBOL



64-bit bipolar RAM (16 × 4)

FAST 74F189A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
CE	WE	Dn	$\bar{Q}_n$	
L	H	X	Complement of stored data	Read
L	L	L	High impedance	Write "0"
H	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable input

Notes to function table

- Notes to function table
1. H = High voltage level
 2. L = Low voltage level
 3. X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in high output state	-0.5 to V _{CC}	V
I _{OUT}	Current applied to output in low output state	48	mA
T _{amb}	Operating free air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{ik}	Input clamp current			-18	mA
I _{OH}	High-level output current			-3	mA
I _{OL}	Low-level output current			24	mA
T _{amb}	Operating free air temperature range	0		+70	°C

64-bit bipolar RAM (16 × 4)**FAST 74F189A****DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹	LIMITS			UNIT
				MIN	TYP ²	MAX	
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = MAX	±10%V _{CC}	2.4		V
			V _{IH} = MIN, I _{OH} = MAX	±5%V _{CC}	2.7	3.4	V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX	±10%V _{CC}		0.35	V
			V _{IH} = MIN, I _{OL} = MAX	±5%V _{CC}		0.35	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}		-0.73	-1.2	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7.0V			100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL}	Low-level input current	others	V _{CC} = MAX, V _I = 0.5V			-0.6	mA
		CE, WE				-1.2	mA
I _{OZH}	Offset output current, high-level voltage applied		V _{CC} = MAX, V _I = 2.7V			50	μA
I _{OZL}	Offset output current, low-level voltage applied		V _{CC} = MAX, V _I = 0.5V			-50	μA
I _{OS}	Short-circuit output current ³		V _{CC} = MAX	-60		-150	mA
I _{CC}	Supply current (total)		V _{CC} = MAX, CE = WE = GND		55	80	mA
C _{IN}	Input capacitance		V _{CC} = 5V, V _{IN} = 2.0V		4		pF
C _{OUT}	Output capacitance		V _{CC} = 5V, V _{OUT} = 2.0V		7		pF

Notes to DC electrical characteristics

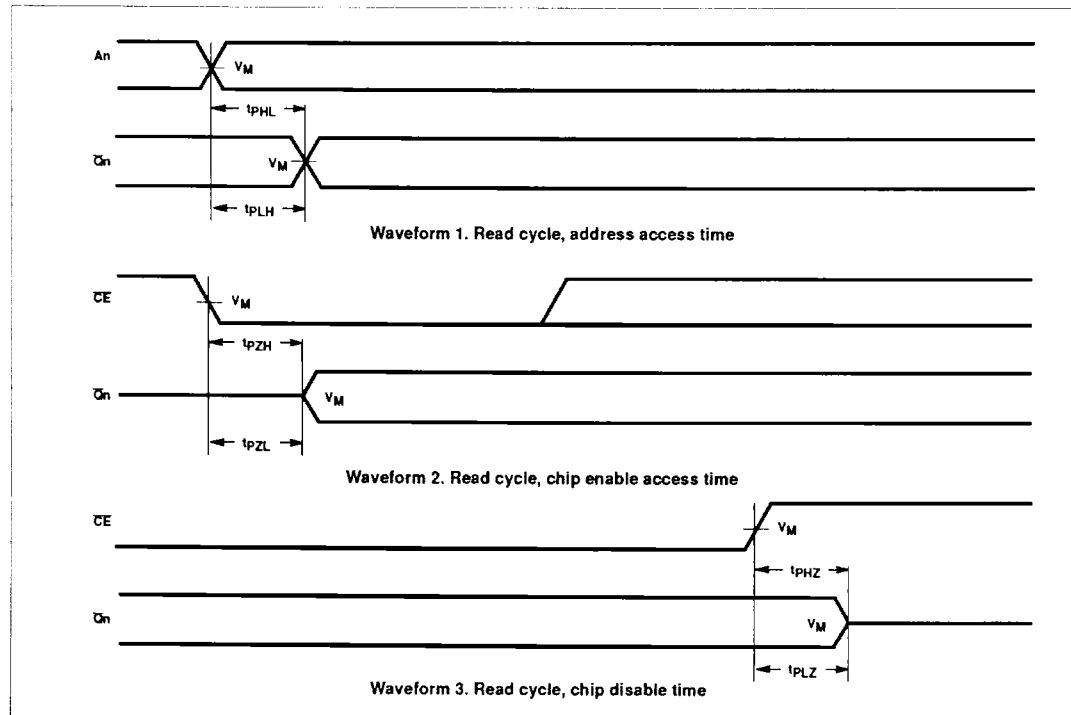
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS						UNIT
				T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω			
				MIN	TYP	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Access time	Propagation delay An to Qn	Waveform 1	2.5 2.0	5.0 4.5	8.0 8.0	2.5 2.0	8.0 8.0	ns	
t _{PZH} t _{PZL}		Enable time CE to Qn	Waveform 2	2.0 2.0	3.5 4.0	6.0 7.0	1.5 2.0	7.0 7.5		
t _{PHZ} t _{PLZ}	Disable time CE to Qn		Waveform 3	2.5 1.5	4.5 3.0	7.0 5.5	2.0 1.5	8.0 6.0	ns	
t _{PZH} t _{PZL}	Write recovery time	Enable time WE to Qn	Waveform 4	2.0 2.5	4.0 4.5	6.5 7.5	2.0 2.5	7.0 8.0	ns	
t _{PHZ} t _{PLZ}	Disable time WE to Qn		Waveform 4	3.5 1.5	5.5 3.5	8.5 6.5	3.0 1.5	9.0 7.0	ns	

64-bit bipolar RAM (16 × 4)**FAST 74F189A****AC SETUP REQUIREMENT**

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{su} (H) t _{su} (L)	Setup time, high or low An to $\overline{\text{WE}}$	Waveform 4	4.5 4.5			5.0 5.0		ns
t _h (H) t _h (L)	Hold time, high or low An to $\overline{\text{WE}}$	Waveform 4	0 0			0 0		ns
t _{su} (H) t _{su} (L)	Setup time, high or low Dn to $\overline{\text{WE}}$	Waveform 4	7.5 6.5			9.0 8.0		ns
t _h (H) t _h (L)	Hold time, high or low Dn to $\overline{\text{WE}}$	Waveform 4	0 0			0 0		ns
t _{su} (L)	Setup time, low $\overline{\text{CE}}$ (falling edge) to $\overline{\text{WE}}$ (falling edge)	Waveform 4	0			0		ns
t _h (L)	Hold time, low $\overline{\text{WE}}$ (falling edge) to $\overline{\text{WE}}$ (rising edge)	Waveform 4	6.5			7.5		ns
t _w (L)	Pulse width, low $\overline{\text{WE}}$	Waveform 4	7.0			8.0		ns

AC WAVEFORMS FOR READ CYCLES

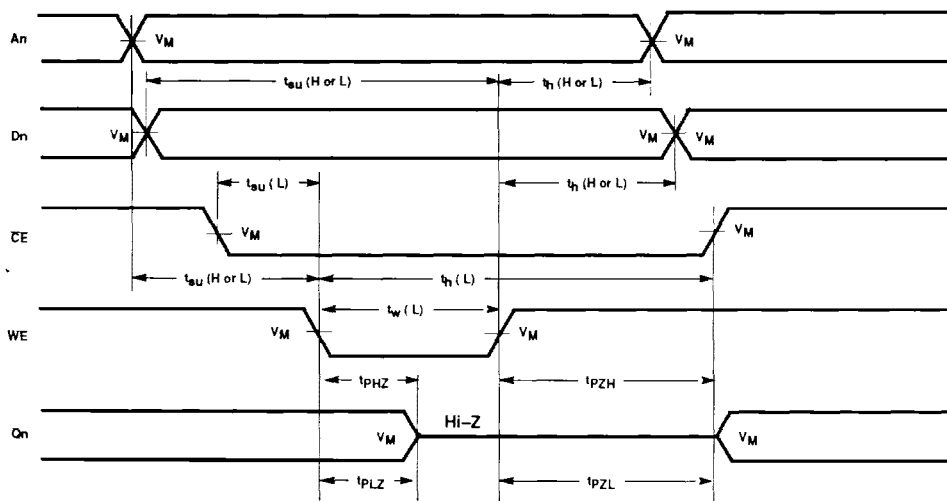
Note to AC Waveforms read cycles

1. For all waveforms, $V_M = 1.5V$.

64-bit bipolar RAM (16 × 4)

FAST 74F189A

AC WAVEFORMS FOR WRITE CYCLE

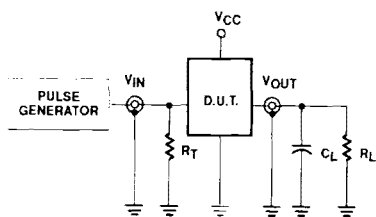


Waveform 3. Write cycle

Note to AC Waveforms write cycle

1. For all waveforms, $V_M = 1.5V$.

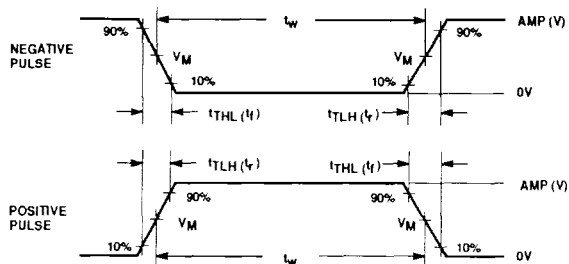
TEST CIRCUIT AND WAVEFORM



Test circuit for totem-pole outputs

DEFINITIONS:

- R_L = Load resistor; see AC electrical characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns