MachXO Family Data Sheet

Data Sheet

FPGA-DS-02071-3.3

July 2022

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS and with all faults, and all risk associated with such information is entirely with Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Contents

Figures

Tables

1. Introduction

The MachXO is optimized to meet the requirements of applications traditionally addressed by CPLDs and low capacity FPGAs: glue logic, bus bridging, bus interfacing, power-up control, and control logic. These devices bring together the best features of CPLD and FPGA devices on a single chip.

1.1. Features

- Non-volatile, Infinitely Reconfigurable
  - Instant-on – powers up in microseconds
  - Single chip, no external configuration memory required
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through JTAG port
  - Supports background programming of non-volatile memory
- Sleep Mode
  - Allows up to 100x static current reduction
- TransFR™ Reconfiguration (TFR)
  - In-field logic update while system operates
- High I/O to Logic Density
  - 256 to 2280 LUT4s
  - 73 to 271 I/Os with extensive package options
  - Density migration supported
  - Lead free/RoHS compliant packaging
- Embedded and Distributed Memory
  - Up to 27.6 Kbits sysMEM™ Embedded Block RAM
  - Up to 7.7 Kbits distributed RAM
  - Dedicated FIFO control logic
- Flexible I/O Buffer
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- sysCLOCK™ PLLs
  - Up to two analog PLLs per device
  - Clock multiply, divide, and phase shifting
- System Level Support
  - IEEE Standard 1149.1 Boundary Scan
  - Onboard oscillator
  - Devices operate with 3.3 V, 2.5 V, 1.8 V or 1.2 V power supply
  - IEEE 1532 compliant in-system programming

Table 1.1. MachXO Family Selection Guide

Device	LCMXO256	LCMXO640	LCMXO1200	LCMXO2280
LUTs	256	640	1200	2280
Dist. RAM (Kbits)	2.0	6.1	6.4	7.7
EBR SRAM (Kbits)	0	0	9.2	27.6
Number of EBR SRAM Blocks (9 Kbits)	0	0	1	3
V_{CC} Voltage	1.2/1.8/2.5/3.3 V	1.2/1.8/2.5/3.3 V	1.2/1.8/2.5/3.3 V	1.2/1.8/2.5/3.3 V
Number of PLLs	0	0	1	2
Max. I/O	78	159	211	271
Packages				
100-pin TQFP (14x14 mm)	78	74	73	73
144-pin TQFP (20x20 mm)		113	113	113
100-ball csBGA (8x8 mm)	78	74		
132-ball csBGA (8x8 mm)		101	101	101
256-ball caBGA (14x14 mm)		159	211	211
256-ball ftBGA (17x17 mm)		159	211	211
324-ball ftBGA (19x19 mm)				271

The devices use look-up tables (LUTs) and embedded block memories traditionally associated with FPGAs for flexible and efficient logic implementation. Through non-volatile technology, the devices provide the single-chip, highsecurity, instant-on capabilities traditionally associated with CPLDs. Finally, advanced process technology and careful design will provide the high pin-to-pin performance also associated with CPLDs.

The ispLEVER® design tools from Lattice allow complex designs to be efficiently implemented using the MachXO family of devices. Popular logic synthesis tools provide synthesis library support for MachXO. The ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the MachXO device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

2. Architecture

2.1. Architecture Overview

The MachXO family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). Some devices in this family have sysCLOCK PLLs and blocks of sysMEM™ Embedded Block RAM (EBRs). Figure 2.1.,Figure 2.2., and Figure 2.3. show the block diagrams of the various family members.

The logic blocks are arranged in a two-dimensional grid with rows and columns. The EBR blocks are arranged in a column to the left of the logic array. The PIO cells are located at the periphery of the device, arranged into Banks. The PIOs utilize a flexible I/O buffer referred to as a sysIO interface that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

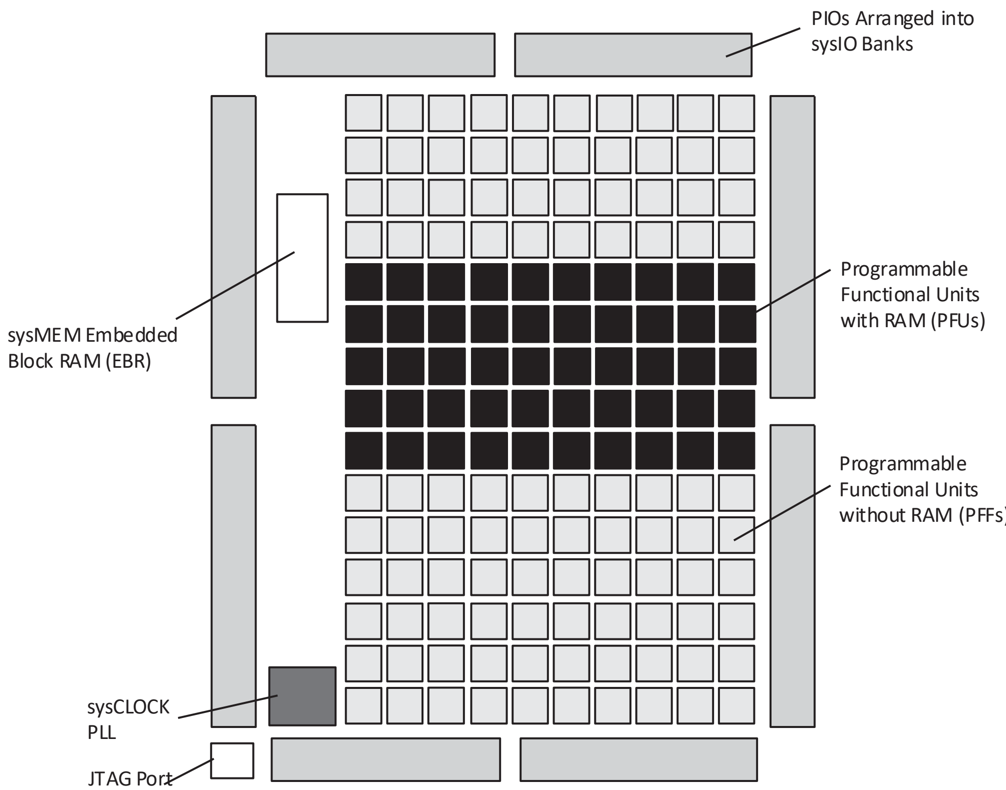
There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and the Programmable Functional unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PFF block contains building blocks for logic, arithmetic, ROM, and register functions. Both the PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and effectively. Logic blocks are arranged in a two-dimensional array. Only one type of block is used per row.

In the MachXO family, the number of sysIO Banks varies by device. There are different types of I/O Buffers on different Banks. See the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found only in the larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT use.

The MachXO registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO architecture provides up to two sysCLOCK™ Phase Locked Loop (PLL) blocks on larger devices. These blocks are located at either end of the memory blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a JTAG Port that supports programming and configuration of the device as well as access to the user logic. The MachXO devices are available for operation from 3.3 V, 2.5 V, 1.8 V, and 1.2 V power supplies, providing easy integration into the overall system.



1. Top view of the MachXO2280 device is similar but with higher LUT count, two PLLs, and three EBR blocks.

Figure 2.1. Top View of the MachXO1200 Device[1]

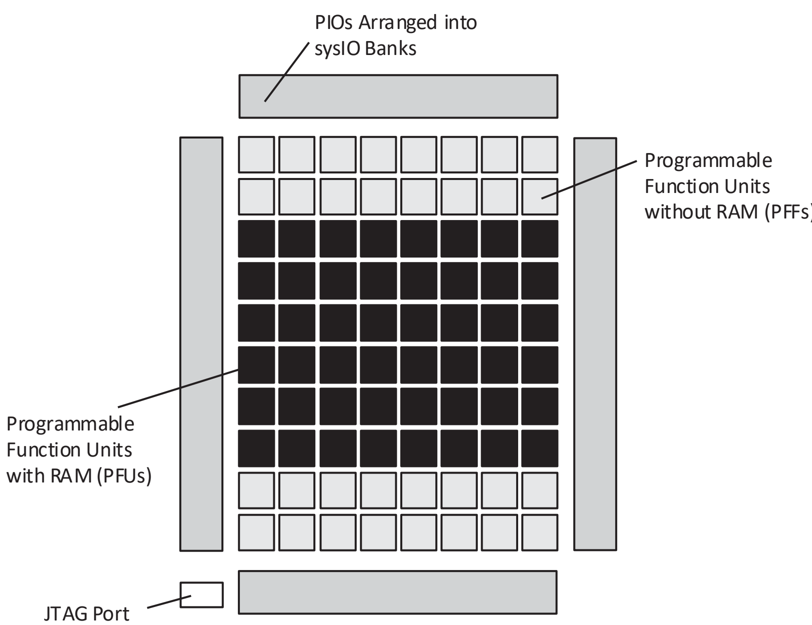


Figure 2.2. Top View of the MachXO640 Device

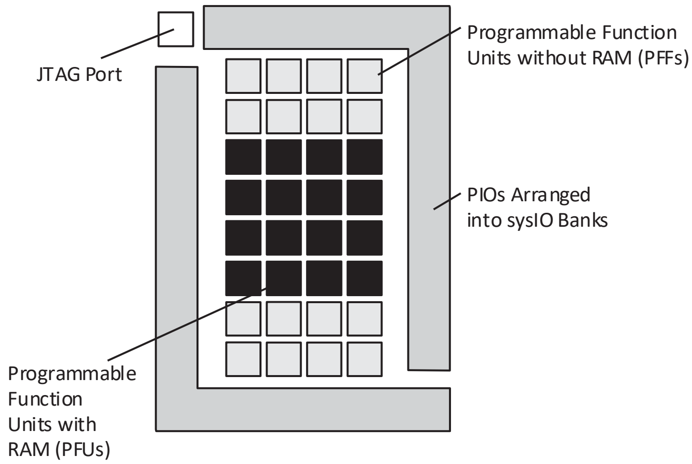


Figure 2.3. Top View of the MachXO256 Device

2.1.1. PFU Blocks

The core of the MachXO devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM, and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic, and Distributed ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected Slices, numbered 0-3 as shown in Figure 2.4. There are 53 inputs and 25 outputs associated with each PFU block.

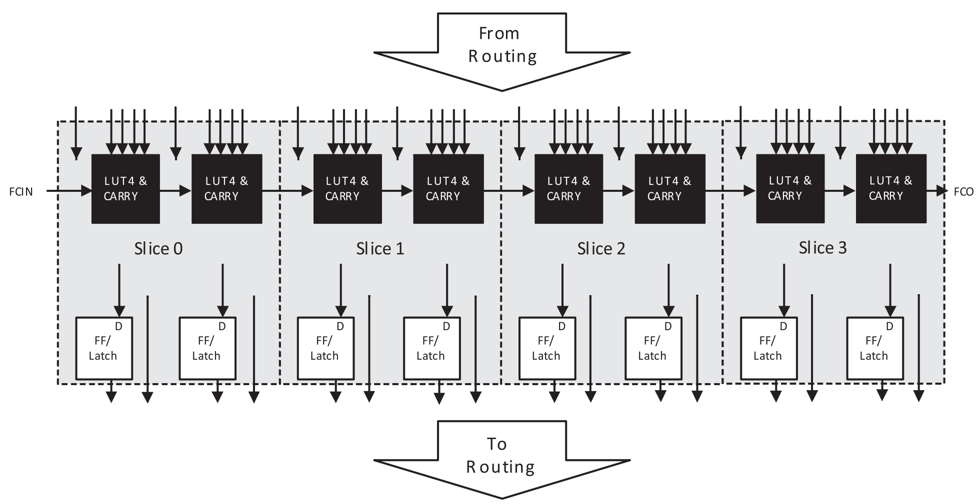
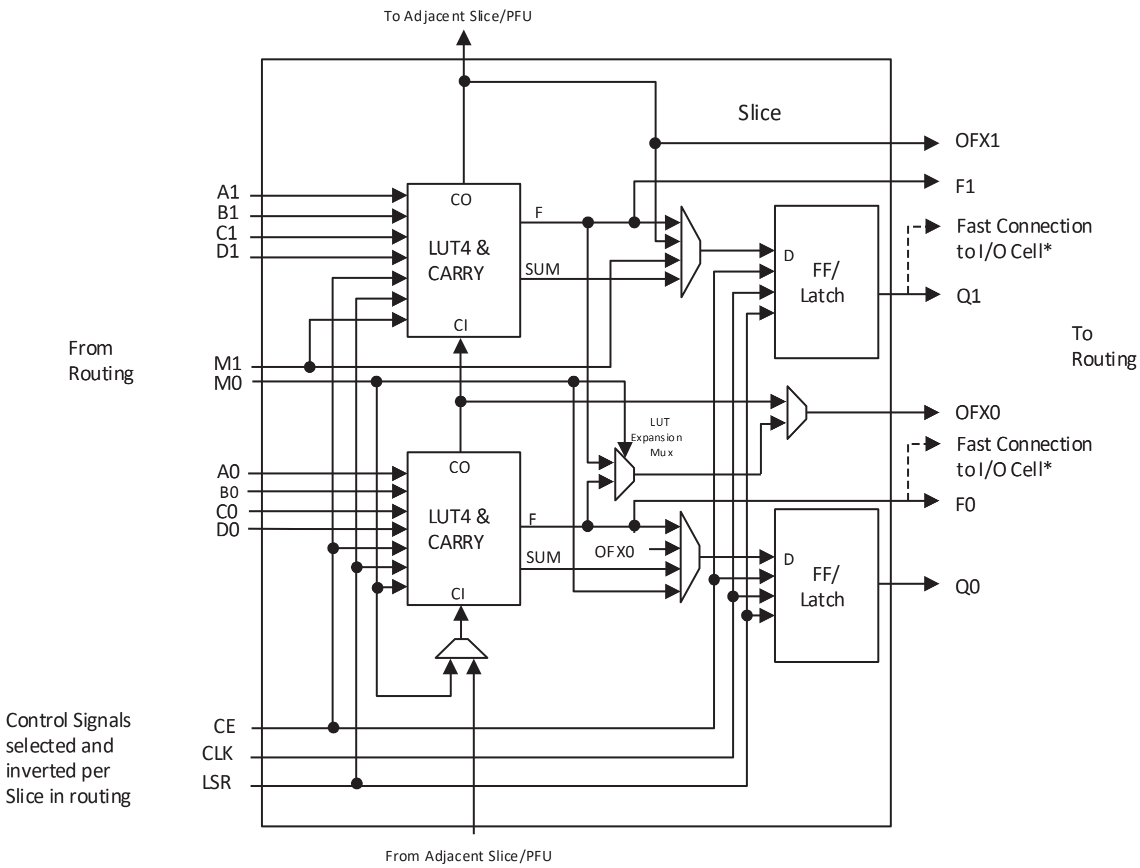


Figure 2.4. PFU Diagram

2.1.2. Slice

Each Slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7, and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select, and wider RAM/ROM functions. Figure 2.5. shows an overview of the internal logic of the Slice. The registers in the Slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent Slice/PFU). There are 7 outputs: 6 to the routing and one to the carry-chain (to the adjacent Slice/PFU). Table 2.1. lists the signals associated with each Slice.



Notes:
Some inter-Slice signals are not shown.
* Only PFUs at the edges have fast connections to the I/O cell.

Figure 2.5. Slice Diagram

Table 2.1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the Slice
Output	Inter-PFU signal	FCO	Fast Carry Out[1]

Notes:

1. See Figure 2.4. for connection details.
2. Requires two PFUs.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2.2. lists the modes and the capability of the Slice blocks.

Table 2.2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
    - A greater-than-or-equal-to B
    - A not-equal-to B
    - A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The ispLEVER design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3. shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in MachXO devices, please see details of additional technical documentation at the end of this data sheet

Table 2.3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

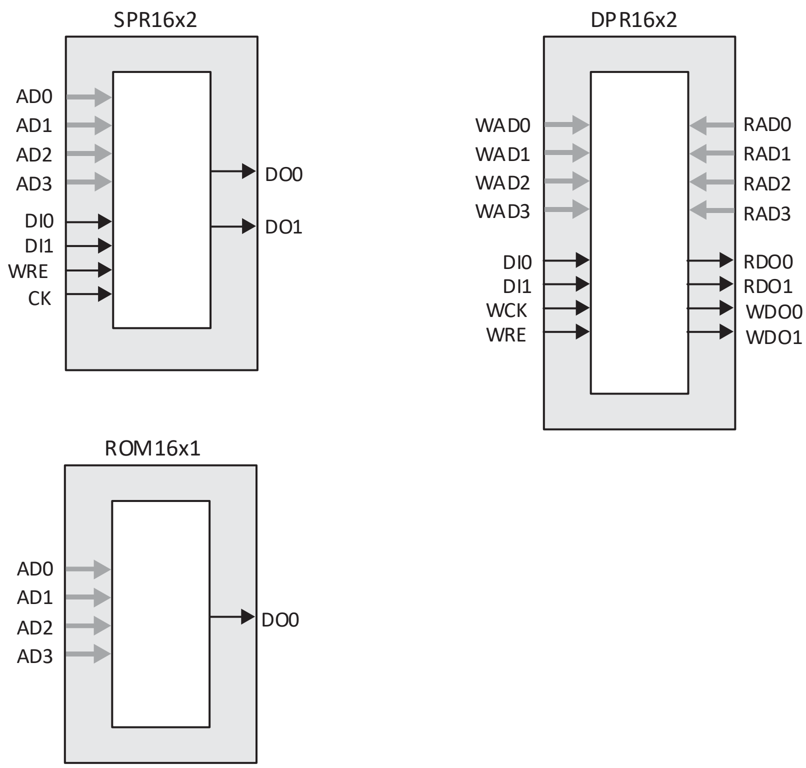


Figure 2.6. Distributed Memory Primitives

ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2.4. tabulates these modes and documents the functionality possible at the PFU level.

Table 2.4. PFU Modes of Operation

Logic	Ripple	RAM	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

2.1.3. Routing

There are many resources provided in the MachXO devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

2.2. Clock/Control Distribution Network

The MachXO family of devices provides global signals that are available to all PFUs. These signals consist of four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 2.7. and Figure 2.8. The available clock sources for the MachXO256 and MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the MachXO1200 and MachXO2280 devices are four dual function clock pins, up to nine internal routing signals and up to six PLL outputs.

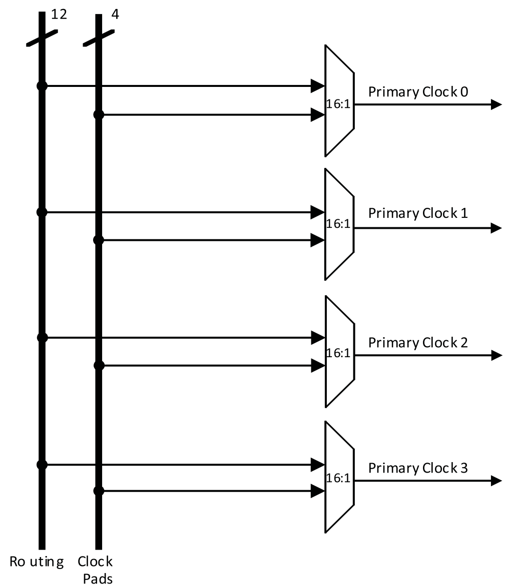


Figure 2.7. Primary Clocks for MachXO256 and MachXO640 Devices

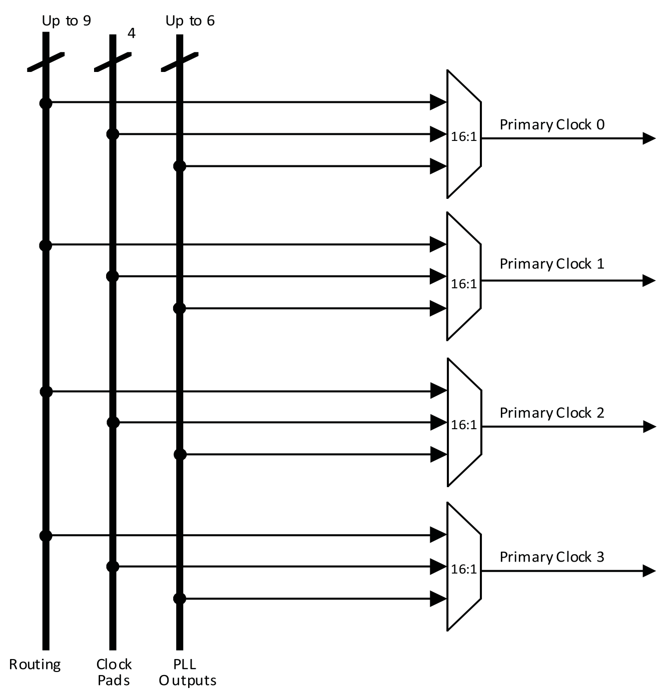


Figure 2.8. Primary Clocks for MachXO1200 and MachXO2280 Devices

Four secondary clocks are generated from four 16:1 muxes as shown in Figure 2.9. Four of the secondary clock sources come from dual function clock pins and 12 come from internal routing.

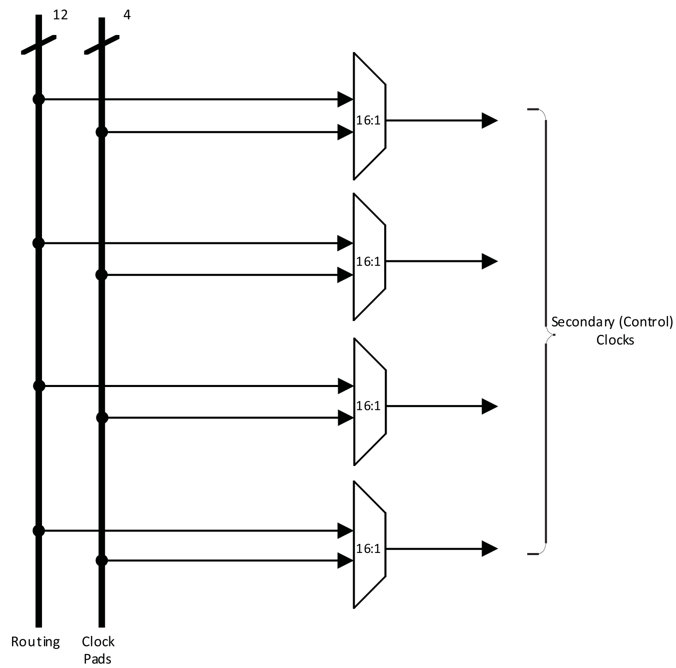


Figure 2.9. Secondary Clocks for MachXO Devices

2.2.1. sysCLOCK Phase Locked Loops (PLLs)

The MachXO1200 and MachXO2280 provide PLL support. The source of the PLL input divider can come from an external pin or from internal routing. There are four sources of feedback signals to the feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from the output of the post scalar divider, and from the routing (or from an external pin). There is a PLL_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 2.10. shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider, and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

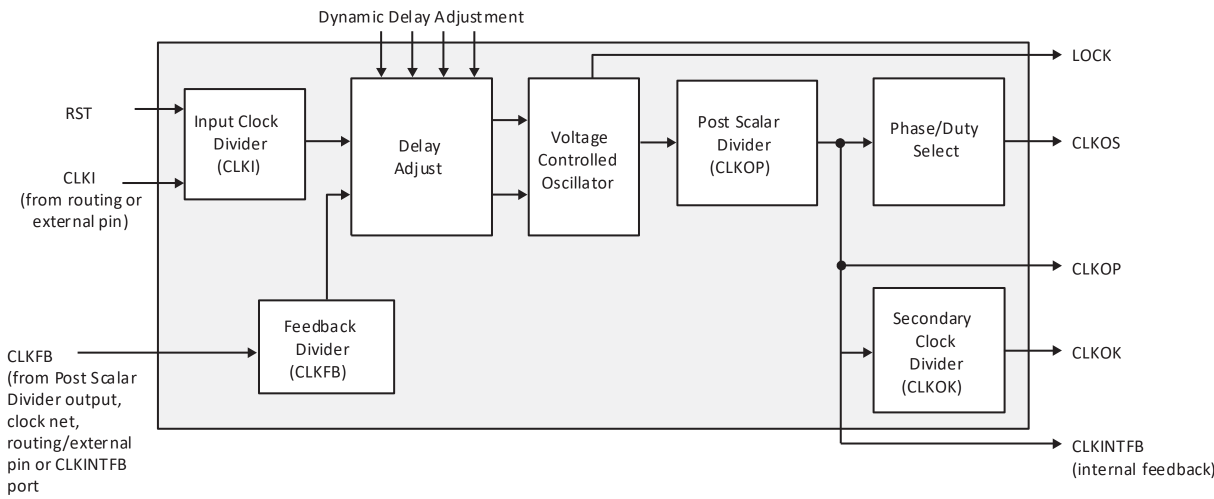


Figure 2.10. PLL Diagram

Figure 2.11. shows the available macros for the PLL. Table 2.5. provides signal description of the PLL Block.

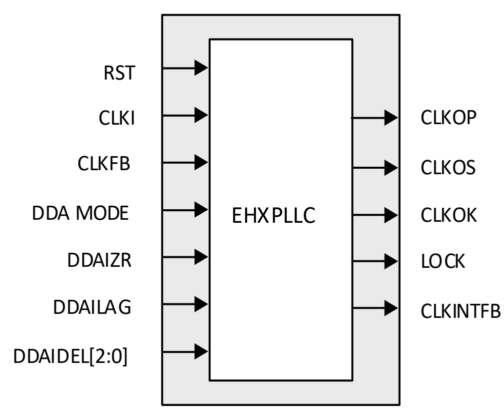


Figure 2.11. PLL Primitive

Table 2.5. PLL Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from PLL output, clock net, routing/external pin or internal feedback from CLKINTFB port
RST	I	"1" to reset the input clock divider
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	"1" indicates PLL LOCK to CLKI
CLKINTFB	O	Internal feedback source, CLKOP divider output before CLOCKTREE
DDAMODE	I	Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. "1": delay = 0, "0": delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. "1": Lag, "0": Lead
DDAIDEL[2:0]	I	Dynamic Delay Input

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

2.3. sysMEM Memory

The MachXO1200 and MachXO2280 devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2.6.

Table 2.6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2.12. shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

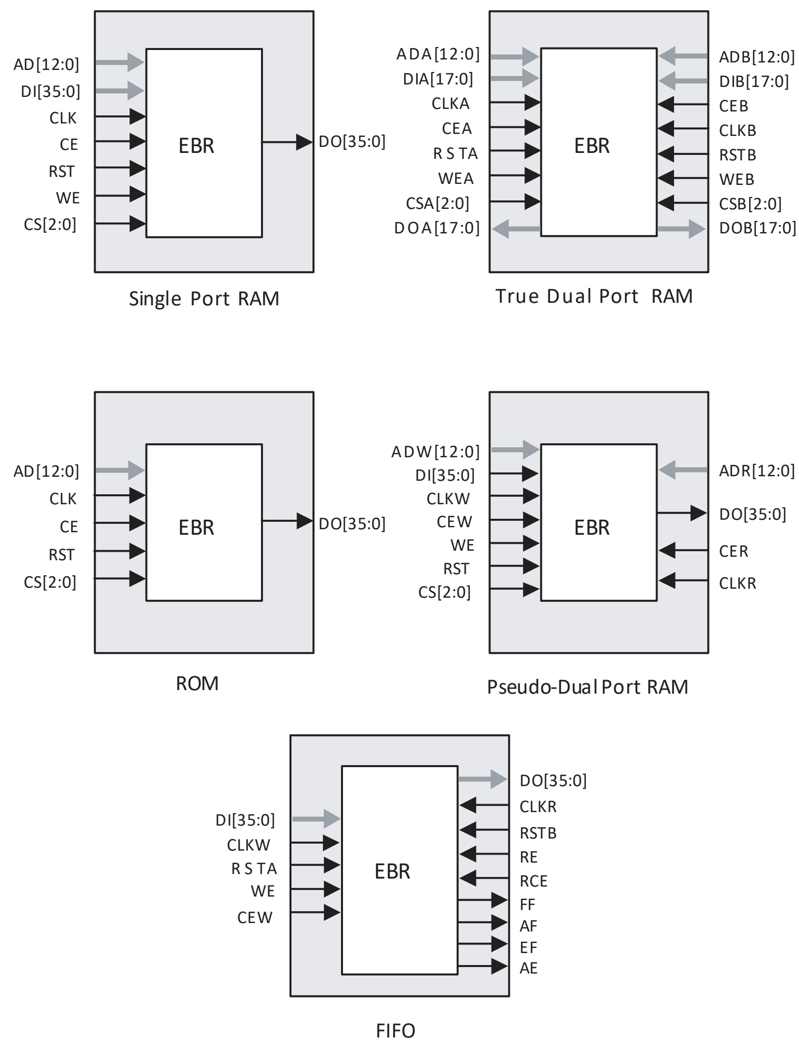


Figure 2.12. sysMEM Memory Primitives

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old contents of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

FIFO Configuration

The FIFO has a write port with Data-in, CEW, WE and CLKW signals. There is a separate read port with Data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. The range of programming values for these flags are in Table 2.7.

Table 2.7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

Note: N = Address bit width

The FIFO state machine supports two types of reset signals: RSTA and RSTB. The RSTA signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RSTB signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2.13.

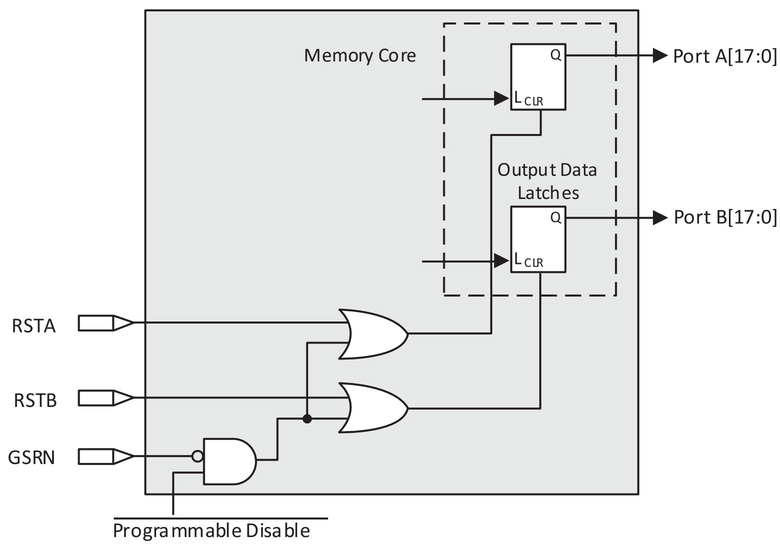


Figure 2.13. Memory Core Reset

For further information on the sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2.14. The GSR input to the EBR is always asynchronous.

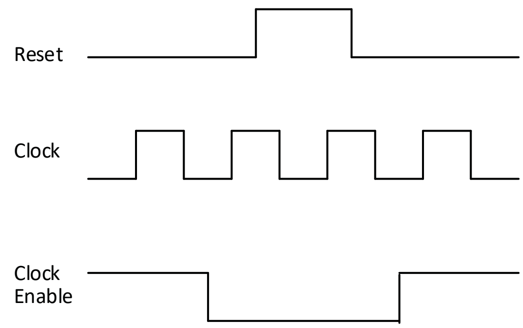


Figure 2.14. EBR Asynchronous Reset (Including GSR) Timing Diagram

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/fMAX (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2.14. The reset timing rules apply to the RPReset input vs the RE input and the RST input vs. the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

2.4. PIO Groups

On the MachXO devices, PIO cells are assembled into two different types of PIO groups, those with four PIO cells and those with six PIO cells. PIO groups with four IOs are placed on the left and right sides of the device while PIO groups with six IOs are placed on the top and bottom. The individual PIO cells are connected to their respective sysIO buffers and PADs.

On all MachXO devices, two adjacent PIOs can be joined to provide a complementary Output driver pair. The I/O pin pairs are labeled as "T" and "C" to distinguish between the true and complement pins.

The MachXO1200 and MachXO2280 devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. In addition, half of the PIO pairs on the left and right sides of these devices can be configured as LVDS transmit/receive pairs. PIOs on the top of these larger devices also provide PCI support.

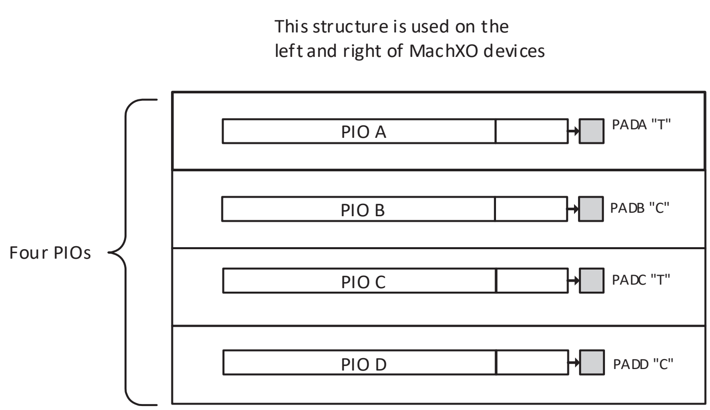


Figure 2.15. Group of Four Programmable I/O Cells

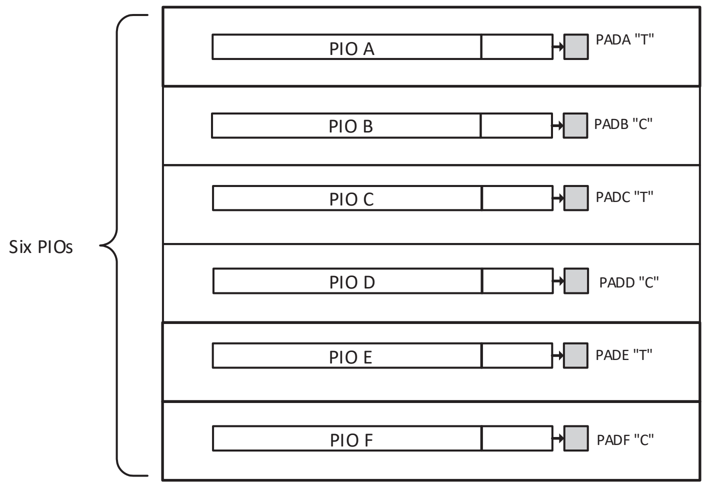


Figure 2.16. Group of Six Programmable I/O Cells

2.4.1. PIO

The PIO blocks provide the interface between the sysIO buffers and the internal PFU array blocks. These blocks receive output data from the PFU array and a fast output data signal from adjacent PFUs. The output data and fast output data signals are multiplexed and provide a single signal to the I/O pin through the sysIO buffer. Figure 2.17. shows the MachXO PIO logic.

The tristate control signal is multiplexed from the output data signals and their complements. In addition a global signal (TSALL) from a dedicated pad can be used to tristate the sysIO buffer.

The PIO receives an input signal from the pin through the sysIO buffer and provides this signal to the core of the device. In addition there are programmable elements that can be utilized by the design tools to avoid positive hold times.

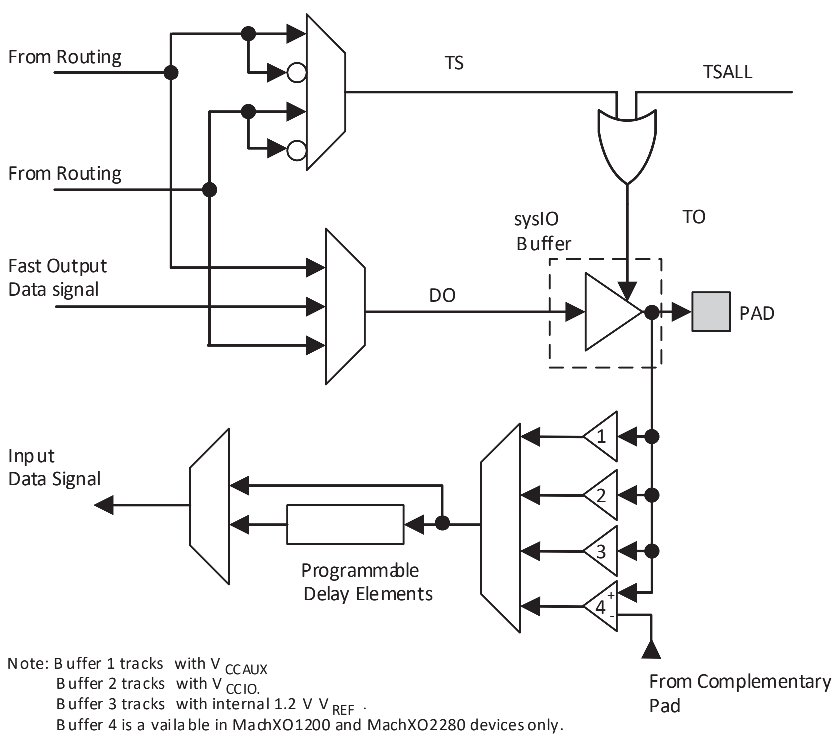


Figure 2.17. MachXO PIO Block Diagram

2.4.2. sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, TTL, BLVDS, LVDS and LVPECL.

In the MachXO devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. In addition to the Bank V_{CCIO} supplies, the MachXO devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that powers up a variety of internal circuits including all the differential and referenced input buffers.

MachXO256 and MachXO640 devices contain single-ended input buffers and single-ended output buffers with complementary outputs on all the I/O Banks.

MachXO1200 and MachXO2280 devices contain two types of sysIO buffer pairs.

1. Top and Bottom sysIO Buffer Pairs

The sysIO buffer pairs in the top and bottom Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (for ratioed or absolute input levels). The I/O pairs on the top and bottom of the devices also support differential input buffers. PCI clamps are available on the top Bank I/O buffers. The PCI clamp is enabled after V_{CC}, V_{CCAUX}, and V_{CCIO} are at valid operating levels and the device has been configured.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

2. Left and Right sysIO Buffer Pairs

The sysIO buffer pairs in the left and right Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (supporting ratioed and absolute input levels). The devices also have a differential driver per output pair. The referenced input buffer can also be configured as a differential input buffer. In these Banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} Banks are active with valid input logic levels to properly control the output logic states of all the I/O Banks that are critical to the application. The default configuration of the I/O pins in a blank device is tristate with a weak pull-up to V_{CCIO}. The I/O pins will maintain the blank configuration until V_{CC}, V_{CCAUX} and V_{CCIO} have reached satisfactory levels at which time the I/Os will take on the user-configured settings.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, the I/O buffers should be powered up along with the FPGA core fabric. Therefore, V_{CCIO} supplies should be powered up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported Standards

The MachXO sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS and LVTTL. The buffer supports the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS and LVPECL output emulation is supported on all devices. The MachXO1200 and MachXO2280 support on-chip LVDS output buffers on approximately 50% of the I/Os on the left and right Banks. Differential receivers for LVDS, BLVDS and LVPECL are supported on all Banks of MachXO1200 and MachXO2280 devices. PCI support is provided in the top Banks of the MachXO1200 and MachXO2280 devices. Table 2.8. summarizes the I/O characteristics of the devices in the MachXO family.

Table 2.9. and Table 2.10. show the I/O standards (together with their supply and reference voltages) supported by the MachXO devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical documentation at the end of this data sheet.

Table 2.8. I/O Support Device by Device

	MachXO256	MachXO640	MachXO1200	MachXO2280
Number of I/O Banks	2	4	8	8
Type of Input Buffers	Single-ended (all I/O Banks)	Single-ended (all I/O Banks)	Single-ended (all I/O Banks) Differential Receivers (all I/O Banks)	Single-ended (all I/O Banks) Differential Receivers (all I/O Banks)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O Banks)	Single-ended buffers with complementary outputs (all I/O Banks)	Single-ended buffers with complementary outputs (all I/O Banks) Differential buffers with true LVDS outputs (50% on left and right side)	Single-ended buffers with complementary outputs (all I/O Banks) Differential buffers with true LVDS outputs (50% on left and right side)
Differential Output Emulation Capability	All I/O Banks	All I/O Banks	All I/O Banks	All I/O Banks
PCI Support	No	No	Top side only	Top side only

Table 2.9. Supported Input Standards

	VCCIO (Typ.)				
Input Standard	**3.3 V**	**2.5 V**	**1.8 V**	**1.5 V**	**1.2 V**
Single Ended Interfaces					
LVTTL	Yes	Yes	Yes	Yes	Yes
LVCMOS33	Yes	Yes	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes	Yes	Yes
LVCMOS18			Yes		
LVCMOS15				Yes	
LVCMOS12	Yes	Yes	Yes	Yes	Yes
PCI[1]	Yes				
Differential Interfaces					
BLVDS[2], LVDS[2], LVPECL[2], RSDS[2]	Yes	Yes	Yes	Yes	Yes

Notes:

1. Top Banks of MachXO1200 and MachXO2280 devices only.
2. MachXO1200 and MachXO2280 devices only.

Table 2.10. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Typ.)
Single-ended Interfaces		
LVTTL	4 mA, 8 mA, 12 mA, 16 mA	3.3
LVCMOS33	4 mA, 8 mA, 12 mA, 14 mA	3.3
LVCMOS25	4 mA, 8 mA, 12 mA, 14 mA	2.5
LVCMOS18	4 mA, 8 mA, 12 mA, 14 mA	1.8
LVCMOS15	4 mA, 8 mA	1.5
LVCMOS12	2 mA, 6 mA	1.2
LVCMOS33, Open Drain	4 mA, 8 mA, 12 mA, 14 mA	—
LVCMOS25, Open Drain	4 mA, 8 mA, 12 mA, 14 mA	—
LVCMOS18, Open Drain	4 mA, 8 mA, 12 mA, 14 mA	—
LVCMOS15, Open Drain	4 mA, 8 mA	—
LVCMOS12, Open Drain	2 mA, 6 mA	—
PCI33[3]	N/A	3.3
Differential Interfaces		
LVDS[1, 2]	N/A	2.5
BLVDS, RSDS[2]	N/A	2.5
LVPECL[2]	N/A	3.3

Notes:

1. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.
3. Top Banks of MachXO1200 and MachXO2280 devices only.

2.4.3. sysIO Buffer Banks

The number of Banks vary between the devices of this family. Eight Banks surround the two larger devices, the MachXO1200 and MachXO2280 (two Banks per side). The MachXO640 has four Banks (one Bank per side). The smallest member of this family, the MachXO256, has only two Banks.

Each sysIO buffer Bank is capable of supporting multiple I/O standards. Each Bank has its own I/O supply voltage (VCCIO) which allows it to be completely independent from the other Banks. Figure 2.18., Figure 2.19., Figure 2.20. and Figure 2.21. shows the sysIO Banks and their associated supplies for all devices.

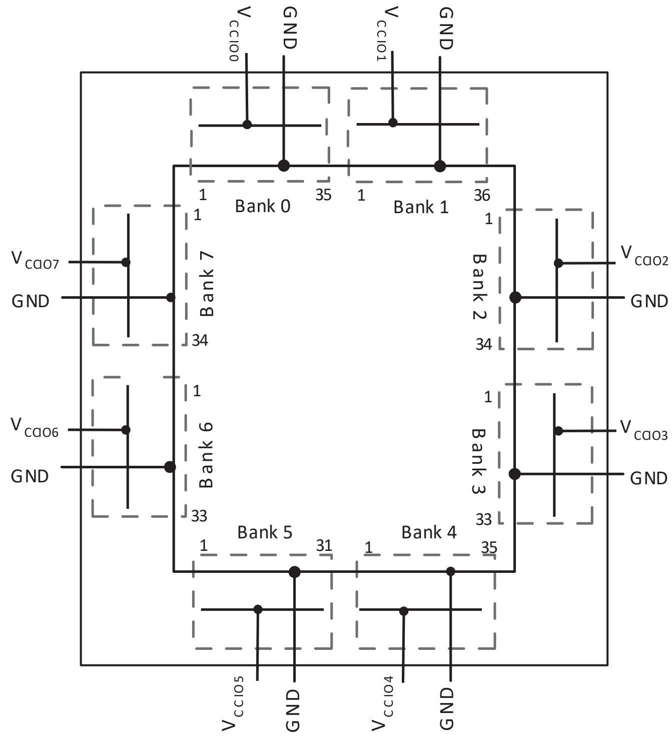


Figure 2.18. MachXO2280 Banks

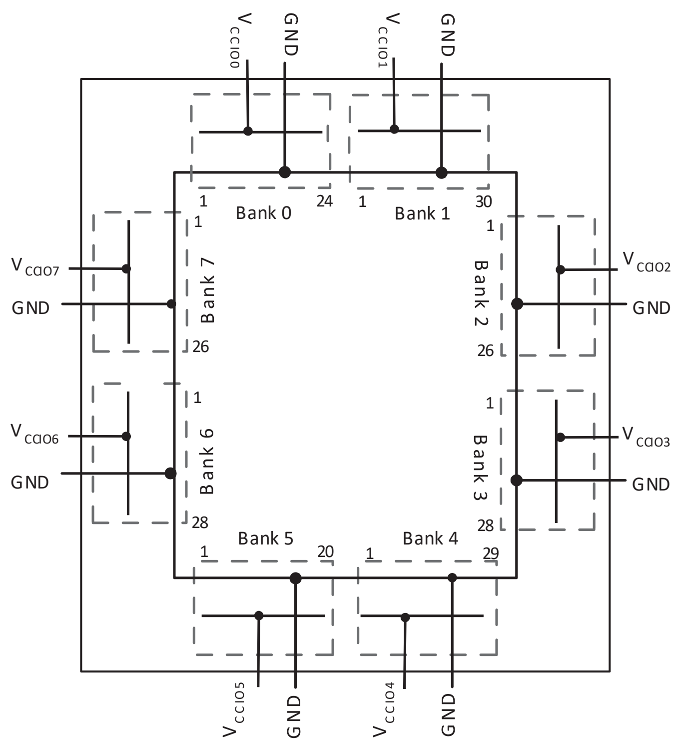


Figure 2.19. MachXO1200 Banks

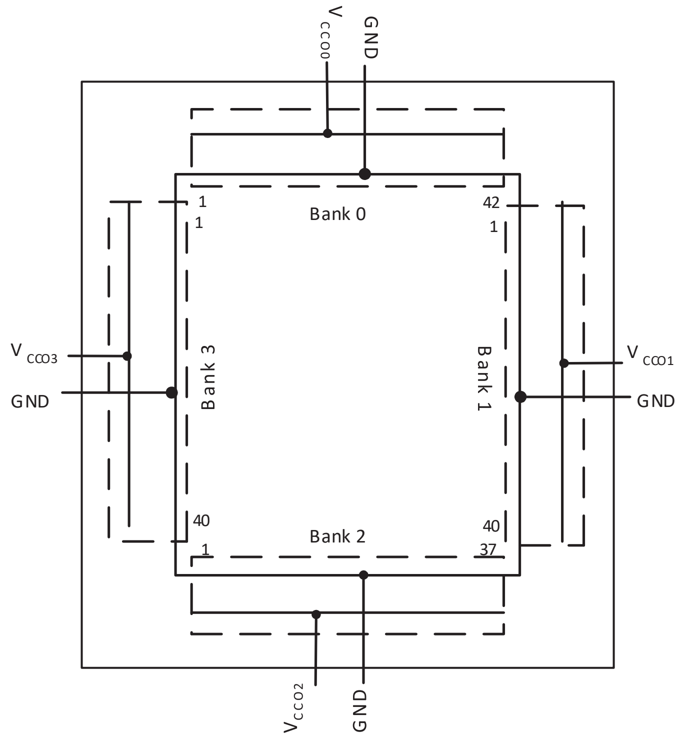


Figure 2.20. MachXO640 Banks

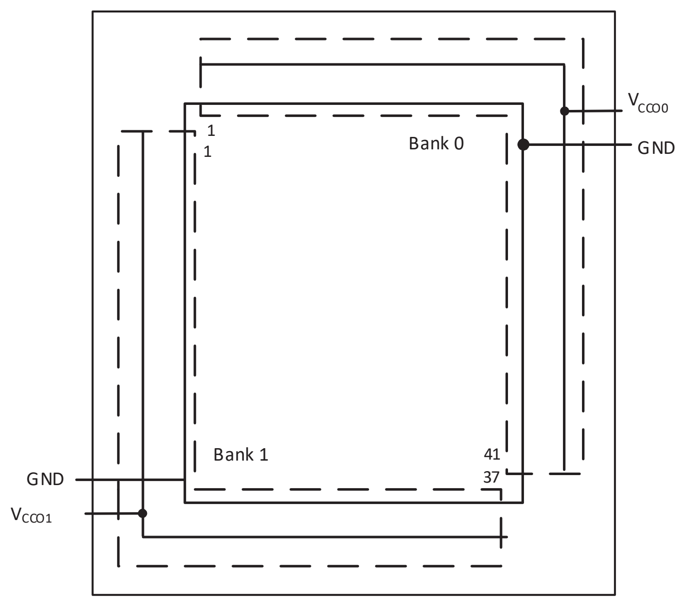


Figure 2.21. MachXO256 Banks

2.5. Hot Socketing

The MachXO devices have been carefully designed to ensure predictable behavior during power-up and powerdown. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO ideal for many multiple power supply and hot-swap applications.

2.6. Sleep Mode

The MachXO "C" devices (V_{CC} = 1.8/2.5/3.3 V) have a sleep mode that allows standby current to be reduced dramatically during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin.

During Sleep mode, the logic is non-operational, registers and EBR contents are not maintained, and I/Os are tristated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 2.11. compares the characteristics of Normal, Off and Sleep modes.

Table 2.11. Characteristics of Normal, Off and Sleep Modes

Characteristic	Normal	Off	Sleep
SLEEPN Pin	High	—	Low
Static Icc	Typical <10 mA	0	Typical <100 uA
I/O Leakage	<10 µA	<1 mA[1]	<10 µA
Power Supplies VCC/VCCIO/VCCAUX	Normal Range	0	Normal Range
Logic Operation	User Defined	Non Operational	Non operational
I/O Operation	User Defined	Tristate	Tristate
JTAG and Programming circuitry	Operational	Non-operational	Non-operational
EBR Contents and Registers	Maintained	Non-maintained	Non-maintained

Note:

1. Hot-socket leakage IDK for standard GPIO. True LVDS capable GPIO IDK_LVDS is higher. See the MachXO1200 and MachXO2280 Hot Socketing Specifications, , section

2.6.1. SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up, along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to VCC is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically, the device enters sleep mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet shows a detailed timing diagram.

2.7. Oscillator

Every MachXO device has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree or to general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator. The oscillator frequency ranges from 18 MHz to 26 MHz.

2.8. Configuration and Testing

The following section describes the configuration and testing features of the MachXO family of devices.

2.8.1. IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with one of the VCCIO Banks (MachXO256: V_{CCIO1}; MachXO640: V_{CCIO2}; MachXO1200 and MachXO2280: V_{CCIO5}) and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

2.8.2. Device Configuration

All MachXO devices contain a test access port that can be used for device configuration and programming.

The non-volatile memory in the MachXO can be configured in two different modes:

- In IEEE 1532 mode through the IEEE 1149.1 port. In this mode, the device is off-line and I/Os are controlled by BSCAN registers.
- In background mode through the IEEE 1149.1 port. This allows the device to remain operational in user mode while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up through the on-chip non-volatile memory.
- After a refresh command is issued through the IEEE 1149.1 port.
- In IEEE 1532 mode through the IEEE 1149.1 port.

Figure 2.22. provides a pictorial representation of the different programming modes available in the MachXO devices. On power-up, the SRAM is ready to be configured with IEEE 1149.1 serial TAP port using IEEE 1532 protocols.

Leave Alone I/O

When using IEEE 1532 mode for non-volatile memory programming, SRAM configuration, or issuing a refresh command, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reconfiguration or reprogramming occurs on-the-fly.

TransFR (Transparent Field Reconfiguration)

TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02025) for details.

Security

The MachXO devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear the security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

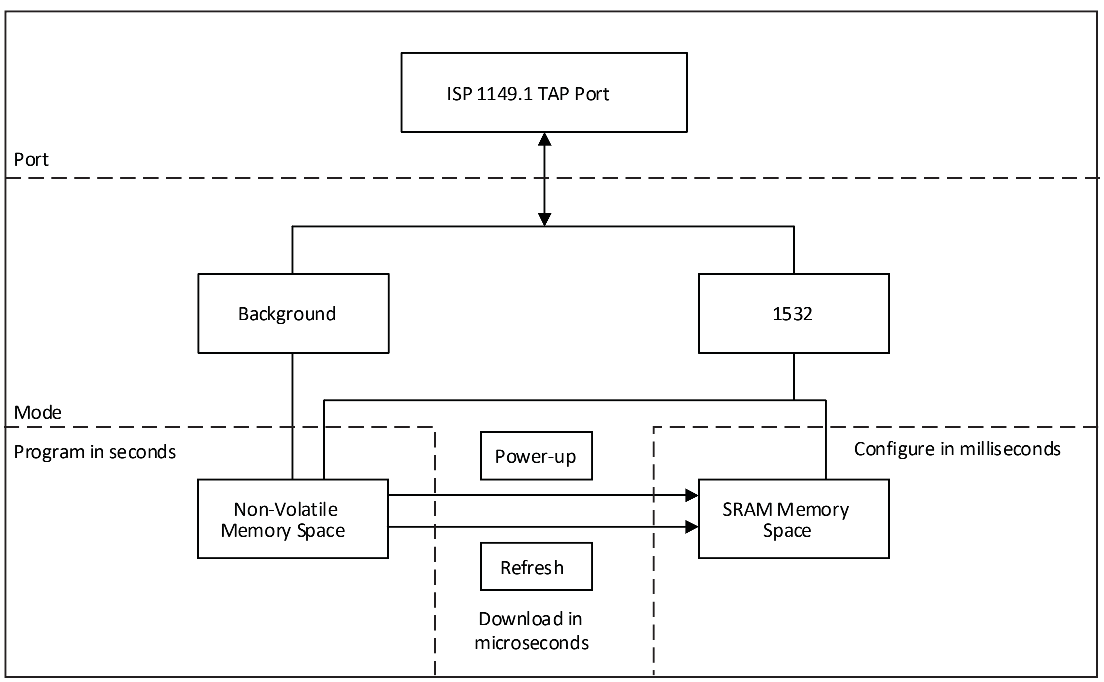


Figure 2.22. MachXO Configuration and Programming

2.9. Density Shifting

The MachXO family has been designed to enable density migration in the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings[1, 2, 3]

	LCMXO E (1.2 V)	LCMXO C (1.8 V / 2.5 V / 3.3 V)
Supply Voltage V_{CC}	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Supply Voltage V_{CCAUX}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tristate Voltage Applied[4]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied[4]	–0.5 V to 3.75 V	–0.5 V to 4.25 V
Storage Temperature (ambient)	–65 °C to 150 °C	–65 °C to 150 °C
Junction Temp. (Tj)	+125 °C	+125 °C

Notes:

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (VIHMAX + 2) volts is permitted for a duration of <20 ns.

3.2. Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 1.8 V / 2.5 V / 3.3 V Devices	1.71	3.465	V
V_{CCAUX}[3]	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCIO}[2]	I/O Driver Supply Voltage	1.14	3.465	V
t_{JCOM}	Junction Temperature Commercial Operation	0	+85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C
$t_{JFLASHCOM}$	Junction Temperature, Flash Programming, Commercial	0	+85	°C
$t_{JFLASHIND}$	Junction Temperature, Flash Programming, Industrial	–40	100	°C

Notes:

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both 2.5 V, they must also be the same supply. 3.3 V V_{CCIO} and 1.2 V V_{CCIO} should be tied to V_{CCAUX} or 1.2 V V_{CC} respectively.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CC} must reach minimum V_{CC} value before V_{CCAUX} reaches 2.5 V.

3.3. MachXO Programming/Erase Specifications

Symbol	Parameter	Min.	Max.	Units
$N_{PROGCYC}$	Flash Programming Cycles per $t_{RETENTION}$		1,000	Cycles
	Flash Functional Programming Cycles		10,000	Cycles
$t_{RETENTION}$	Data Retention at 125° Junction Temperature	10		Years

3.4. MachXO256 and MachXO640 Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Input or I/O leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	+/– 1000	µA

Notes:

1. Insensitive to sequence of VCC, VCCAUX, and VCCIO. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX}, and V_{CCIO}.
2. $0 \leq V_{CC} \leq V_{CC}$ (MAX), $0 \leq V_{CCIO} \leq V_{CCIO}$ (MAX) and $0 \leq V_{CCAUX} \leq V_{CCAUX}$ (MAX).
3. IDK is additive to IPU, IPD or IBH.

3.5. MachXO1200 and MachXO2280 Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Non-LVDS General Purpose sysIOs						
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	+/–1000	µA
LVDS General Purpose sysIOs						
I_{DK_LVDS}	Input or I/O Leakage Current	$V_{IN} \leq V_{CCIO}$	—	—	+/–1000	µA
		$V_{IN} > V_{CCIO}$	—	35	—	mA

Notes:

1. Insensitive to sequence of V_{CC}, V_{CCAUX}, and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX}, and V_{CCIO}.
2. $0 \leq V_{CC} \leq V_{CC}$ (MAX), $0 \leq V_{CCIO} \leq V_{CCIO}$ (MAX), and $0 \leq V_{CCAUX} \leq V_{CCAUX}$ (MAX).
3. IDK is additive to IPU, IPD or IBH.

3.6. DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH} [1, 4, 5]	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2\ V)$	—	—	10	µA
		$(V_{CCIO} - 0.2V) < V_{IN} \leq 3.6\ V$	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7\ V_{CCIO}$	–30	—	–150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\leq V_{IN} \leq V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7\ V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	–150	µA
V_{BHT}[3]	Bus Hold trip Points	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	VIL (MAX)	—	VIH (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Not applicable to SLEEPN pin.
5. When VIH is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the high-to- low transition. For MachXO1200 and MachXO2280 true LVDS output pins, V_{IH} must be less than or equal to V_{CCIO}.

3.7. Supply Current (Sleep Mode)[1, 2]

Symbol	Parameter	Device	Typ.[3]	Max.	Units
I_{CC}	Core Power Supply	LCMXO256C	12	25	µA
		LCMXO640C	12	25	µA
		LCMXO1200C	12	25	µA
		LCMXO2280C	12	25	µA
I_{CCAUX}	Auxiliary Power Supply	LCMXO256C	1	15	µA
		LCMXO640C	1	25	µA
		LCMXO1200C	1	45	µA
		LCMXO2280C	1	85	µA
I_{CCIO}	Bank Power Supply[4]	All LCMXO 'C' Devices	2	30	µA

Notes:

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency = 0 MHz.
3. T_A = 25 °C, power supplies at nominal voltage.
4. Per Bank.

3.8. Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO256C	7	mA
		LCMXO640C	9	mA
		LCMXO1200C	14	mA
		LCMXO2280C	20	mA
		LCMXO256E	4	mA
		LCMXO640E	6	mA
		LCMXO1200E	10	mA
		LCMXO2280E	12	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3 V	LCMXO256E/C	5	mA
		LCMXO640E/C	7	mA
		LCMXO1200E/C	12	mA
		LCMXO2280E/C	13	mA
I_{CCIO}	Bank Power Supply[6]	All devices	2	mA

Notes:

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND.
3. Frequency = 0 MHz.
4. User pattern = blank.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per Bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down

3.9. Initialization Supply Current[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO256C	13	mA
		LCMXO640C	17	mA
		LCMXO1200C	21	mA
		LCMXO2280C	23	mA
		LCMXO256E	10	mA
		LCMXO640E	14	mA
		LCMXO1200E	18	mA
		LCMXO2280E	20	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3 V	LCMXO256E/C	10	mA
		LCMXO640E/C	13	mA
		LCMXO1200E/C	24	mA
		LCMXO2280E/C	25	mA
I_{CCIO}	Bank Power Supply[6]	All devices	2	mA

Notes:

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at V_{CCIO} or GND.
3. Frequency = 0 MHz.
4. Typical user pattern.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per Bank, V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

3.10. Programming and Erase Flash Supply Current[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO256C	9	mA
		LCMXO640C	11	mA
		LCMXO1200C	16	mA
		LCMXO2280C	22	mA
		LCMXO256E	6	mA
		LCMXO640E	8	mA
		LCMXO1200E	12	mA
		LCMXO2280E	14	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3 V	LCMXO256C/E	8	mA
		LCMXO640C/E	10	mA
		LCMXO1200/E	15	mA
		LCMXO2280C/E	16	mA
I_{CCIO}	Bank Power Supply[6]	All devices	2	mA

Notes:

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at V_{CCIO} or GND.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per Bank. VCCIO = 2.5 V. Does not include pull-up/pull-down.

3.11. sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465
LVCMOS 2.5	2.375	2.5	2.625
LVCMOS 1.8	1.71	1.8	1.89
LVCMOS 1.5	1.425	1.5	1.575
LVCMOS 1.2	1.14	1.2	1.26
LVTTL	3.135	3.3	3.465
PCI[3]	3.135	3.3	3.465
LVDS[1, 2]	2.375	2.5	2.625
LVPECL[1]	3.135	3.3	3.465
BLVDS[1]	2.375	2.5	2.625
RSDS[1]	2.375	2.5	2.625

Notes:

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers
3. Input on the top bank of the MachXO1200 and MachXO2280 only.

3.12. sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	–0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	–14, –12, –8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVTTL	–0.3	0.8	2.0	3.6	0.4	2.4	16	–16
					0.4	V_{CCIO} - 0.4	12, 8, 4	–12, –8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	–14, –12, –8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	–14, –12, –8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	–8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 1.2 (“C” Version)	–0.3	0.42	0.78	3.6	0.4	V_{CCIO} - 0.4	6, 2	–6, –2
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 1.2	–0.3			3.6	0.4	V_{CCIO} -	6, 2	–6, –2

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
("E" Version)		$0.35V_{CC}$	$0.65V_{CC}$			0.4		
					0.2	V_{CCIO} - 0.2	0.1	–0.1
PCI	–0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1\ V_{CCIO}$	$0.9\ V_{CCIO}$	1.5	–0.5

Note:

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O Bank and the end of an I/O Bank, as shown in the logic signal connections table shall not exceed n * 8 mA. Where n is the number of I/Os between Bank GND connections or between the last GND in a Bank and the end of a Bank.

3.13. sysIO Differential Electrical Characteristics

3.13.1. LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{THD}	Differential Input Threshold		+/–100	—	—	mV
V_{CM}	Input Common Mode Voltage	100 mV ≤ V_{THD}	$V_{THD}/2$	1.2	1.8	V
		200 mV ≤ V_{THD}	$V_{THD}/2$	1.2	1.9	V
		350 mV ≤ V_{THD}	$V_{THD}/2$	1.2	2.0	V
I_{IN}	Input current	Power on	—	—	+/–10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ω	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ω	0.9 V	1.03	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	6	mA

3.13.2. LVDS Emulation

MachXO devices can support LVDS outputs through emulation (LVDS25E), in addition to the LVDS support that is available on-chip on certain devices. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3.1. is one possible solution for LVDS standard implementation. Resistor values in Figure 3.1. are industry standard values for 1% resistors.

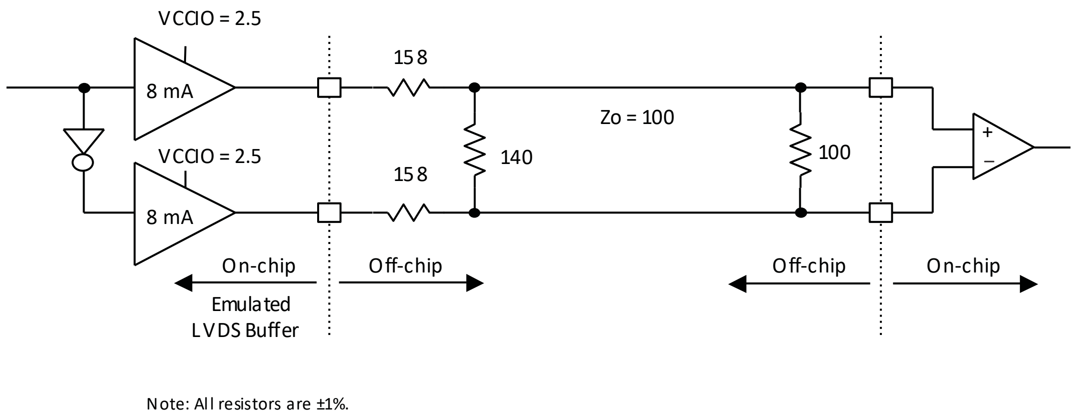


Figure 3.1. LVDS Using External Resistors (LVDS25E)

The LVDS differential input buffers are available on certain devices in the MachXO family.

Table 3.1. LVDS DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	294	Ω
R_P	Driver parallel resistor	121	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100	Ω
I_{DC}	DC output current	3.66	mA

3.13.3. BLVDS

The MachXO family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. The input standard is supported by the LVDS differential input buffer on certain devices. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2. is one possible solution for bi-directional multi-point differential signals.

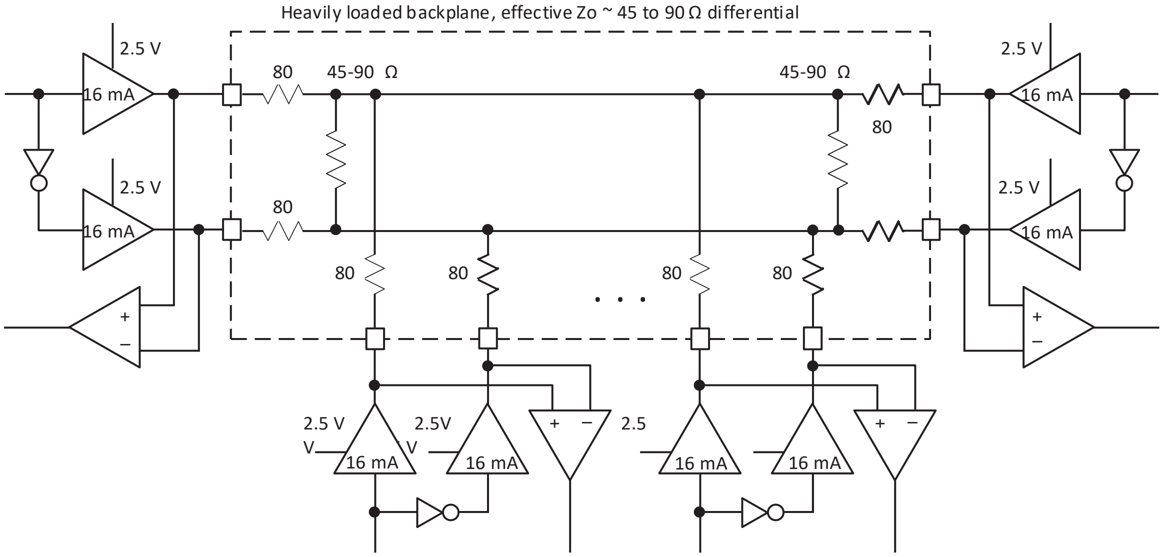


Figure 3.2. BLVDS Multi-point Output Example

Table 3.2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	Ω
R_{TLEFT}	Left end termination	45	90	Ω
R_{TRIGHT}	Right end termination	45	90	Ω
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

Note:

1. For input buffer, see LVDS table.

3.13.4. LVPECL

The MachXO family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3.3. is one possible solution for point-to-point signals.

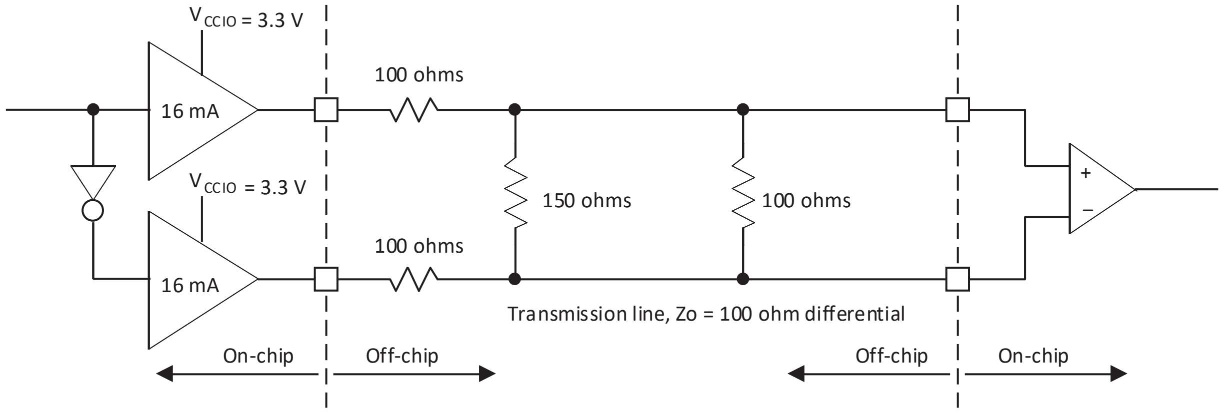


Figure 3.3. Differential LVPECL

Table 3.3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	100	Ω
R_P	Driver parallel resistor	150	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	2.03	V
V_{OL}	Output low voltage	1.27	V
V_{OD}	Output differential voltage	0.76	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	85.7	Ω
I_{DC}	DC output current	12.7	mA

Note:

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

3.13.5. RSDS

The MachXO family supports the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3.4. is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3.4. are industry standard values for 1% resistors.

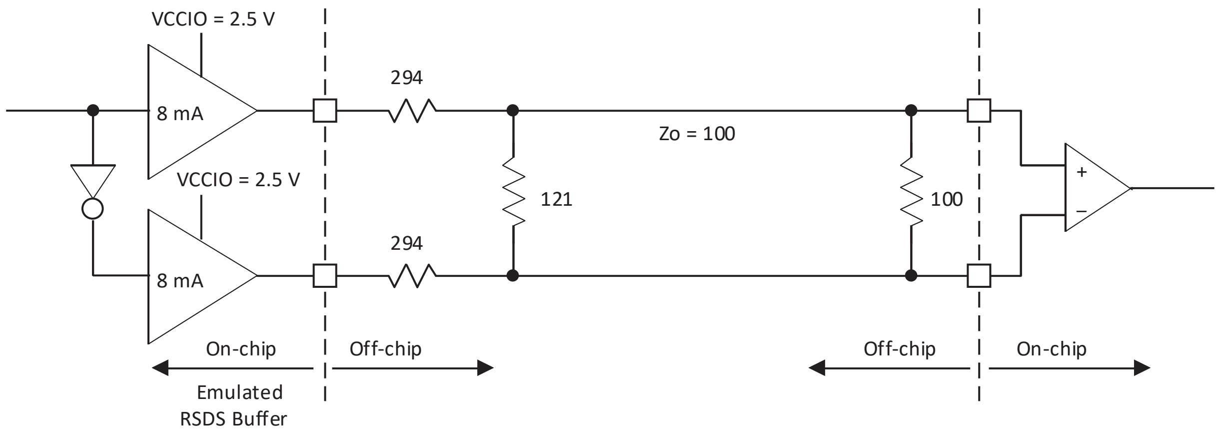


Figure 3.4. RSDS (Reduced Swing Differential Standard)

Table 3.4. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	294	Ω
R_P	Driver parallel resistor	121	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ω
I_{DC}	DC output current	3.66	mA

3.14. Typical Building Block Function Performance[1]

3.14.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–5 Timing	Units
Basic Functions		
16-bit decoder	6.7	ns
4:1 MUX	4.5	ns
16:1 MUX	5.1	ns

3.14.2. Register-to-Register Performance

Function	–5 Timing	Units
Basic Functions		
16:1 MUX	487	MHz
16-bit adder	292	MHz
16-bit counter	388	MHz
64-bit counter	200	MHz
Embedded Memory Functions (1200 and 2280 Devices Only)		
256x36 Single Port RAM	284	MHz
512x18 True-Dual Port RAM	284	MHz

Distributed Memory Functions		
16x2 Single Port RAM	434	MHz
64x2 Single Port RAM	320	MHz
128x4 Single Port RAM	261	MHz
32x2 Pseudo-Dual Port RAM	314	MHz
64x4 Pseudo-Dual Port RAM	271	MHz

Note:

1. The above timing numbers are generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Rev. A 0.19

3.15. Derating Logic Timing

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst case numbers in the operating range. Actual delays may be much faster. The ispLEVER design tool from Lattice can provide logic timing numbers at a particular temperature and voltage.

3.16. MachXO External Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	Device	–5		–4		–3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Global Clock without PLL)[1]									
t_{PD}	Best Case t_{PD} Through 1 LUT	LCMXO256	—	3.5	—	4.2	—	4.9	ns
		LCMXO640	—	3.5	—	4.2	—	4.9	ns
		LCMXO1200	—	3.6	—	4.4	—	5.1	ns
		LCMXO2280	—	3.6	—	4.4	—	5.1	ns
t_{CO}	Best Case Clock to Output - From PFU	LCMXO256	—	4.0	—	4.8	—	5.6	ns
		LCMXO640	—	4.0	—	4.8	—	5.7	ns
		LCMXO1200	—	4.3	—	5.2	—	6.1	ns
		LCMXO2280	—	4.3	—	5.2	—	6.1	ns
t_{SU}	Clock to Data Setup - To PFU	LCMXO256	1.3	—	1.6	—	1.8	—	ns
		LCMXO640	1.1	—	1.3	—	1.5	—	ns
		LCMXO1200	1.1	—	1.3	—	1.6	—	ns
		LCMXO2280	1.1	—	1.3	—	1.5	—	ns
t_H	Clock to Data Hold - To PFU	LCMXO256	–0.3	—	–0.3	—	–0.3	—	ns
		LCMXO640	–0.1	—	–0.1	—	–0.1	—	ns
		LCMXO1200	0.0	—	0.0	—	0.0	—	ns
		LCMXO2280	–0.4	—	–0.4	—	–0.4	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LCMXO256	—	600	—	550	—	500	MHz
		LCMXO640	—	600	—	550	—	500	MHz
		LCMXO1200	—	600	—	550	—	500	MHz
		LCMXO2280	—	600	—	550	—	500	MHz
t_{SKEW_PRI}	Global Clock Skew Across Device	LCMXO256	—	200	—	220	—	240	ps
		LCMXO640	—	200	—	220	—	240	ps
		LCMXO1200	—	220	—	240	—	260	ps
		LCMXO2280	—	220	—	240	—	260	ps

Note:

1. General timing numbers based on LVCMOS 2.5 V, 12 mA.
   Rev. A 0.19

3.17. MachXO Internal Timing Parameters[1]

Over Recommended Operating Conditions

Parameter	Description	–5		–4		–3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.28	—	0.34	—	0.39	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.44	—	0.53	—	0.62	ns
t_{LSR_PFU}	Set/Reset to output of PFU	—	0.90	—	1.08	—	1.26	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) input setup time	0.10	—	0.13	—	0.15	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) input hold time	–0.05	—	–0.06	—	–0.07	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.13	—	0.16	—	0.18	—	ns
t_{HD_PFU}	Clock to D input hold time	–0.03	—	–0.03	—	–0.04	—	ns
t_{CK2Q_PFU}	Clock to Q delay, D-type register configuration	—	0.40	—	0.48	—	0.56	ns
t_{LE2Q_PFU}	Clock to Q delay latch configuration	—	0.53	—	0.64	—	0.74	ns
t_{LD2Q_PFU}	D to Q throughput delay when latch is enabled	—	0.55	—	0.66	—	0.77	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output	—	0.40	—	0.48	—	0.56	ns
t_{SUDATA_PFU}	Data Setup Time	–0.18	—	–0.22	—	–0.25	—	ns
t_{HDATA_PFU}	Data Hold Time	0.28	—	0.34	—	0.39	—	ns
t_{SUADDR_PFU}	Address Setup Time	–0.46	—	–0.56	—	–0.65	—	ns
t_{HADDR_PFU}	Address Hold Time	0.71	—	0.85	—	0.99	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	–0.22	—	–0.26	—	–0.30	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.33	—	0.40	—	0.47	—	ns
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay	—	0.75	—	0.90	—	1.06	ns
t_{OUT_PIO}	Output Buffer Delay	—	1.29	—	1.54	—	1.80	ns
EBR Timing (1200 and 2280 Devices Only)								
t_{CO_EBR}	Clock to output from Address or Data with no output register	—	2.24	—	2.69	—	3.14	ns
t_{COO_EBR}	Clock to output from EBR output Register	—	0.54	—	0.64	—	0.75	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	–0.26	—	–0.31	—	–0.37	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.41	—	0.49	—	0.57	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	–0.26	—	–0.31	—	–0.37	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.41	—	0.49	—	0.57	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	–0.17	—	–0.20	—	–0.23	—	ns
t_{HWREN_EBR}	Hold Write/Read Enable to EBR Memory	0.26	—	0.31	—	0.36	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.19	—	0.23	—	0.27	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	–0.13	—	–0.16	—	–0.18	—	ns

Parameter	Description	–5		–4		–3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.03	—	1.23	—	1.44	ns
PLL Parameters (1200 and 2280 Devices Only)								
t_{RSTREC}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
t_{RSTSU}	Reset Signal Setup Time	1.00	—	1.00	—	1.00	—	ns

Note:

1. Internal parameters are characterized but not tested on every device.
   Rev. A 0.19

3.18. MachXO Family Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description	–5	–4	–3	Units
Input Adjusters					
LVDS25[4]	LVDS	0.44	0.53	0.61	ns
BLVDS25[4]	BLVDS	0.44	0.53	0.61	ns
LVPECL33[4]	LVPECL	0.42	0.50	0.59	ns
LVTTL33	LVTTL	0.01	0.01	0.01	ns
LVCMOS33	LVCMOS 3.3	0.01	0.01	0.01	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	0.07	0.08	0.10	ns
LVCMOS15	LVCMOS 1.5	0.14	0.17	0.19	ns
LVCMOS12	LVCMOS 1.2	0.40	0.48	0.56	ns
PCI33[4]	PCI	0.01	0.01	0.01	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E	–0.13	–0.15	–0.18	ns
LVDS25[4]	LVDS 2.5	–0.21	–0.26	–0.30	ns
BLVDS25	BLVDS 2.5	–0.03	–0.03	–0.04	ns
LVPECL33	LVPECL 3.3	0.04	0.04	0.05	ns
LVTTL33_4mA	LVTTL 4 mA drive	0.04	0.04	0.05	ns
LVTTL33_8mA	LVTTL 8 mA drive	0.06	0.07	0.08	ns
LVTTL33_12mA	LVTTL 12 mA drive	–0.01	–0.01	–0.01	ns
LVTTL33_16mA	LVTTL 16 mA drive	0.50	0.60	0.70	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive	0.04	0.04	0.05	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive	0.06	0.07	0.08	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive	–0.01	–0.01	–0.01	ns
LVCMOS33_14mA	LVCMOS 3.3 14 mA drive	0.50	0.60	0.70	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive	0.05	0.06	0.07	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive	0.10	0.12	0.13	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive	0.00	0.00	0.00	ns
LVCMOS25_14mA	LVCMOS 2.5 14 mA drive	0.34	0.40	0.47	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive	0.11	0.13	0.15	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive	0.05	0.06	0.06	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive	–0.06	–0.07	–0.08	ns
LVCMOS18_14mA	LVCMOS 1.8 14 mA drive	0.06	0.07	0.09	ns
LVCMOS15_4mA	LVCMOS 1.5 4 mA drive	0.15	0.19	0.22	ns
LVCMOS15_8mA	LVCMOS 1.5 8 mA drive	0.05	0.06	0.07	ns

Buffer Type	Description	–5	–4	–3	Units
LVCMOS12_2mA	LVCMOS 1.2 2 mA drive	0.26	0.31	0.36	ns
LVCMOS12_6mA	LVCMOS 1.2 6 mA drive	0.05	0.06	0.07	ns
PCI33[4]	PCI33	1.85	2.22	2.59	ns

Notes:

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing is measured with the load specified in Switching Test Conditions table.
3. All other standards tested according to the appropriate specifications.
4. I/O standard only available in LCMXO1200 and LCMXO2280 devices.

   Rev. A 0.19

3.19. sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	420	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4[5, 6]	18	25	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	420	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	210	MHz
f_{VCO}	PLL VCO Frequency		420	840	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	MHz
		Input Divider (M) = 1; Feedback Divider (N) <= 4[5, 6]	18	25	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected[3]	45	55	%
t_{PH}[4]	Output Phase Accuracy		—	0.05	UI
t[1] OPJIT	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	+/– 120	ps
		f_{OUT} < 100 MHz	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	+/– 200	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	1	—	ns
t_{LOCK}[2]	PLL Lock-in Time		—	150	µs
t_{PA}	Programmable Delay Unit		100	450	ps
t_{IPJIT}	Input Clock Period Jitter	$f_{OUT} \geq$ 100 MHz	—	+/– 200	ps
		f_{OUT} < 100 MHz	—	0.02	UI
t_{FBKDLY}	External Feedback Delay		—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{RST}	RST Pulse Width		10	—	ns

Notes:

1. Jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock.
2. Output clock is valid after tLOCK for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output.
5. When using an input frequency less than 25 MHz the output frequency must be less than or equal to 4 times the input frequency.

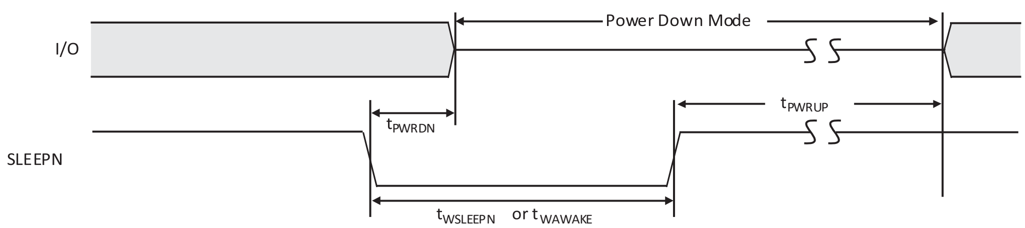
6. The on-chip oscillator can be used to provide reference clock input to the PLL provided the output frequency restriction for clock inputs below 25 MHz are followed.
Rev. A 0.19

3.20. MachXO "C" Sleep Mode Timing

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	SLEEPN Low to Power Down	All	—	—	400	ns
t_{PWRUP}	SLEEPN High to Power Up	LCMXO256	—	—	400	µs
		LCMXO640	—	—	600	µs
		LCMXO1200	—	—	800	µs
		LCMXO2280	—	—	1000	µs
$t_{WSLEEPN}$	SLEEPN Pulse Width	All	400	—	—	ns
t_{WAWAKE}	SLEEPN Pulse Rejection	All	—	—	100	ns

Note: Rev. A 0.19

3.21. Flash Download Time



Symbol	Parameter		Min.	Typ.	Max.	Units
$t_{REFRESH}$	Minimum V_{CC} or V_{CCAUX} (later of the two supplies) to Device I/O Active	LCMXO256	—	—	0.4	ms
		LCMXO640	—	—	0.6	ms
		LCMXO1200	—	—	0.8	ms
		LCMXO2280	—	—	1.0	ms

3.22. JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK [BSCAN] clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to output valid	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to output disabled	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to output enabled	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to output valid	—	25	ns

Symbol	Parameter	Min.	Max.	Units
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to output disabled	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to output enabled	—	25	ns

Note: Rev. A 0.19

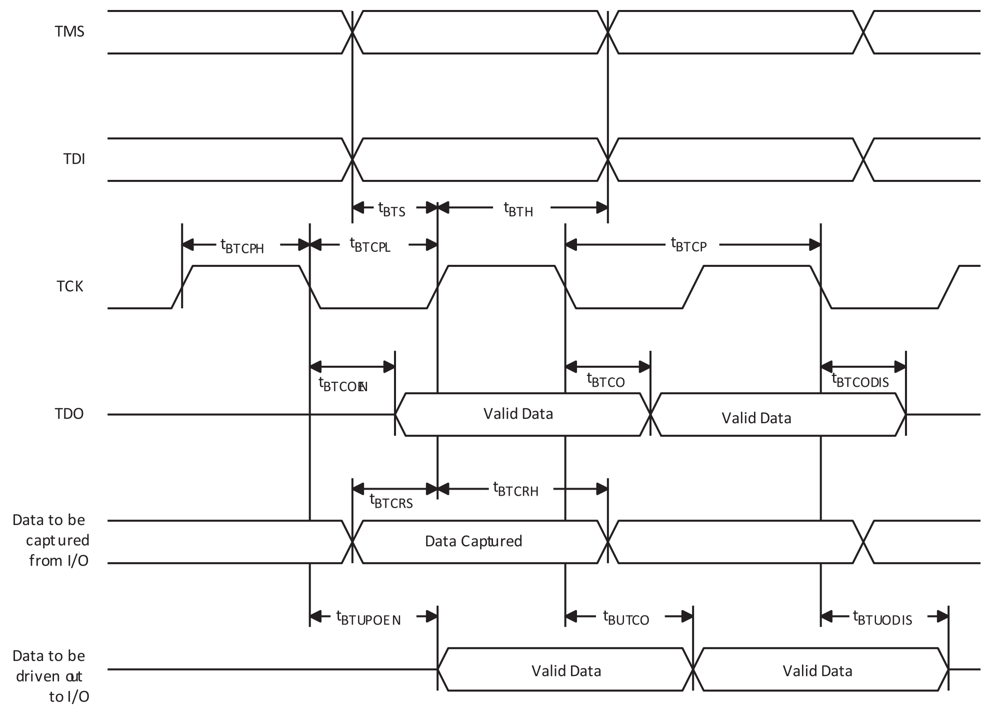


Figure 3.5. JTAG Port Timing Waveforms

3.23. Switching Test Conditions

Figure 3.6. shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3.5.

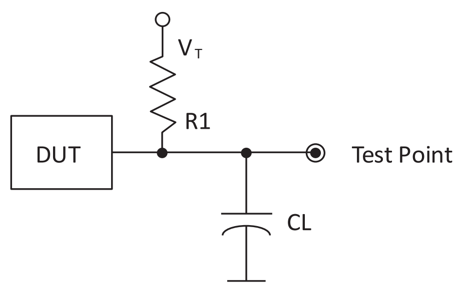


Figure 3.6. Output Test Load, LVTTL and LVCMOS Standards

Table 3.5. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)				V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTL + LVCMOS (H -> Z)			V_{OH} - 0.15	V_{OL}
LVTTL + LVCMOS (L -> Z)			V_{OL} - 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

4. Pinout Information

4.1. Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D/E/F]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D/E/F] indicates the PIO within the group to which the pad is connected. Some of these user programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic. During configuration of the user-programmable I/Os, the user has an option to tristate the I/Os and enable an internal pull-up resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tristated with an internal pull-up resistor enabled. When the device is erased, I/Os will be tristated with an internal pull-up resistor enabled.
GSRN	I	Global RESET signal (active low). Dedicated pad, when not in use it can be used as an I/O pin.
TSALL	I	TSALL is a dedicated pad for the global output enable signal. When TSALL is high all the outputs are tristated. It is a dual function pin. When not in use, it can be used as an I/O pin.
NC	—	No connect.
GND	—	GND - Ground. Dedicated pins.
V_{CC}	—	VCC - The power supply pins for core logic. Dedicated pins.
V_{CCAUX}	—	VCCAUX - the Auxiliary power supply pin. This pin powers up a variety of internal circuits including all the differential and referenced input buffers. Dedicated pins.
V_{CCIOx}	—	V_{CCIO} - The power supply pins for I/O Bank x. Dedicated pins.
SLEEPN[1]	I	Sleep Mode pin - Active low sleep pin. When this pin is held high, the device operates normally. This pin has a weak internal pull-up, but when unused, an external pull-up to V_{CC} is recommended. When driven low, the device moves into Sleep mode after a specified time.
PLL and Clock Functions (Used as user programmable I/O pins when not used for PLL or clock pins)		
[LOC][0]_PLL[T, C]_IN	—	Reference clock (PLL) input Pads: [LOC] indicates location. Valid designations are ULM (Upper PLL) and LLM (Lower PLL). T = true and C = complement.
[LOC][0]_PLL[T, C]_FB	—	Optional feedback (PLL) input Pads: [LOC] indicates location. Valid designations are ULM (Upper PLL) and LLM (Lower PLL). T = true and C = complement.
PCLK [n]_[1:0]	—	Primary Clock Pads, n per side.
Test and Programming (Dedicated pins)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin -Test Data output pin used to shift data out of the device using 1149.1.

Note:

1. Applies to MachXO "C" devices only. NC for "E" devices.

4.2. Pin Information Summary

Pin Type		LCMXO256C/E		LCMXO640C/E				
		100 TQFP	100 csBGA	100 TQFP	144 TQFP	100 csBGA	132 csBGA	256 caBGA / 256 ftBGA
Single Ended User I/O		78	78	74	113	74	101	159
Differential Pair User I/O[1]		38	38	17	43	17	42	79
Muxed		6	6	6	6	6	6	6
TAP		4	4	4	4	4	4	4
Dedicated (Total Without Supplies)		5	5	5	5	5	5	5
VCC		2	2	2	4	2	4	4
VCCAUX		1	1	1	2	1	2	2
VCCIO	Bank0	3	3	2	2	2	2	4
	Bank1	3	3	2	2	2	2	4
	Bank2	—	—	2	2	2	2	4
	Bank3	—	—	2	2	2	2	4
GND		8	8	10	12	10	12	18
NC		0	0	0	0	0	0	52
Single Ended/Differential I/O per Bank	Bank0	41/20	41/20	18/5	29/10	18/5	26/11	42/21
	Bank1	37/18	37/18	21/4	30/11	21/4	27/12	40/20
	Bank2	—	—	14/2	24/9	14/2	21/9	36/18
	Bank3	—	—	21/6	30/13	21/6	27/10	40/20

Note:

1. These devices support emulated LVDS outputs. LVDS inputs are not supported.

Pin Type		LCMXO1200C/E				LCMXO2280C/E				
		100 TQFP	144 TQFP	132 csBGA	256 caBGA / 256 ftBGA	100 TQFP	144 TQFP	132 csBGA	256 caBGA / 256 ftBGA	324 ftBGA
Single Ended User I/O		73	113	101	211	73	113	101	211	271
Differential Pair User I/O[1]		27	48	42	105	30	47	41	105	134
Muxed		6	6	6	6	6	6	6	6	6
TAP		4	4	4	4	4	4	4	4	4
Dedicated (Total Without Supplies)		5	5	5	5	5	5	5	5	5
VCC		4	4	4	4	2	4	4	4	6
VCCAUX		2	2	2	2	2	2	2	2	2
VCCIO	Bank0	1	1	1	2	1	1	1	2	2
	Bank1	1	1	1	2	1	1	1	2	2
	Bank2	1	1	1	2	1	1	1	2	2
	Bank3	1	1	1	2	1	1	1	2	2
	Bank4	1	1	1	2	1	1	1	2	2
	Bank5	1	1	1	2	1	1	1	2	2
	Bank6	1	1	1	2	1	1	1	2	2
	Bank7	1	1	1	2	1	1	1	2	2
GND		8	12	12	18	8	12	12	18	24
NC		0	0	0	0	0	0	0	0	0
Single Ended/Differential I/O per Bank	Bank0	10/3	14/6	13/5	26/13	9/3	13/6	12/5	24/12	34/17
	Bank1	8/2	15/7	13/5	28/14	9/3	16/7	14/5	30/15	36/18
	Bank2	10/4	15/7	13/6	26/13	10/4	15/7	13/6	26/13	34/17
	Bank3	11/5	15/7	14/7	28/14	11/5	15/7	14/7	28/14	34/17
	Bank4	8/3	14/5	13/5	27/13	8/3	14/4	13/4	29/14	35/17
	Bank5	5/2	10/4	8/2	22/11	5/2	10/4	8/2	20/10	30/15
	Bank6	10/3	15/6	13/6	28/14	10/4	15/6	13/6	28/14	34/17
	Bank7	11/5	15/6	14/6	26/13	11/5	15/6	14/6	26/13	34/17

Note:

1. These devices support on-chip LVDS buffers for left and right I/O Banks.

4.3. Power Supply and NC

Signal	100 TQFP[1]	144 TQFP[1]	100 csBGA[2]
VCC	**LCMXO256/640**: 35, 90 **LCMXO1200/2280**: 17, 35, 66, 91	21, 52, 93, 129	P7, B6
VCCIO0	**LCMXO256**: 60, 74, 92 **LCMXO640**: 80, 92 **LCMXO1200/2280**: 94	**LCMXO640**: 117, 135 **LCMXO1200/2280**: 135	**LCMXO256**: H14, A14, B5 **LCMXO640**: B12, B5
VCCIO1	**LCMXO256**: 10, 24, 41 **LCMXO640**: 60, 74 **LCMXO1200/2280**: 80	**LCMXO640**: 82, 98 **LCMXO1200/2280**: 117	**LCMXO256**: G1, P1, P10 **LCMXO640**: H14, A14
VCCIO2	**LCMXO256**: None **LCMXO640**: 29, 41 **LCMXO1200/2280**: 70	**LCMXO640**: 38, 63 **LCMXO1200/2280**: 98	**LCMXO256**: None **LCMXO640**: P4, P10
VCCIO3	**LCMXO256**: None **LCMXO640**: 10, 24 **LCMXO1200/2280**: 56	**LCMXO640**: 10, 26 **LCMXO1200/2280**: 82	**LCMXO256**: None **LCMXO640**: G1, P1
VCCIO4	**LCMXO256/640**: None **LCMXO1200/2280**: 44	**LCMXO640**: None **LCMXO1200/2280**: 63	—
VCCIO5	**LCMXO256/640**: None **LCMXO1200/2280**: 27	**LCMXO640**: None **LCMXO1200/2280**: 38	—
VCCIO6	**LCMXO256/640**: None **LCMXO1200/2280**: 20	**LCMXO640**: None **LCMXO1200/2280**: 26	—
VCCIO7	**LCMXO256/640**: None **LCMXO1200/2280**: 6	**LCMXO640**: None **LCMXO1200/2280**: 10	—
VCCAUX	**LCMXO256/640**: 88 **LCMXO1200/2280**: 36, 90	53, 128	B7
GND[3]	**LCMXO256**: 40, 84, 62, 75, 93, 12, 25, 42 **LCMXO640**: 40, 84, 81, 93, 62, 75, 30, 42, 12, 25 **LCMXO1200/2280**: 9, 41, 59, 83, 100, 76, 50, 26	16, 59, 88, 123, 118, 136, 83, 99, 37, 64, 11, 27	**LCMXO256**: N9, B9, G14, B13, A4, H1, N2, N10 **LCMXO640**: N9, B9, A10, A4, G14, B13, N3, N10, H1, N2
NC[4]			—

Notes:

1. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
2. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
3. All grounds must be electrically connected at the board level. For fpBGA and ftBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
4. NC pins should not be connected to any active signals, VCC or GND.

4.4. Power Supply and NC (Cont.)

Signal	132 csBGA[1]	256 caBGA / 256 ftBGA[1]	324 ftBGA[1]
VCC	H3, P6, G12, C7	G7, G10, K7, K10	F14, G11, G9, H7, L7, M9
VCCIO0	**LCMXO640**: B11, C5 **LCMXO1200/2280**: C5	**LCMXO640**: F8, F7, F9, F10 **LCMXO1200/2280**: F8, F7	G8, G7
VCCIO1	**LCMXO640**: L12, E12 **LCMXO1200/2280**: B11	**LCMXO640**: H11, G11, K11, J11 **LCMXO1200/2280**: F9, F10	G12, G10
VCCIO2	**LCMXO640**: N2, M10 **LCMXO1200/2280**: E12	**LCMXO640**: L9, L10, L8, L7 **LCMXO1200/2280**: H11, G11	J12, H12
VCCIO3	**LCMXO640**: D2, K3	**LCMXO640**: K6, J6, H6, G6	L12, K12

Signal	132 csBGA[1]	256 caBGA / 256 ftBGA[1]	324 ftBGA[1]
	LCMXO1200/2280: L12	**LCMXO1200/2280**: K11, J11	
VCCIO4	**LCMXO640**: None **LCMXO1200/2280**: M10	**LCMXO640**: None **LCMXO1200/2280**: L9, L10	M12, M11
VCCIO5	**LCMXO640**: None **LCMXO1200/2280**: N2	**LCMXO640**: None **LCMXO1200/2280**: L8, L7	M8, R9
VCCIO6	**LCMXO640**: None **LCMXO1200/2280**: K3	**LCMXO640**: None **LCMXO1200/2280**: K6, J6	M7, K7
VCCIO7	**LCMXO640**: None **LCMXO1200/2280**: D2	**LCMXO640**: None **LCMXO1200/2280**: H6, G6	H6, J7
VCCAUX	P7, A7	T9, A8	M10, F9
GND[2]	F1, P9, J14, C9, A10, B4, L13, D13, P2, N11, E1, L2	A1, A16, F11, G8, G9, H7, H8, H9, H10, J7, J8, J9, J10, K8, K9, L6, T1, T16	E14, F16, H10, H11, H8, H9, J10, J11, J4, J8, J9, K10, K11, K17, K8, K9, L10, L11, L8, L9, N2, P14, P5, R7
NC[3]	—	**LCMXO640**: E4, E5, F5, F6, C3, C2, G4, G5, H4, H5, K5, K4, M5, M4, P2, P3, N5, N6, M7, M8, N10, N11, R15, R16, P15, P16, M11, L11, N12, N13, M13, M12, K12, J12, F12, F13, E12, E13, D13, D14, B15, A15, C14, B14, E11, E10, E7, E6, D4, D3, B3, B2 **LCMXO1200**: None **LCMXO2280**: None	—

Notes:

1. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
2. All grounds must be electrically connected at the board level. For fpBGA and ftBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
3. NC pins should not be connected to any active signals, VCC or GND.

4.5. LCMXO256 and LCMXO640 Logic Signal Connections: 100 TQFP

Pin Number	LCMXO256				LCMXO640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	1		T	PL2A	3		T
2	PL2B	1		C	PL2C	3		T
3	PL3A	1		T	PL2B	3		C
4	PL3B	1		C	PL2D	3		C
5	PL3C	1		T	PL3A	3		T
6	PL3D	1		C	PL3B	3		C
7	PL4A	1		T	PL3C	3		T
8	PL4B	1		C	PL3D	3		C
9	PL5A	1		T	PL4A	3		
10	VCCIO1	1			VCCIO3	3		
11	PL5B	1		C	PL4C	3		T
12	GNDIO1	1			GNDIO3	3		
13	PL5C	1		T	PL4D	3		C
14	PL5D	1	GSRN	C	PL5B	3	GSRN	
15	PL6A	1		T	PL7B	3		
16	PL6B	1	TSALL	C	PL8C	3	TSALL	T

Pin Number	LCMXO256				LCMXO640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
17	PL7A	1		T	PL8D	3		C
18	PL7B	1		C	PL9A	3		
19	PL7C	1		T	PL9C	3		
20	PL7D	1		C	PL10A	3		
21	PL8A	1		T	PL10C	3		
22	PL8B	1		C	PL11A	3		
23	PL9A	1		T	PL11C	3		
24	VCCIO1	1			VCCIO3	3		
25	GNDIO1	1			GNDIO3	3		
26	TMS	1	TMS		TMS	2	TMS	
27	PL9B	1		C	PB2C	2		
28	TCK	1	TCK		TCK	2	TCK	
29	PB2A	1		T	VCCIO2	2		
30	PB2B	1		C	GNDIO2	2		
31	TDO	1	TDO		TDO	2	TDO	
32	PB2C	1		T	PB4C	2		
33	TDI	1	TDI		TDI	2	TDI	
34	PB2D	1		C	PB4E	2		
35	VCC	—			VCC	—		
36	PB3A	1	PCLK1_1[2]	T	PB5B	2	PCLK2_1[2]	
37	PB3B	1		C	PB5D	2		
38	PB3C	1	PCLK1_0[2]	T	PB6B	2	PCLK2_0[2]	
39	PB3D	1		C	PB6C	2		
40	GND	—			GND	—		
41	VCCIO1	1			VCCIO2	2		
42	GNDIO1	1			GNDIO2	2		
43	PB4A	1		T	PB8B	2		
44	PB4B	1		C	PB8C	2		T
45	PB4C	1		T	PB8D	2		C
46	PB4D	1		C	PB9A	2		
47	PB5A	1			PB9C	2		T
48[1]	SLEEPN	—	SLEEPN		SLEEPN	—	SLEEPN	
49	PB5C	1		T	PB9D	2		C
50	PB5D	1		C	PB9F	2		
51	PR9B	0		C	PR11D	1		C
52	PR9A	0		T	PR11B	1		C
53	PR8B	0		C	PR11C	1		T
54	PR8A	0		T	PR11A	1		T
55	PR7D	0		C	PR10D	1		C
56	PR7C	0		T	PR10C	1		T
57	PR7B	0		C	PR10B	1		C
58	PR7A	0		T	PR10A	1		T
59	PR6B	0		C	PR9D	1		
60	VCCIO0	0			VCCIO1	1		
61	PR6A	0		T	PR9B	1		
62	GNDIO0	0			GNDIO1	1		

Pin Number	LCMXO256				LCMXO640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
63	PR5D	0		C	PR7B	1		
64	PR5C	0		T	PR6C	1		
65	PR5B	0		C	PR6B	1		
66	PR5A	0		T	PR5D	1		
67	PR4B	0		C	PR5B	1		
68	PR4A	0		T	PR4D	1		
69	PR3D	0		C	PR4B	1		
70	PR3C	0		T	PR3D	1		
71	PR3B	0		C	PR3B	1		
72	PR3A	0		T	PR2D	1		
73	PR2B	0		C	PR2B	1		
74	VCCIO0	0			VCCIO1	1		
75	GNDIO0	0			GNDIO1	1		
76	PR2A	0		T	PT9F	0		C
77	PT5C	0			PT9E	0		T
78	PT5B	0		C	PT9C	0		
79	PT5A	0		T	PT9A	0		
80	PT4F	0		C	VCCIO0	0		
81	PT4E	0		T	GNDIO0	0		
82	PT4D	0		C	PT7E	0		
83	PT4C	0		T	PT7A	0		
84	GND	—			GND	—		
85	PT4B	0	PCLK0_1[2]	C	PT6B	0	PCLK0_1[2]	
86	PT4A	0	PCLK0_0[2]	T	PT5B	0	PCLK0_0[2]	C
87	PT3D	0		C	PT5A	0		T
88	VCCAUX	—			VCCAUX	—		
89	PT3C	0		T	PT4F	0		
90	VCC	—			VCC	—		
91	PT3B	0		C	PT3F	0		
92	VCCIO0	0			VCCIO0	0		
93	GNDIO0	0			GNDIO0	0		
94	PT3A	0		T	PT3B	0		C
95	PT2F	0		C	PT3A	0		T
96	PT2E	0		T	PT2F	0		C
97	PT2D	0		C	PT2E	0		T
98	PT2C	0		T	PT2B	0		C
99	PT2B	0		C	PT2C	0		
100	PT2A	0		T	PT2A	0		T

Notes:

1. NC for “E” devices.
2. Primary clock inputs are single-ended.

4.6. LCMXO1200 and LCMXO2280 Logic Signal Connections: 100 TQFP

Pin Number	LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	7		T	PL2A	7	LUM0_PLLT_FB_A	T
2	PL2B	7		C	PL2B	7	LUM0_PLLC_FB_A	C
3	PL3C	7		T	PL3C	7	LUM0_PLLT_IN_A	T
4	PL3D	7		C	PL3D	7	LUM0_PLLC_IN_A	C
5	PL4B	7			PL4B	7		
6	VCCIO7	7			VCCIO7	7		
7	PL6A	7		T[1]	PL7A	7		T[1]
8	PL6B	7	GSRN	C[1]	PL7B	7	GSRN	C[1]
9	GND	—			GND	—		
10	PL7C	7		T	PL9C	7		T
11	PL7D	7		C	PL9D	7		C
12	PL8C	7		T	PL10C	7		T
13	PL8D	7		C	PL10D	7		C
14	PL9C	6			PL11C	6		
15	PL10A	6		T[1]	PL13A	6		T[1]
16	PL10B	6		C[1]	PL13B	6		C[1]
17	VCC	—			VCC	—		
18	PL11B	6			PL14D	6		C
19	PL11C	6	TSALL		PL14C	6	TSALL	T
20	VCCIO6	6			VCCIO6	6		
21	PL13C	6			PL16C	6		
22	PL14A	6	LLM0_PLLT_FB_A	T[1]	PL17A	6	LLM0_PLLT_FB_A	T[1]
23	PL14B	6	LLM0_PLLC_FB_A	C[1]	PL17B	6	LLM0_PLLC_FB_A	C[1]
24	PL15A	6	LLM0_PLLT_IN_A	T[1]	PL18A	6	LLM0_PLLT_IN_A	T[1]
25	PL15B	6	LLM0_PLLC_IN_A	C[1]	PL18B	6	LLM0_PLLC_IN_A	C[1]
26[2]	GNDIO6 GNDIO5	—			GNDIO6 GNDIO5	—		
27	VCCIO5	5			VCCIO5	5		
28	TMS	5	TMS		TMS	5	TMS	
29	TCK	5	TCK		TCK	5	TCK	
30	PB3B	5			PB3B	5		
31	PB4A	5		T	PB4A	5		T
32	PB4B	5		C	PB4B	5		C
33	TDO	5	TDO		TDO	5	TDO	
34	TDI	5	TDI		TDI	5	TDI	
35	VCC	—			VCC	—		
36	VCCAUX	—			VCCAUX	—		
37	PB6E	5		T	PB8E	5		T
38	PB6F	5		C	PB8F	5		C
39	PB7B	4	PCLK4_1[4]		PB10F	4	PCLK4_1[4]	
40	PB7F	4	PCLK4_0[4]		PB10B	4	PCLK4_0[4]	
41	GND	—			GND	—		
42	PB9A	4		T	PB12A	4		T
43	PB9B	4		C	PB12B	4		C
44	VCCIO4	4			VCCIO4	4		

Pin Number	LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
45	PB10A	4		T	PB13A	4		T
46	PB10B	4		C	PB13B	4		C
47[3]	SLEEPN	—	SLEEPN		SLEEPN	—	SLEEPN	
48	PB11A	4		T	PB16A	4		T
49	PB11B	4		C	PB16B	4		C
50[2]	GNDIO3 GNDIO4	—			GNDIO3 GNDIO4	—		
51	PR16B	3			PR19B	3		
52	PR15B	3		C[1]	PR18B	3		C[1]
53	PR15A	3		T[1]	PR18A	3		T[1]
54	PR14B	3		C[1]	PR17B	3		C[1]
55	PR14A	3		T[1]	PR17A	3		T[1]
56	VCCIO3	3			VCCIO3	3		
57	PR12B	3		C[1]	PR15B	3		C[1]
58	PR12A	3		T[1]	PR15A	3		T[1]
59	GND	—			GND	—		
60	PR10B	3		C[1]	PR13B	3		C[1]
61	PR10A	3		T[1]	PR13A	3		T[1]
62	PR9B	3		C[1]	PR11B	3		C[1]
63	PR9A	3		T[1]	PR11A	3		T[1]
64	PR8B	2		C[1]	PR10B	2		C[1]
65	PR8A	2		T[1]	PR10A	2		T[1]
66	VCC	—			VCC	—		
67	PR6C	2			PR8C	2		
68	PR6B	2		C[1]	PR8B	2		C[1]
69	PR6A	2		T[1]	PR8A	2		T[1]
70	VCCIO2	2			VCCIO2	2		
71	PR4D	2			PR5D	2		
72	PR4B	2		C[1]	PR5B	2		C[1]
73	PR4A	2		T[1]	PR5A	2		T[1]
74	PR2B	2		C	PR3B	2		C[1]
75	PR2A	2		T	PR3A	2		T[1]
76[2]	GNDIO1 GNDIO2	—			GNDIO1 GNDIO2	—		
77	PT11C	1			PT15C	1		
78	PT11B	1		C	PT14B	1		C
79	PT11A	1		T	PT14A	1		T
80	VCCIO1	1			VCCIO1	1		
81	PT9E	1			PT12D	1		C
82	PT9A	1			PT12C	1		T
83	GND	—			GND	—		
84	PT8B	1		C	PT11B	1		C
85	PT8A	1		T	PT11A	1		T
86	PT7D	1	PCLK1_1[4]		PT10B	1	PCLK1_1[4]	
87	PT6F	0	PCLK0_0[4]		PT9B	1	PCLK1_0[4]	
88	PT6D	0		C	PT8F	0		C

Pin Number	LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
89	PT6C	0		T	PT8E	0		T
90	VCCAUX	—			VCCAUX	—		
91	VCC	—			VCC	—		
92	PT5B	0			PT6D	0		
93	PT4B	0			PT6F	0		
94	VCCIO0	0			VCCIO0	0		
95	PT3D	0		C	PT4B	0		C
96	PT3C	0		T	PT4A	0		T
97	PT3B	0			PT3B	0		
98	PT2B	0		C	PT2B	0		C
99	PT2A	0		T	PT2A	0		T
100[2]	GNDIO0 GNDIO7	—			GNDIO0 GNDIO7	—		

Notes:

1. Supports true LVDS outputs.
2. Double bonded to the pin.
3. NC for "E" devices.
4. Primary clock inputs are single-ended.

4.7. LCMXO256 and LCMXO640 Logic Signal Connections: 100 csBGA

LCMXO256					LCMXO640				
Ball Number	Ball Function	Bank	Dual Function	Differen-tial	Ball Number	Ball Function	Bank	Dual Function	Differential
B1	PL2A	1		T	B1	PL2A	3		T
C1	PL2B	1		C	C1	PL2C	3		T
D2	PL3A	1		T	D2	PL2B	3		C
D1	PL3B	1		C	D1	PL2D	3		C
C2	PL3C	1		T	C2	PL3A	3		T
E1	PL3D	1		C	E1	PL3B	3		C
E2	PL4A	1		T	E2	PL3C	3		T
F1	PL4B	1		C	F1	PL3D	3		C
F2	PL5A	1		T	F2	PL4A	3		
G2	PL5B	1		C	G2	PL4C	3		T
H1	GNDIO1	1			H1	GNDIO3	3		
H2	PL5C	1		T	H2	PL4D	3		C
J1	PL5D	1	GSRN	C	J1	PL5B	3	GSRN	
J2	PL6A	1		T	J2	PL7B	3		
K1	PL6B	1	TSALL	C	K1	PL8C	3	TSALL	T
K2	PL7A	1		T	K2	PL8D	3		C
L1	PL7B	1		C	L1	PL9A	3		
L2	PL7C	1		T	L2	PL9C	3		
M1	PL7D	1		C	M1	PL10A	3		
M2	PL8A	1		T	M2	PL10C	3		
N1	PL8B	1		C	N1	PL11A	3		
M3	PL9A	1		T	M3	PL11C	3		
N2	GNDIO1	1			N2	GNDIO3	3		

LCMXO256					LCMXO640				
Ball Number	Ball Function	Bank	Dual Function	Differen-tial	Ball Number	Ball Function	Bank	Dual Function	Differential
P2	TMS	1	TMS		P2	TMS	2	TMS	
P3	PL9B	1		C	P3	PB2C	2		
N4	TCK	1	TCK		N4	TCK	2	TCK	
P4	PB2A	1		T	P4	VCCIO2	2		
N3	PB2B	1		C	N3	GNDIO2	2		
P5	TDO	1	TDO		P5	TDO	2	TDO	
N5	PB2C	1		T	N5	PB4C	2		
P6	TDI	1	TDI		P6	TDI	2	TDI	
N6	PB2D	1		C	N6	PB4E	2		
P7	VCC	—			P7	VCC	—		
N7	PB3A	1	PCLK1_1[2]	T	N7	PB5B	2	PCLK2_1[2]	
P8	PB3B	1		C	P8	PB5D	2		
N8	PB3C	1	PCLK1_0[2]	T	N8	PB6B	2	PCLK2_0[2]	
P9	PB3D	1		C	P9	PB6C	2		
N10	GNDIO1	1			N10	GNDIO2	2		
P11	PB4A	1		T	P11	PB8B	2		
N11	PB4B	1		C	N11	PB8C	2		T
P12	PB4C	1		T	P12	PB8D	2		C
N12	PB4D	1		C	N12	PB9A	2		
P13	PB5A	1			P13	PB9C	2		T
M12[1]	SLEEPN	—	SLEEPN		M12[1]	SLEEPN	—	SLEEPN	
P14	PB5C	1		T	P14	PB9D	2		C
N13	PB5D	1		C	N13	PB9F	2		
N14	PR9B	0		C	N14	PR11D	1		C
M14	PR9A	0		T	M14	PR11B	1		C
L13	PR8B	0		C	L13	PR11C	1		T
L14	PR8A	0		T	L14	PR11A	1		T
M13	PR7D	0		C	M13	PR10D	1		C
K14	PR7C	0		T	K14	PR10C	1		T
K13	PR7B	0		C	K13	PR10B	1		C
J14	PR7A	0		T	J14	PR10A	1		T
J13	PR6B	0		C	J13	PR9D	1		
H13	PR6A	0		T	H13	PR9B	1		
G14	GNDIO0	0			G14	GNDIO1	1		
G13	PR5D	0		C	G13	PR7B	1		
F14	PR5C	0		T	F14	PR6C	1		
F13	PR5B	0		C	F13	PR6B	1		
E14	PR5A	0		T	E14	PR5D	1		
E13	PR4B	0		C	E13	PR5B	1		
D14	PR4A	0		T	D14	PR4D	1		
D13	PR3D	0		C	D13	PR4B	1		
C14	PR3C	0		T	C14	PR3D	1		
C13	PR3B	0		C	C13	PR3B	1		
B14	PR3A	0		T	B14	PR2D	1		
C12	PR2B	0		C	C12	PR2B	1		
B13	GNDIO0	0			B13	GNDIO1	1		

LCMXO256					LCMXO640				
Ball Number	Ball Function	Bank	Dual Function	Differen-tial	Ball Number	Ball Function	Bank	Dual Function	Differential
A13	PR2A	0		T	A13	PT9F	0		C
A12	PT5C	0			A12	PT9E	0		T
B11	PT5B	0		C	B11	PT9C	0		
A11	PT5A	0		T	A11	PT9A	0		
B12	PT4F	0		C	B12	VCCIO0	0		
A10	PT4E	0		T	A10	GNDIO0	0		
B10	PT4D	0		C	B10	PT7E	0		
A9	PT4C	0		T	A9	PT7A	0		
A8	PT4B	0	PCLK0_1[2]	C	A8	PT6B	0	PCLK0_1[2]	
B8	PT4A	0	PCLK0_0[2]	T	B8	PT5B	0	PCLK0_0[2]	C
A7	PT3D	0		C	A7	PT5A	0		T
B7	VCCAUX	—			B7	VCCAUX	—		
A6	PT3C	0		T	A6	PT4F	0		
B6	VCC	—			B6	VCC	—		
A5	PT3B	0		C	A5	PT3F	0		
A4	GNDIO0	0			A4	GNDIO0	0		
B4	PT3A	0		T	B4	PT3B	0		C
A3	PT2F	0		C	A3	PT3A	0		T
B3	PT2E	0		T	B3	PT2F	0		C
A2	PT2D	0		C	A2	PT2E	0		T
C3	PT2C	0		T	C3	PT2B	0		C
A1	PT2B	0		C	A1	PT2C	0		
B2	PT2A	0		T	B2	PT2A	0		T
N9	GND	—			N9	GND	—		
B9	GND	—			B9	GND	—		
B5	VCCIO0	0			B5	VCCIO0	0		
A14	VCCIO0	0			A14	VCCIO1	1		
H14	VCCIO0	0			H14	VCCIO1	1		
P10	VCCIO1	1			P10	VCCIO2	2		
G1	VCCIO1	1			G1	VCCIO3	3		
P1	VCCIO1	1			P1	VCCIO3	3		

Notes:

1. NC for “E” devices.
2. Primary clock inputs are single-ended.

4.8. LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 132 csBGA

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
B1	PL2A	3		T	B1	PL2A	7		T	B1	PL2A	7	LUM0_PLLT_FB_A	T
C1	PL2B	3		C	C1	PL3C	7		T	C1	PL3C	7	LUM0_PLLT_IN_A	T
B2	PL2C	3		T	B2	PL2B	7		C	B2	PL2B	7	LUM0_PLLC_FB_A	C
C2	PL2D	3		C	C2	PL4A	7		T[1]	C2	PL4A	7		T[1]
C3	PL3A	3		T	C3	PL3D	7		C	C3	PL3D	7	LUM0_PLLC_IN_A	C
D1	PL3B	3		C	D1	PL4B	7		C[1]	D1	PL4B	7		C[1]
D3	PL3D	3			D3	PL4C	7			D3	PL4C	7		
E1	GNDIO3	3			E1	GNDIO7	7			E1	GNDIO7	7		
E2	PL5A	3		T	E2	PL6A	7		T[1]	E2	PL7A	7		T[1]
E3	PL5B	3	GSRN	C	E3	PL6B	7	GSRN	C[1]	E3	PL7B	7	GSRN	C[1]
F2	PL5D	3			F2	PL6D	7			F2	PL7D	7		
F3	PL6B	3			F3	PL7C	7		T	F3	PL9C	7		T
G1	PL6C	3		T	G1	PL7D	7		C	G1	PL9D	7		C
G2	PL6D	3		C	G2	PL8C	7		T	G2	PL10C	7		T
G3	PL7A	3		T	G3	PL8D	7		C	G3	PL10D	7		C
H2	PL7B	3		C	H2	PL10A	6		T[1]	H2	PL12A	6		T[1]
H1	PL7C	3			H1	PL10B	6		C[1]	H1	PL12B	6		C[1]
H3	VCC	—			H3	VCC	—			H3	VCC	—		
J1	PL8A	3			J1	PL11B	6			J1	PL14D	6		C
J2	PL8C	3	TSALL		J2	PL11C	6	TSALL	T	J2	PL14C	6	TSALL	T
J3	PL9A	3		T	J3	PL11D	6		C	J3	PL14B	6		
K2	PL9B	3		C	K2	PL12A	6		T[1]	K2	PL15A	6		T[1]
K1	PL9C	3			K1	PL12B	6		C[1]	K1	PL15B	6		C[1]
L2	GNDIO3	3			L2	GNDIO6	6			L2	GNDIO6	6		
L1	PL10A	3		T	L1	PL14A	6	LLM0_PLLT_FB_A	T[1]	L1	PL17A	6	LLM0_PLLT_FB_A	T[1]
L3	PL10B	3		C	L3	PL14B	6	LLM0_PLLC_FB_A	C[1]	L3	PL17B	6	LLM0_PLLC_FB_A	C[1]
M1	PL11A	3		T	M1	PL15A	6	LLM0_PLLT_IN_A	T[1]	M1	PL18A	6	LLM0_PLLT_IN_A	T[1]
N1	PL11B	3		C	N1	PL16A	6		T	N1	PL19A	6		T
M2	PL11C	3		T	M2	PL15B	6	LLM0_PLLC_IN_A	C[1]	M2	PL18B	6	LLM0_PLLC_IN_A	C[1]
P1	PL11D	3		C	P1	PL16B	6		C	P1	PL19B	6		C
P2	GNDIO2	2			P2	GNDIO5	5			P2	GNDIO5	5		
P3	TMS	2	TMS		P3	TMS	5	TMS		P3	TMS	5	TMS	
M3	PB2C	2		T	M3	PB2C	5		T	M3	PB2A	5		T
N3	PB2D	2		C	N3	PB2D	5		C	N3	PB2B	5		C
P4	TCK	2	TCK		P4	TCK	5	TCK		P4	TCK	5	TCK	
M4	PB3B	2			M4	PB3B	5			M4	PB3B	5		
N4	PB3C	2		T	N4	PB4A	5		T	N4	PB4A	5		T
P5	PB3D	2		C	P5	PB4B	5		C	P5	PB4B	5		C
N5	TDO	2	TDO		N5	TDO	5	TDO		N5	TDO	5	TDO	
M5	TDI	2	TDI		M5	TDI	5	TDI		M5	TDI	5	TDI	
N6	PB4E	2		T	N6	PB5C	5			N6	PB6C	5		
P6	VCC	—			P6	VCC	—			P6	VCC	—		
M6	PB4F	2		C	M6	PB6A	5			M6	PB8A	5		
P7	VCCAUX	—			P7	VCCAUX	—			P7	VCCAUX	—		
N7	PB5A	2		T	N7	PB6F	5			N7	PB8F	5		
M7	PB5B	2	PCLK2_1[3]	C	M7	PB7B	4	PCLK4_1[3]		M7	PB10F	4	PCLK4_1[3]	
N8	PB5D	2			N8	PB7C	4		T	N8	PB10C	4		T
P8	PB6A	2		T	P8	PB7D	4		C	P8	PB10D	4		C
M8	PB6B	2	PCLK2_0[3]	C	M8	PB7F	4	PCLK4_0[3]		M8	PB10B	4	PCLK4_0[3]	
N9	PB7A	2		T	N9	PB9A	4		T	N9	PB12A	4		T
M9	PB7B	2		C	M9	PB9B	4		C	M9	PB12B	4		C
N10	PB7E	2		T	N10	PB9C	4		T	N10	PB12C	4		T
P10	PB7F	2		C	P10	PB9D	4		C	P10	PB12D	4		C
N11	GNDIO2	2			N11	GNDIO4	4			N11	GNDIO4	4		

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
P11	PB8C	2		T	P11	PB10A	4		T	P11	PB13C	4		T
M11	PB8D	2		C	M11	PB10B	4		C	M11	PB13D	4		C
P12	PB9C	2		T	P12	PB10C	4			P12	PB15B	4		
P13	PB9D	2		C	P13	PB11C	4		T	P13	PB16C	4		T
N12[2]	SLEEPN	—	SLEEPN		N12[2]	SLEEPN	—	SLEEPN		N12[2]	SLEEPN	—	SLEEPN	
P14	PB9F	2			P14	PB11D	4		C	P14	PB16D	4		C
N14	PR11D	1		C	N14	PR16B	3		C	N14	PR19B	3		C
M14	PR11C	1		T	M14	PR15B	3		C[1]	M14	PR18B	3		C[1]
N13	PR11B	1		C	N13	PR16A	3		T	N13	PR19A	3		T
M12	PR11A	1		T	M12	PR15A	3		T[1]	M12	PR18A	3		T[1]
M13	PR10B	1		C	M13	PR14B	3		C[1]	M13	PR17B	3		C[1]
L14	PR10A	1		T	L14	PR14A	3		T[1]	L14	PR17A	3		T[1]
L13	GNDIO1	1			L13	GNDIO3	3			L13	GNDIO3	3		
K14	PR8D	1		C	K14	PR12B	3		C[1]	K14	PR15B	3		C[1]
K13	PR8C	1		T	K13	PR12A	3		T[1]	K13	PR15A	3		T[1]
K12	PR8B	1		C	K12	PR11B	3		C[1]	K12	PR14B	3		C[1]
J13	PR8A	1		T	J13	PR11A	3		T[1]	J13	PR14A	3		T[1]
J12	PR7C	1			J12	PR10B	3		C[1]	J12	PR13B	3		C[1]
H14	PR7B	1		C	H14	PR10A	3		T[1]	H14	PR13A	3		T[1]
H13	PR7A	1		T	H13	PR9B	3		C[1]	H13	PR11B	3		C[1]
H12	PR6D	1		C	H12	PR9A	3		T[1]	H12	PR11A	3		T[1]
G13	PR6C	1		T	G13	PR8B	2		C[1]	G13	PR10B	2		C[1]
G14	PR6B	1			G14	PR8A	2		T[1]	G14	PR10A	2		T[1]
G12	VCC	—			G12	VCC	—			G12	VCC	—		
F14	PR5D	1		C	F14	PR6C	2			F14	PR8C	2		
F13	PR5C	1		T	F13	PR6B	2		C[1]	F13	PR8B	2		C[1]
F12	PR4D	1		C	F12	PR6A	2		T[1]	F12	PR8A	2		T[1]
E13	PR4C	1		T	E13	PR5B	2		C[1]	E13	PR7B	2		C[1]
E14	PR4B	1			E14	PR5A	2		T[1]	E14	PR7A	2		T[1]
D13	GNDIO1	1			D13	GNDIO2	2			D13	GNDIO2	2		
D14	PR3D	1		C	D14	PR4B	2		C[1]	D14	PR5B	2		C[1]
D12	PR3C	1		T	D12	PR4A	2		T[1]	D12	PR5A	2		T[1]
C14	PR2D	1		C	C14	PR3D	2		C	C14	PR4D	2		C
B14	PR2C	1		T	B14	PR2B	2		C	B14	PR3B	2		C[1]
C13	PR2B	1		C	C13	PR3C	2		T	C13	PR4C	2		T
A14	PR2A	1		T	A14	PR2A	2		T	A14	PR3A	2		T[1]
A13	PT9F	0		C	A13	PT11D	1		C	A13	PT16D	1		C
A12	PT9E	0		T	A12	PT11B	1		C	A12	PT16B	1		C
B13	PT9D	0		C	B13	PT11C	1		T	B13	PT16C	1		T
B12	PT9C	0		T	B12	PT10F	1			B12	PT15D	1		
C12	PT9B	0		C	C12	PT11A	1		T	C12	PT16A	1		T
A11	PT9A	0		T	A11	PT10D	1		C	A11	PT14B	1		C
C11	PT8C	0			C11	PT10C	1		T	C11	PT14A	1		T
A10	GNDIO0	0			A10	GNDIO1	1			A10	GNDIO1	1		
B10	PT7F	0		C	B10	PT9F	1		C	B10	PT12F	1		C
C10	PT7E	0		T	C10	PT9E	1		T	C10	PT12E	1		T
B9	PT7B	0		C	B9	PT9B	1		C	B9	PT12D	1		C
A9	PT7A	0		T	A9	PT9A	1		T	A9	PT12C	1		T
A8	PT6B	0	PCLK0_1[3]	C	A8	PT7D	1	PCLK1_1[3]		A8	PT10B	1	PCLK1_1[3]	
B8	PT6A	0		T	B8	PT7B	1			B8	PT9D	1		
C8	PT5B	0	PCLK0_0[3]	C	C8	PT6F	0	PCLK1_0[3]		C8	PT9B	1	PCLK1_0[3]	
B7	PT5A	0		T	B7	PT6D	0			B7	PT8D	0		
A7	VCCAUX	—			A7	VCCAUX	—			A7	VCCAUX	—		
C7	VCC	—			C7	VCC	—			C7	VCC	—		

LCMXO640					LCMXO1200					LCMXO2280				
Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential	Ball #	Ball Function	Bank	Dual Function	Differential
A6	PT4D	0		C	A6	PT5D	0		C	A6	PT7B	0		C
B6	PT4C	0		T	B6	PT5C	0		T	B6	PT7A	0		T
C6	PT3F	0		C	C6	PT5B	0		C	C6	PT6D	0		
B5	PT3E	0		T	B5	PT5A	0		T	B5	PT6E	0		T
A5	PT3D	0			A5	PT4B	0			A5	PT6F	0		C
B4	GNDIO0	0			B4	GNDIO0	0			B4	GNDIO0	0		
A4	PT3B	0			A4	PT3D	0		C	A4	PT4B	0		C
C4	PT2F	0			C4	PT3C	0		T	C4	PT4A	0		T
A3	PT2D	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2C	0		T	A2	PT2B	0		C	A2	PT2B	0		C
B3	PT2B	0		C	B3	PT3A	0		T	B3	PT3A	0		T
A1	PT2A	0		T	A1	PT2A	0		T	A1	PT2A	0		T
F1	GND	—			F1	GND	—			F1	GND	—		
P9	GND	—			P9	GND	—			P9	GND	—		
J14	GND	—			J14	GND	—			J14	GND	—		
C9	GND	—			C9	GND	—			C9	GND	—		
C5	VCCIO0	0			C5	VCCIO0	0			C5	VCCIO0	0		
B11	VCCIO0	0			B11	VCCIO1	1			B11	VCCIO1	1		
E12	VCCIO1	1			E12	VCCIO2	2			E12	VCCIO2	2		
L12	VCCIO1	1			L12	VCCIO3	3			L12	VCCIO3	3		
M10	VCCIO2	2			M10	VCCIO4	4			M10	VCCIO4	4		
N2	VCCIO2	2			N2	VCCIO5	5			N2	VCCIO5	5		
D2	VCCIO3	3			D2	VCCIO7	7			D2	VCCIO7	7		
K3	VCCIO3	3			K3	VCCIO6	6			K3	VCCIO6	6		

Notes:

1. Supports true LVDS outputs.
2. NC for "E" devices.
3. Primary clock inputs are single-ended.

4.9. LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 144 TQFP

Pin Number	LCMXO640				LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	3		T	PL2A	7		T	PL2A	7	LUM0_PLLT_FB_A	T
2	PL2C	3		T	PL2B	7		C	PL2B	7	LUM0_PLLC_FB_A	C
3	PL2B	3		C	PL3A	7		T[1]	PL3A	7		T[1]
4	PL3A	3		T	PL3B	7		C[1]	PL3B	7		C[1]
5	PL2D	3		C	PL3C	7		T	PL3C	7	LUM0_PLLT_IN_A	T
6	PL3B	3		C	PL3D	7		C	PL3D	7	LUM0_PLLC_IN_A	C
7	PL3C	3		T	PL4A	7		T[1]	PL4A	7		T[1]
8	PL3D	3		C	PL4B	7		C[1]	PL4B	7		C[1]
9	PL4A	3			PL4C	7			PL4C	7		
10	VCCIO3	3			VCCIO7	7			VCCIO7	7		
11	GNDIO3	3			GNDIO7	7			GNDIO7	7		
12	PL4D	3			PL5C	7			PL6C	7		
13	PL5A	3		T	PL6A	7		T[1]	PL7A	7		T[1]
14	PL5B	3	GSRN	C	PL6B	7	GSRN	C[1]	PL7B	7	GSRN	C[1]
15	PL5D	3			PL6D	7			PL7D	7		
16	GND	—			GND	—			GND	—		
17	PL6C	3		T	PL7C	7		T	PL9C	7		T
18	PL6D	3		C	PL7D	7		C	PL9D	7		C
19	PL7A	3		T	PL10A	6		T[1]	PL13A	6		T[1]
20	PL7B	3		C	PL10B	6		C[1]	PL13B	6		C[1]
21	VCC	—			VCC	—			VCC	—		
22	PL8A	3		T	PL11A	6		T[1]	PL13D	6		
23	PL8B	3		C	PL11B	6		C[1]	PL14D	6		C
24	PL8C	3	TSALL		PL11C	6	TSALL		PL14C	6	TSALL	T

Pin Number	LCMXO640				LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
25	PL9C	3		T	PL12B	6			PL15B	6		
26	VCCIO3	3			VCCIO6	6			VCCIO6	6		
27	GNDIO3	3			GNDIO6	6			GNDIO6	6		
28	PL9D	3		C	PL13D	6			PL16D	6		
29	PL10A	3		T	PL14A	6	LLM0_PLLT_FB_A	T[1]	PL17A	6	LLM0_PLLT_FB_A	T[1]
30	PL10B	3		C	PL14B	6	LLM0_PLLC_FB_A	C[1]	PL17B	6	LLM0_PLLC_FB_A	C[1]
31	PL10C	3		T	PL14C	6		T	PL17C	6		T
32	PL11A	3		T	PL14D	6		C	PL17D	6		C
33	PL10D	3		C	PL15A	6	LLM0_PLLT_IN_A	T[1]	PL18A	6	LLM0_PLLT_IN_A	T[1]
34	PL11C	3		T	PL15B	6	LLM0_PLLC_IN_A	C[1]	PL18B	6	LLM0_PLLC_IN_A	C[1]
35	PL11B	3		C	PL16A	6		T	PL19A	6		T
36	PL11D	3		C	PL16B	6		C	PL19B	6		C
37	GNDIO2	2			GNDIO5	5			GNDIO5	5		
38	VCCIO2	2			VCCIO5	5			VCCIO5	5		
39	TMS	2	TMS		TMS	5	TMS		TMS	5	TMS	
40	PB2C	2			PB2C	5		T	PB2A	5		T
41	PB3A	2		T	PB2D	5		C	PB2B	5		C
42	TCK	2	TCK		TCK	5	TCK		TCK	5	TCK	
43	PB3B	2		C	PB3A	5		T	PB3A	5		T
44	PB3C	2		T	PB3B	5		C	PB3B	5		C
45	PB3D	2		C	PB4A	5		T	PB4A	5		T
46	PB4A	2		T	PB4B	5		C	PB4B	5		C
47	TDO	2	TDO		TDO	5	TDO		TDO	5	TDO	
48	PB4B	2		C	PB4D	5			PB4D	5		
49	PB4C	2		T	PB5A	5		T	PB5A	5		T
50	PB4D	2		C	PB5B	5		C	PB5B	5		C
51	TDI	2	TDI		TDI	5	TDI		TDI	5	TDI	
52	VCC	—			VCC	—			VCC	—		
53	VCCAUX	—			VCCAUX	—			VCCAUX	—		
54	PB5A	2		T	PB6F	5			PB8F	5		
55	PB5B	2	PCLKT2_1[3]	C	PB7B	4	PCLK4_1[3]		PB10F	4	PCLK4_1[3]	
56	PB5D	2			PB7C	4		T	PB10C	4		T
57	PB6A	2		T	PB7D	4		C	PB10D	4		C
58	PB6B	2	PCLKT2_0[3]	C	PB7F	4	PCLK4_0[3]		PB10B	4	PCLK4_0[3]	
59	GND	—			GND	—			GND	—		
60	PB7C	2			PB9A	4		T	PB12A	4		T
61	PB7E	2			PB9B	4		C	PB12B	4		C
62	PB8A	2			PB9E	4			PB12E	4		
63	VCCIO2	2			VCCIO4	4			VCCIO4	4		
64	GNDIO2	2			GNDIO4	4			GNDIO4	4		
65	PB8C	2		T	PB10A	4		T	PB13A	4		T
66	PB8D	2		C	PB10B	4		C	PB13B	4		C
67	PB9A	2		T	PB10C	4		T	PB13C	4		T
68	PB9C	2		T	PB10D	4		C	PB13D	4		C
69	PB9B	2		C	PB10F	4			PB14D	4		
70[2]	SLEEPN	—	SLEEPN		SLEEPN	—	SLEEPN		SLEEPN	—	SLEEPN	
71	PB9D	2		C	PB11C	4		T	PB16C	4		T
72	PB9F	2			PB11D	4		C	PB16D	4		C
73	PR11D	1		C	PR16B	3		C	PR20B	3		C
74	PR11B	1		C	PR16A	3		T	PR20A	3		T
75	PR11C	1		T	PR15B	3		C[1]	PR19B	3		C
76	PR10D	1		C	PR15A	3		T[1]	PR19A	3		T
77	PR11A	1		T	PR14D	3		C	PR17D	3		C
78	PR10B	1		C	PR14C	3		T	PR17C	3		T
79	PR10C	1		T	PR14B	3		C[1]	PR17B	3		C[1]
80	PR10A	1		T	PR14A	3		T[1]	PR17A	3		T[1]
81	PR9D	1			PR13D	3			PR16D	3		

Pin Number	LCMXO640				LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
82	VCCIO1	1			VCCIO3	3			VCCIO3	3		
83	GNDIO1	1			GNDIO3	3			GNDIO3	3		
84	PR9A	1			PR12B	3		C[1]	PR15B	3		C[1]
85	PR8C	1			PR12A	3		T[1]	PR15A	3		T[1]
86	PR8A	1			PR11B	3		C[1]	PR14B	3		C[1]
87	PR7D	1			PR11A	3		T[1]	PR14A	3		T[1]
88	GND	—			GND	—			GND	—		
89	PR7B	1		C	PR10B	3		C[1]	PR13B	3		C[1]
90	PR7A	1		T	PR10A	3		T[1]	PR13A	3		T[1]
91	PR6D	1		C	PR8B	2		C[1]	PR10B	2		C[1]
92	PR6C	1		T	PR8A	2		T[1]	PR10A	2		T[1]
93	VCC	—			VCC	—			VCC	—		
94	PR5D	1			PR6B	2		C[1]	PR8B	2		C[1]
95	PR5B	1			PR6A	2		T[1]	PR8A	2		T[1]
96	PR4D	1			PR5B	2		C[1]	PR7B	2		C[1]
97	PR4B	1		C	PR5A	2		T[1]	PR7A	2		T[1]
98	VCCIO1	1			VCCIO2	2			VCCIO2	2		
99	GNDIO1	1			GNDIO2	2			GNDIO2	2		
100	PR4A	1		T	PR4C	2			PR5C	2		
101	PR3D	1		C	PR4B	2		C[1]	PR5B	2		C[1]
102	PR3C	1		T	PR4A	2		T[1]	PR5A	2		T[1]
103	PR3B	1		C	PR3D	2		C	PR4D	2		C
104	PR2D	1		C	PR3C	2		T	PR4C	2		T
105	PR3A	1		T	PR3B	2		C[1]	PR4B	2		C[1]
106	PR2B	1		C	PR3A	2		T[1]	PR4A	2		T[1]
107	PR2C	1		T	PR2B	2		C	PR3B	2		C[1]
108	PR2A	1		T	PR2A	2		T	PR3A	2		T[1]
109	PT9F	0		C	PT11D	1		C	PT16D	1		C
110	PT9D	0		C	PT11C	1		T	PT16C	1		T
111	PT9E	0		T	PT11B	1		C	PT16B	1		C
112	PT9B	0		C	PT11A	1		T	PT16A	1		T
113	PT9C	0		T	PT10F	1		C	PT15D	1		C
114	PT9A	0		T	PT10E	1		T	PT15C	1		T
115	PT8C	0			PT10D	1		C	PT14B	1		C
116	PT8B	0		C	PT10C	1		T	PT14A	1		T
117	VCCIO0	0			VCCIO1	1			VCCIO1	1		
118	GNDIO0	0			GNDIO1	1			GNDIO1	1		
119	PT8A	0		T	PT9F	1		C	PT12F	1		C
120	PT7E	0			PT9E	1		T	PT12E	1		T
121	PT7C	0			PT9B	1		C	PT12D	1		C
122	PT7A	0			PT9A	1		T	PT12C	1		T
123	GND	—			GND	—			GND	—		
124	PT6B	0	PCLK0_1[3]	C	PT7D	1	PCLK1_1[3]		PT10B	1	PCLK1_1[3]	
125	PT6A	0		T	PT7B	1		C	PT9D	1		C
126	PT5C	0			PT7A	1		T	PT9C	1		T
127	PT5B	0	PCLK0_0[3]		PT6F	0	PCLK1_0[3]		PT9B	1	PCLK1_0[3]	
128	VCCAUX	—			VCCAUX	—			VCCAUX	—		
129	VCC	—			VCC	—			VCC	—		
130	PT4D	0			PT5D	0		C	PT7B	0		C
131	PT4B	0		C	PT5C	0		T	PT7A	0		T
132	PT4A	0		T	PT5B	0		C	PT6D	0		
133	PT3F	0			PT5A	0		T	PT6E	0		T
134	PT3D	0			PT4B	0			PT6F	0		C
135	VCCIO0	0			VCCIO0	0			VCCIO0	0		
136	GNDIO0	0			GNDIO0	0			GNDIO0	0		

Pin Number	LCMXO640				LCMXO1200				LCMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
137	PT3B	0		C	PT3D	0		C	PT4B	0		T
138	PT2F	0		C	PT3C	0		T	PT4A	0		C
139	PT3A	0		T	PT3B	0		C	PT3B	0		C
140	PT2D	0		C	PT3A	0		T	PT3A	0		T
141	PT2E	0		T	PT2D	0		C	PT2D	0		C
142	PT2B	0		C	PT2C	0		T	PT2C	0		T
143	PT2C	0		T	PT2B	0		C	PT2B	0		C
144	PT2A	0		T	PT2A	0		T	PT2A	0		T

Notes:

1. Supports true LVDS outputs.
2. NC for “E” devices.
3. Primary clock inputs are single-ended.

4.10. LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 256 caBGA / 256 ftBGA

LCMXO640					LCMXO1200					LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
E4	NC				E4	PL2A	7		T	E4	PL2A	7	LUM0_PLLT_FB_A	T
E5	NC				E5	PL2B	7		C	E5	PL2B	7	LUM0_PLLC_FB_A	C
F5	NC				F5	PL3A	7		T[1]	F5	PL3A	7		T[1]
F6	NC				F6	PL3B	7		C[1]	F6	PL3B	7		C[1]
F3	PL3A	3		T	F3	PL3C	7		T	F3	PL3C	7	LUM0_PLLT_IN_A	T
F4	PL3B	3		C	F4	PL3D	7		C	F4	PL3D	7	LUM0_PLLC_IN_A	C
E3	PL2C	3		T	E3	PL4A	7		T[1]	E3	PL4A	7		T[1]
E2	PL2D	3		C	E2	PL4B	7		C[1]	E2	PL4B	7		C[1]
C3	NC				C3	PL4C	7		T	C3	PL4C	7		T
C2	NC				C2	PL4D	7		C	C2	PL4D	7		C
B1	PL2A	3		T	B1	PL5A	7		T[1]	B1	PL5A	7		T[1]
C1	PL2B	3		C	C1	PL5B	7		C[1]	C1	PL5B	7		C[1]
D2	PL3C	3		T	D2	PL5C	7		T	D2	PL6C	7		T
D1	PL3D	3		C	D1	PL5D	7		C	D1	PL6D	7		C
F2	PL5A	3		T	F2	PL6A	7		T[1]	F2	PL7A	7		T[1]
G2	PL5B	3	GSRN	C	G2	PL6B	7	GSRN	C[1]	G2	PL7B	7	GSRN	C[1]
E1	PL4A	3		T	E1	PL6C	7		T	E1	PL7C	7		T
F1	PL4B	3		C	F1	PL6D	7		C	F1	PL7D	7		C
G4	NC				G4	PL7A	7		T[1]	G4	PL8A	7		T[1]
G5	NC				G5	PL7B	7		C[1]	G5	PL8B	7		C[1]
G3	PL4C	3		T	G3	PL7C	7		T	G3	PL8C	7		T
H3	PL4D	3		C	H3	PL7D	7		C	H3	PL8D	7		C
H4	NC				H4	PL8A	7		T[1]	H4	PL9A	7		T[1]
H5	NC				H5	PL8B	7		C[1]	H5	PL9B	7		C[1]
G1	PL5C	3		T	G1	PL8C	7		T	G1	PL10C	7		T
H1	PL5D	3		C	H1	PL8D	7		C	H1	PL10D	7		C
H2	PL6A	3		T	H2	PL9A	6		T[1]	H2	PL11A	6		T[1]
J2	PL6B	3		C	J2	PL9B	6		C[1]	J2	PL11B	6		C[1]
J3	PL7C	3		T	J3	PL9C	6		T	J3	PL11C	6		T
K3	PL7D	3		C	K3	PL9D	6		C	K3	PL11D	6		C
J1	PL6C	3		T	J1	PL10A	6		T[1]	J1	PL12A	6		T[1]
K1	PL6D	3		C	K1	PL10B	6		C[1]	K1	PL12B	6		C[1]
K2	PL9A	3		T	K2	PL10C	6		T	K2	PL12C	6		T
L2	PL9B	3		C	L2	PL10D	6		C	L2	PL12D	6		C
L1	PL7A	3		T	L1	PL11A	6		T[1]	L1	PL13A	6		T[1]
M1	PL7B	3		C	M1	PL11B	6		C[1]	M1	PL13B	6		C[1]
P1	PL8D	3		C	P1	PL11D	6		C	P1	PL14D	6		C
N1	PL8C	3	TSALL	T	N1	PL11C	6	TSALL	T	N1	PL14C	6	TSALL	T
L3	PL10A	3		T	L3	PL12A	6		T[1]	L3	PL15A	6		T[1]
M3	PL10B	3		C	M3	PL12B	6		C[1]	M3	PL15B	6		C[1]
M2	PL9C	3		T	M2	PL12C	6		T	M2	PL15C	6		T
N2	PL9D	3		C	N2	PL12D	6		C	N2	PL15D	6		C
J4	PL8A	3		T	J4	PL13A	6		T[1]	J4	PL16A	6		T[1]
J5	PL8B	3		C	J5	PL13B	6		C[1]	J5	PL16B	6		C[1]
R1	PL11A	3		T	R1	PL13C	6		T	R1	PL16C	6		T
R2	PL11B	3		C	R2	PL13D	6		C	R2	PL16D	6		C
K5	NC				K5	PL14A	6	LLM0_PLLT_FB_A	T[1]	K5	PL17A	6	LLM0_PLLT_FB_A	T[1]
K4	NC				K4	PL14B	6	LLM0_PLLC_FB_A	C[1]	K4	PL17B	6	LLM0_PLLC_FB_A	C[1]
L5	PL10C	3		T	L5	PL14C	6		T	L5	PL17C	6		T
L4	PL10D	3		C	L4	PL14D	6		C	L4	PL17D	6		C

LCMXO640					LCMXO1200					LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**	**Ball Number**	**Ball Function**	**Bank**	**Dual Function**	**Differential**	**Ball Number**	**Ball Function**	**Bank**	**Dual Function**	**Differential**
M5	NC				M5	PL15A	6	LLM0_PLLT_IN_A	T[1]	M5	PL18A	6	LLM0_PLLT_IN_A	T[1]
M4	NC				M4	PL15B	6	LLM0_PLLC_IN_A	C[1]	M4	PL18B	6	LLM0_PLLC_IN_A	C[1]
N4	PL11C	3		T	N4	PL16A	6		T	N4	PL19A	6		T
N3	PL11D	3		C	N3	PL16B	6		C	N3	PL19B	6		C
P4	TMS	2	TMS		P4	TMS	5	TMS		P4	TMS	5	TMS	
P2	NC				P2	PB2A	5		T	P2	PB2A	5		T
P3	NC				P3	PB2B	5		C	P3	PB2B	5		C
N5	NC				N5	PB2C	5		T	N5	PB2C	5		T
R3	TCK	2	TCK		R3	TCK	5	TCK		R3	TCK	5	TCK	
N6	NC				N6	PB2D	5		C	N6	PB2D	5		C
T2	PB2A	2		T	T2	PB3A	5		T	T2	PB3A	5		T
T3	PB2B	2		C	T3	PB3B	5		C	T3	PB3B	5		C
R4	PB2C	2		T	R4	PB3C	5		T	R4	PB3C	5		T
R5	PB2D	2		C	R5	PB3D	5		C	R5	PB3D	5		C
P5	PB3A	2		T	P5	PB4A	5		T	P5	PB4A	5		T
P6	PB3B	2		C	P6	PB4B	5		C	P6	PB4B	5		C
T5	PB3C	2		T	T5	PB4C	5		T	T5	PB4C	5		T
M6	TDO	2	TDO		M6	TDO	5	TDO		M6	TDO	5	TDO	
T4	PB3D	2		C	T4	PB4D	5		C	T4	PB4D	5		C
R6	PB4A	2		T	R6	PB5A	5		T	R6	PB5A	5		T
T6	PB4B	2		C	T6	PB5B	5		C	T6	PB5B	5		C
N7	TDI	2	TDI		N7	TDI	5	TDI		N7	TDI	5	TDI	
T8	PB4C	2		T	T8	PB5C	5		T	T8	PB6A	5		T
T7	PB4D	2		C	T7	PB5D	5		C	T7	PB6B	5		C
M7	NC				M7	PB6A	5		T	M7	PB7C	5		T
M8	NC				M8	PB6B	5		C	M8	PB7D	5		C
T9	VCCAUX	—			T9	VCCAUX	—			T9	VCCAUX	—		
R7	PB4E	2		T	R7	PB6C	5		T	R7	PB8C	5		T
R8	PB4F	2		C	R8	PB6D	5		C	R8	PB8D	5		C
P7	PB5C	2		T	P7	PB6E	5		T	P7	PB9A	4		T
P8	PB5D	2		C	P8	PB6F	5		C	P8	PB9B	4		C
N8	PB5A	2		T	N8	PB7A	4		T	N8	PB10E	4		T
N9	PB5B	2	PCLK2_1[3]	C	N9	PB7B	4	PCLK4_1[3]	C	N9	PB10F	4	PCLK4_1[3]	C
P10	PB7B	2		C	P10	PB7D	4		C	P10	PB10D	4		C
P9	PB7A	2		T	P9	PB7C	4		T	P9	PB10C	4		T
M9	PB6B	2	PCLK2_0[3]	C	M9	PB7F	4	PCLK4_0[3]	C	M9	PB10B	4	PCLK4_0[3]	C
M10	PB6A	2		T	M10	PB7E	4		T	M10	PB10A	4		T
R9	PB6C	2		T	R9	PB8A	4		T	R9	PB11C	4		T
R10	PB6D	2		C	R10	PB8B	4		C	R10	PB11D	4		C
T10	PB7C	2		T	T10	PB8C	4		T	T10	PB12A	4		T
T11	PB7D	2		C	T11	PB8D	4		C	T11	PB12B	4		C
N10	NC				N10	PB8E	4		T	N10	PB12C	4		T
N11	NC				N11	PB8F	4		C	N11	PB12D	4		C
R11	PB7E	2		T	R11	PB9A	4		T	R11	PB13A	4		T
R12	PB7F	2		C	R12	PB9B	4		C	R12	PB13B	4		C
P11	PB8A	2		T	P11	PB9C	4		T	P11	PB13C	4		T
P12	PB8B	2		C	P12	PB9D	4		C	P12	PB13D	4		C
T13	PB8C	2		T	T13	PB9E	4		T	T13	PB14A	4		T
T12	PB8D	2		C	T12	PB9F	4		C	T12	PB14B	4		C
R13	PB9A	2		T	R13	PB10A	4		T	R13	PB14C	4		T
R14	PB9B	2		C	R14	PB10B	4		C	R14	PB14D	4		C
T14	PB9C	2		T	T14	PB10C	4		T	T14	PB15A	4		T
T15	PB9D	2		C	T15	PB10D	4		C	T15	PB15B	4		C
P13[2]	SLEEPN	—	SLEEPN		P13[2]	SLEEPN	—	SLEEPN		P13[2]	SLEEPN	—	SLEEPN	
P14	PB9F	2			P14	PB10F	4			P14	PB15D	4		
R15	NC				R15	PB11A	4		T	R15	PB16A	4		T
R16	NC				R16	PB11B	4		C	R16	PB16B	4		C
P15	NC				P15	PB11C	4		T	P15	PB16C	4		T
P16	NC				P16	PB11D	4		C	P16	PB16D	4		C

LCMXO640					LCMXO1200					LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
M11	NC				M11	PR16B	3		C	M11	PR20B	3		C
L11	NC				L11	PR16A	3		T	L11	PR20A	3		T
N12	NC				N12	PR15B	3		C[1]	N12	PR18B	3		C[1]
N13	NC				N13	PR15A	3		T[1]	N13	PR18A	3		T[1]
M13	NC				M13	PR14D	3		C	M13	PR17D	3		C
M12	NC				M12	PR14C	3		T	M12	PR17C	3		T
N14	PR11D	1		C	N14	PR14B	3		C[1]	N14	PR17B	3		C[1]
N15	PR11C	1		T	N15	PR14A	3		T[1]	N15	PR17A	3		T[1]
L13	PR11B	1		C	L13	PR13D	3		C	L13	PR16D	3		C
L12	PR11A	1		T	L12	PR13C	3		T	L12	PR16C	3		T
M14	PR10B	1		C	M14	PR13B	3		C[1]	M14	PR16B	3		C[1]
L14	PR10A	1		T	L14	PR13A	3		T[1]	L14	PR16A	3		T[1]
N16	PR10D	1		C	N16	PR12D	3		C	N16	PR15D	3		C
M16	PR10C	1		T	M16	PR12C	3		T	M16	PR15C	3		T
M15	PR9D	1		C	M15	PR12B	3		C[1]	M15	PR15B	3		C[1]
L15	PR9C	1		T	L15	PR12A	3		T[1]	L15	PR15A	3		T[1]
L16	PR9B	1		C	L16	PR11D	3		C	L16	PR14D	3		C
K16	PR9A	1		T	K16	PR11C	3		T	K16	PR14C	3		T
K13	PR8D	1		C	K13	PR11B	3		C[1]	K13	PR14B	3		C[1]
J13	PR8C	1		T	J13	PR11A	3		T[1]	J13	PR14A	3		T[1]
K14	PR8B	1		C	K14	PR10D	3		C	K14	PR13D	3		C
J14	PR8A	1		T	J14	PR10C	3		T	J14	PR13C	3		T
K15	PR7D	1		C	K15	PR10B	3		C[1]	K15	PR13B	3		C[1]
J15	PR7C	1		T	J15	PR10A	3		T[1]	J15	PR13A	3		T[1]
K12	NC				K12	PR9D	3		C	K12	PR11D	3		C
J12	NC				J12	PR9C	3		T	J12	PR11C	3		T
J16	PR7B	1		C	J16	PR9B	3		C[1]	J16	PR11B	3		C[1]
H16	PR7A	1		T	H16	PR9A	3		T[1]	H16	PR11A	3		T[1]
H15	PR6B	1		C	H15	PR8D	2		C	H15	PR10D	2		C
G15	PR6A	1		T	G15	PR8C	2		T	G15	PR10C	2		T
H14	PR5D	1		C	H14	PR8B	2		C[1]	H14	PR10B	2		C[1]
G14	PR5C	1		T	G14	PR8A	2		T[1]	G14	PR10A	2		T[1]
H13	PR6D	1		C	H13	PR7D	2		C	H13	PR9D	2		C
H12	PR6C	1		T	H12	PR7C	2		T	H12	PR9C	2		T
G13	PR4D	1		C	G13	PR7B	2		C[1]	G13	PR9B	2		C[1]
G12	PR4C	1		T	G12	PR7A	2		T[1]	G12	PR9A	2		T[1]
G16	PR5B	1		C	G16	PR6D	2		C	G16	PR7D	2		C
F16	PR5A	1		T	F16	PR6C	2		T	F16	PR7C	2		T
F15	PR4B	1		C	F15	PR6B	2		C[1]	F15	PR7B	2		C[1]
E15	PR4A	1		T	E15	PR6A	2		T[1]	E15	PR7A	2		T[1]
E16	PR3B	1		C	E16	PR5D	2		C	E16	PR6D	2		C
D16	PR3A	1		T	D16	PR5C	2		T	D16	PR6C	2		T
D15	PR2D	1		C	D15	PR5B	2		C[1]	D15	PR6B	2		C[1]
C15	PR2C	1		T	C15	PR5A	2		T[1]	C15	PR6A	2		T[1]
C16	PR2B	1		C	C16	PR4D	2		C	C16	PR5D	2		C
B16	PR2A	1		T	B16	PR4C	2		T	B16	PR5C	2		T
F14	PR3D	1		C	F14	PR4B	2		C[1]	F14	PR5B	2		C[1]
E14	PR3C	1		T	E14	PR4A	2		T[1]	E14	PR5A	2		T[1]
F12	NC				F12	PR3D	2		C	F12	PR4D	2		C
F13	NC				F13	PR3C	2		T	F13	PR4C	2		T
E12	NC				E12	PR3B	2		C[1]	E12	PR4B	2		C[1]
E13	NC				E13	PR3A	2		T[1]	E13	PR4A	2		T[1]
D13	NC				D13	PR2B	2		C	D13	PR3B	2		C[1]

LCMXO640					LCMXO1200					LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
D14	NC				D14	PR2A	2		T	D14	PR3A	2		T[1]
B15	NC				B15	PT11D	1		C	B15	PT16D	1		C
A15	NC				A15	PT11C	1		T	A15	PT16C	1		T
C14	NC				C14	PT11B	1		C	C14	PT16B	1		C
B14	NC				B14	PT11A	1		T	B14	PT16A	1		T
C13	PT9F	0		C	C13	PT10F	1		C	C13	PT15D	1		C
B13	PT9E	0		T	B13	PT10E	1		T	B13	PT15C	1		T
E11	NC				E11	PT10D	1		C	E11	PT15B	1		C
E10	NC				E10	PT10C	1		T	E10	PT15A	1		T
D12	PT9D	0		C	D12	PT10B	1		C	D12	PT14D	1		C
D11	PT9C	0		T	D11	PT10A	1		T	D11	PT14C	1		T
A14	PT7F	0		C	A14	PT9F	1		C	A14	PT14B	1		C
A13	PT7E	0		T	A13	PT9E	1		T	A13	PT14A	1		T
C12	PT8B	0		C	C12	PT9D	1		C	C12	PT13D	1		C
C11	PT8A	0		T	C11	PT9C	1		T	C11	PT13C	1		T
B12	PT7B	0		C	B12	PT9B	1		C	B12	PT12D	1		C
B11	PT7A	0		T	B11	PT9A	1		T	B11	PT12C	1		T
A12	PT7D	0		C	A12	PT8F	1		C	A12	PT12B	1		C
A11	PT7C	0		T	A11	PT8E	1		T	A11	PT12A	1		T
B10	PT5D	0		C	B10	PT8D	1		C	B10	PT11B	1		C
B9	PT5C	0		T	B9	PT8C	1		T	B9	PT11A	1		T
D10	PT8D	0		C	D10	PT8B	1		C	D10	PT10F	1		C
D9	PT8C	0		T	D9	PT8A	1		T	D9	PT10E	1		T
C10	PT6D	0		C	C10	PT7F	1		C	C10	PT10D	1		C
C9	PT6C	0		T	C9	PT7E	1		T	C9	PT10C	1		T
A9	PT6B	0	PCLK0_1[3]	C	A9	PT7D	1	PCLK1_1[3]	C	A9	PT10B	1	PCLK1_1[3]	C
A10	PT6A	0		T	A10	PT7C	1		T	A10	PT10A	1		T
E9	PT9B	0		C	E9	PT7B	1		C	E9	PT9D	1		C
E8	PT9A	0		T	E8	PT7A	1		T	E8	PT9C	1		T
D7	PT5B	0	PCLK0_0[3]	C	D7	PT6F	0	PCLK1_0[3]	C	D7	PT9B	1	PCLK1_0[3]	C
D8	PT5A	0		T	D8	PT6E	0		T	D8	PT9A	1		T
C8	PT4F	0		C	C8	PT6D	0		C	C8	PT8D	0		C
B8	PT4E	0		T	B8	PT6C	0		T	B8	PT8C	0		T
A8	VCCAUX	—			A8	VCCAUX	—			A8	VCCAUX	—		
A7	PT4D	0		C	A7	PT6B	0		C	A7	PT7D	0		C
A6	PT4C	0		T	A6	PT6A	0		T	A6	PT7C	0		T
B7	PT4B	0		C	B7	PT5F	0		C	B7	PT7B	0		C
B6	PT4A	0		T	B6	PT5E	0		T	B6	PT7A	0		T
C6	PT3C	0		T	C6	PT5C	0		T	C6	PT6A	0		T
C7	PT3D	0		C	C7	PT5D	0		C	C7	PT6B	0		C
A5	PT3E	0		T	A5	PT5A	0		T	A5	PT6C	0		T
A4	PT3F	0		C	A4	PT5B	0		C	A4	PT6D	0		C
E7	NC				E7	PT4C	0		T	E7	PT6E	0		T
E6	NC				E6	PT4D	0		C	E6	PT6F	0		C
B5	PT3B	0		C	B5	PT3F	0		C	B5	PT5D	0		C
B4	PT3A	0		T	B4	PT3E	0		T	B4	PT5C	0		T
D5	PT2D	0		C	D5	PT3D	0		C	D5	PT5B	0		C
D6	PT2C	0		T	D6	PT3C	0		T	D6	PT5A	0		T
C4	PT2E	0		T	C4	PT4A	0		T	C4	PT4A	0		T
C5	PT2F	0		C	C5	PT4B	0		C	C5	PT4B	0		C
D4	NC				D4	PT2D	0		C	D4	PT3D	0		C
D3	NC				D3	PT2C	0		T	D3	PT3C	0		T
A3	PT2B	0		C	A3	PT3B	0		C	A3	PT3B	0		C
A2	PT2A	0		T	A2	PT3A	0		T	A2	PT3A	0		T
B3	NC				B3	PT2B	0		C	B3	PT2D	0		C
B2	NC				B2	PT2A	0		T	B2	PT2C	0		T
A1	GND	—			A1	GND	—			A1	GND	—		
A16	GND	—			A16	GND	—			A16	GND	—		
F11	GND	—			F11	GND	—			F11	GND	—		
G8	GND	—			G8	GND	—			G8	GND	—		

LCMXO640					LCMXO1200					LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
G9	GND	—			G9	GND	—			G9	GND	—		
H7	GND	—			H7	GND	—			H7	GND	—		
H8	GND	—			H8	GND	—			H8	GND	—		
H9	GND	—			H9	GND	—			H9	GND	—		
H10	GND	—			H10	GND	—			H10	GND	—		
J7	GND	—			J7	GND	—			J7	GND	—		
J8	GND	—			J8	GND	—			J8	GND	—		
J9	GND	—			J9	GND	—			J9	GND	—		
J10	GND	—			J10	GND	—			J10	GND	—		
K8	GND	—			K8	GND	—			K8	GND	—		
K9	GND	—			K9	GND	—			K9	GND	—		
L6	GND	—			L6	GND	—			L6	GND	—		
T1	GND	—			T1	GND	—			T1	GND	—		
T16	GND	—			T16	GND	—			T16	GND	—		
G7	VCC	—			G7	VCC	—			G7	VCC	—		
G10	VCC	—			G10	VCC	—			G10	VCC	—		
K7	VCC	—			K7	VCC	—			K7	VCC	—		
K10	VCC	—			K10	VCC	—			K10	VCC	—		
H6	VCCIO3	3			H6	VCCIO7	7			H6	VCCIO7	7		
G6	VCCIO3	3			G6	VCCIO7	7			G6	VCCIO7	7		
K6	VCCIO3	3			K6	VCCIO6	6			K6	VCCIO6	6		
J6	VCCIO3	3			J6	VCCIO6	6			J6	VCCIO6	6		
L8	VCCIO2	2			L8	VCCIO5	5			L8	VCCIO5	5		
L7	VCCIO2	2			L7	VCCIO5	5			L7	VCCIO5	5		
L9	VCCIO2	2			L9	VCCIO4	4			L9	VCCIO4	4		
L10	VCCIO2	2			L10	VCCIO4	4			L10	VCCIO4	4		
K11	VCCIO1	1			K11	VCCIO3	3			K11	VCCIO3	3		
J11	VCCIO1	1			J11	VCCIO3	3			J11	VCCIO3	3		
H11	VCCIO1	1			H11	VCCIO2	2			H11	VCCIO2	2		
G11	VCCIO1	1			G11	VCCIO2	2			G11	VCCIO2	2		
F9	VCCIO0	0			F9	VCCIO1	1			F9	VCCIO1	1		
F10	VCCIO0	0			F10	VCCIO1	1			F10	VCCIO1	1		
F8	VCCIO0	0			F8	VCCIO0	0			F8	VCCIO0	0		
F7	VCCIO0	0			F7	VCCIO0	0			F7	VCCIO0	0		

Notes:

1. Supports true LVDS outputs.
2. NC for “E” devices.
3. Primary clock inputs are single-ended.

4.11. LCMXO2280 Logic Signal Connections: 324 ftBGA

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
D4	PL2A	7	LUM0_PLLT_FB_A	T
F5	PL2B	7	LUM0_PLLC_FB_A	C
B3	PL3A	7		T[1]
C3	PL3B	7		C[1]
E4	PL3C	7	LUM0_PLLT_IN_A	T
G6	PL3D	7	LUM0_PLLC_IN_A	C
A1	PL4A	7		T[1]
B1	PL4B	7		C[1]
F4	PL4C	7		T
E3	PL4D	7		C
D2	PL5A	7		T[1]
D3	PL5B	7		C[1]

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
G5	PL5C	7		T
F3	PL5D	7		C
C2	PL6A	7		T[1]
C1	PL6B	7		C[1]
H5	PL6C	7		T
G4	PL6D	7		C
E2	PL7A	7		T[1]
D1	PL7B	7	GSRN	C[1]
J6	PL7C	7		T
H4	PL7D	7		C
F2	PL8A	7		T[1]
E1	PL8B	7		C[1]
J3	PL8C	7		T
J5	PL8D	7		C
G3	PL9A	7		T[1]
H3	PL9B	7		C[1]
K3	PL9C	7		T
K5	PL9D	7		C
F1	PL10A	7		T[1]
G1	PL10B	7		C[1]
K4	PL10C	7		T
K6	PL10D	7		C
G2	PL11A	6		T[1]
H2	PL11B	6		C[1]
L3	PL11C	6		T
L5	PL11D	6		C
H1	PL12A	6		T[1]
J2	PL12B	6		C[1]
L4	PL12C	6		T
L6	PL12D	6		C
K2	PL13A	6		T[1]
K1	PL13B	6		C[1]
J1	PL13C	6		T
L2	PL13D	6		C
M5	PL14D	6		C
M3	PL14C	6	TSALL	T
L1	PL14B	6		C[1]
M2	PL14A	6		T[1]
M1	PL15A	6		T[1]
N1	PL15B	6		C[1]
M6	PL15C	6		T
M4	PL15D	6		C
P1	PL16A	6		T[1]
P2	PL16B	6		C[1]
N3	PL16C	6		T
N4	PL16D	6		C
T1	PL17A	6	LLM0_PLLT_FB_A	T[1]

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
R1	PL17B	6	LLM0_PLLC_FB_A	C[1]
P3	PL17C	6		T
N5	PL17D	6		C
R3	PL18A	6	LLM0_PLLT_IN_A	T[1]
R2	PL18B	6	LLM0_PLLC_IN_A	C[1]
P4	PL19A	6		T
N6	PL19B	6		C
U1	PL20A	6		T
T2	PL20B	6		C
P6	TMS	5	TMS	
V1	PB2A	5		T
U2	PB2B	5		C
T3	PB2C	5		T
N7	TCK	5	TCK	
R4	PB2D	5		C
R5	PB3A	5		T
T4	PB3B	5		C
R6	PB3C	5		T
P7	PB3D	5		C
U3	PB4A	5		T
T5	PB4B	5		C
V2	PB4C	5		T
N8	TDO	5	TDO	
V3	PB4D	5		C
T6	PB5A	5		T
U4	PB5B	5		C
P8	PB5C	5		T
T7	PB5D	5		C
V4	TDI	5	TDI	
R8	PB6A	5		T
N9	PB6B	5		C
U5	PB6C	5		T
V5	PB6D	5		C
U6	PB7A	5		T
V6	PB7B	5		C
P9	PB7C	5		T
T8	PB7D	5		C
U7	PB8A	5		T
V7	PB8B	5		C
M10	VCCAUX	—		
U8	PB8C	5		T
V8	PB8D	5		C
T9	PB8E	5		T
U9	PB8F	5		C
V9	PB9A	4		T
V10	PB9B	4		C
N10	PB9C	4		T

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
R10	PB9D	4		C
P10	PB10F	4	PCLK4_1[3]	C
T10	PB10E	4		T
U10	PB10D	4		C
V11	PB10C	4		T
U11	PB10B	4	PCLK4_0[3]	C
T11	PB10A	4		T
U12	PB11A	4		T
R11	PB11B	4		C
T12	PB11C	4		T
P11	PB11D	4		C
V12	PB12A	4		T
V13	PB12B	4		C
R12	PB12C	4		T
N11	PB12D	4		C
U13	PB12E	4		T
V14	PB12F	4		C
T13	PB13A	4		T
P12	PB13B	4		C
R13	PB13C	4		T
N12	PB13D	4		C
V15	PB14A	4		T
U14	PB14B	4		C
V16	PB14C	4		T
T14	PB14D	4		C
U15	PB15A	4		T
V17	PB15B	4		C
P13[2]	SLEEPN	—	SLEEPN	
T15	PB15D	4		
U16	PB16A	4		T
V18	PB16B	4		C
N13	PB16C	4		T
R14	PB16D	4		C
P15	PR20B	3		C
N14	PR20A	3		T
N15	PR19B	3		C
M13	PR19A	3		T
R15	PR18B	3		C[1]
T16	PR18A	3		T[1]
N16	PR17D	3		C
M14	PR17C	3		T
U17	PR17B	3		C[1]
U18	PR17A	3		T[1]
R17	PR16D	3		C
R16	PR16C	3		T
P16	PR16B	3		C[1]
P17	PR16A	3		T[1]

LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
L13	PR15D	3		C
M15	PR15C	3		T
T17	PR15B	3		C[1]
T18	PR15A	3		T[1]
L14	PR14D	3		C
L15	PR14C	3		T
R18	PR14B	3		C[1]
P18	PR14A	3		T[1]
K15	PR13D	3		C
K13	PR13C	3		T
N17	PR13B	3		C[1]
N18	PR13A	3		T[1]
K16	PR12D	3		C
K14	PR12C	3		T
M16	PR12B	3		C[1]
L16	PR12A	3		T[1]
J16	PR11D	3		C
J14	PR11C	3		T
M17	PR11B	3		C[1]
L17	PR11A	3		T[1]
J15	PR10D	2		C
J13	PR10C	2		T
M18	PR10B	2		C[1]
L18	PR10A	2		T[1]
H16	PR9D	2		C
H14	PR9C	2		T
K18	PR9B	2		C[1]
J18	PR9A	2		T[1]
J17	PR8D	2		C
H18	PR8C	2		T
H17	PR8B	2		C[1]
G17	PR8A	2		T[1]
H13	PR7D	2		C
H15	PR7C	2		T
G18	PR7B	2		C[1]
F18	PR7A	2		T[1]
G14	PR6D	2		C
G16	PR6C	2		T
E18	PR6B	2		C[1]
F17	PR6A	2		T[1]
G13	PR5D	2		C
G15	PR5C	2		T
E17	PR5B	2		C[1]
E16	PR5A	2		T[1]
F15	PR4D	2		C
E15	PR4C	2		T
D17	PR4B	2		C[1]

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
D18	PR4A	2		T[1]
B18	PR3D	2		C
C18	PR3C	2		T
C16	PR3B	2		C[1]
D16	PR3A	2		T[1]
C17	PR2B	2		C
D15	PR2A	2		T
E13	PT16D	1		C
C15	PT16C	1		T
F13	PT16B	1		C
D14	PT16A	1		T
A18	PT15D	1		C
B17	PT15C	1		T
A16	PT15B	1		C
A17	PT15A	1		T
D13	PT14D	1		C
F12	PT14C	1		T
C14	PT14B	1		C
E12	PT14A	1		T
C13	PT13D	1		C
B16	PT13C	1		T
B15	PT13B	1		C
A15	PT13A	1		T
B14	PT12F	1		C
A14	PT12E	1		T
D12	PT12D	1		C
F11	PT12C	1		T
B13	PT12B	1		C
A13	PT12A	1		T
C12	PT11D	1		C
B12	PT11C	1		T
E11	PT11B	1		C
D11	PT11A	1		T
C11	PT10F	1		C
A12	PT10E	1		T
F10	PT10D	1		C
D10	PT10C	1		T
B11	PT10B	1	PCLK1_1[3]	C
A11	PT10A	1		T
E10	PT9D	1		C
C10	PT9C	1		T
D9	PT9B	1	PCLK1_0[3]	C
E9	PT9A	1		T
B10	PT8F	0		C
A10	PT8E	0		T
A9	PT8D	0		C
C9	PT8C	0		T

LCMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
B9	PT8B	0		C
F9	VCCAUX	—		
A8	PT8A	0		T
B8	PT7D	0		C
C8	PT7C	0		T
A7	PT7B	0		C
B7	PT7A	0		T
A6	PT6A	0		T
B6	PT6B	0		C
D8	PT6C	0		T
F8	PT6D	0		C
C7	PT6E	0		T
E8	PT6F	0		C
D7	PT5D	0		C
E7	PT5C	0		T
A5	PT5B	0		C
C6	PT5A	0		T
B5	PT4A	0		T
A4	PT4B	0		C
D6	PT4C	0		T
F7	PT4D	0		C
B4	PT4E	0		T
C5	PT4F	0		C
F6	PT3D	0		C
E5	PT3C	0		T
E6	PT3B	0		C
D5	PT3A	0		T
A3	PT2D	0		C
C4	PT2C	0		T
A2	PT2B	0		C
B2	PT2A	0		T
E14	GND	—		
F16	GND	—		
H10	GND	—		
H11	GND	—		
H8	GND	—		
H9	GND	—		
J10	GND	—		
J11	GND	—		
J4	GND	—		
J8	GND	—		
J9	GND	—		
K10	GND	—		
K11	GND	—		
K17	GND	—		
K8	GND	—		
K9	GND	—		

LCMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
L10	GND	—		
L11	GND	—		
L8	GND	—		
L9	GND	—		
N2	GND	—		
P14	GND	—		
P5	GND	—		
R7	GND	—		
F14	VCC	—		
G11	VCC	—		
G9	VCC	—		
H7	VCC	—		
L7	VCC	—		
M9	VCC	—		
H6	VCCIO7	7		
J7	VCCIO7	7		
M7	VCCIO6	6		
K7	VCCIO6	6		
M8	VCCIO5	5		
R9	VCCIO5	5		
M12	VCCIO4	4		
M11	VCCIO4	4		
L12	VCCIO3	3		
K12	VCCIO3	3		
J12	VCCIO2	2		
H12	VCCIO2	2		
G12	VCCIO1	1		
G10	VCCIO1	1		
G8	VCCIO0	0		
G7	VCCIO0	0		

Notes:

1. Supports true LVDS outputs.
2. NC for “E” devices.
3. Primary clock inputs are single-ended.

4.12. Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

4.12.1. For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- Power Estimation and Management for MachXO Devices (FPGA-TN-02171)
- Power Calculator tool included with the Lattice ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

5. Ordering Information

5.1. Part Number Description

LCMXO XXXX X – X XXXXXX X XX

- Device Family
  - MachXO PLD
- Logic Capacity
  - 256 LUTs = 256
  - 640 LUTs = 640
  - 1200 LUTs = 1200
  - 2280 LUTs = 2280
- Supply Voltage
  - C = 1.8 V / 2.5 V / 3.3 V
  - E = 1.2 V
- Speed
  - 3 = Slowest
  - 4
  - 5 = Fastest
- Package
  - T100 = 100-pin TQFP
  - T144 = 144-pin TQFP
  - M100 = 100-ball csBGA
  - M132 = 132-ball csBGA
  - B256 = 256-ball caBGA
  - FT256 = 256-ball ftBGA
  - FT324 = 324-ball ftBGA
  - TN100 = 100-pin Lead-Free TQFP
  - TN144 = 144-pin Lead-Free TQFP
  - MN100 = 100-ball Lead-Free csBGA
  - MN132 = 132-ball Lead-Free csBGA
  - BN256 = 256-ball Lead-Free caBGA
  - FTN256 = 256-ball Lead-Free ftBGA
  - FTN324 = 324-ball Lead-Free ftBGA
- Grade
  - C = Commercial
  - I = Industrial
- ES = Engineering Sample
- Blank = Production Device

Note: Parts dual marked as described.

5.2. Ordering Information

Note: MachXO devices are dual marked except the slowest commercial speed grade device. For example the commercial speed grade LCMXO640E-4F256C is also marked with industrial grade -3I grade. The slowest commercial speed grade does not have industrial markings. The markings appears as follows:

Dual Mark

5.2.1. Conventional Packaging

Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3T100C	256	1.8 V / 2.5 V / 3.3 V	78	-3	TQFP	100	COM
LCMXO256C-4T100C	256	1.8 V / 2.5 V / 3.3 V	78	-4	TQFP	100	COM
LCMXO256C-5T100C	256	1.8 V / 2.5 V / 3.3 V	78	-5	TQFP	100	COM
LCMXO256C-3M100C	256	1.8V / 2.5 V / 3.3 V	78	-3	csBGA	100	COM
LCMXO256C-4M100C	256	1.8 V / 2.5 V / 3.3 V	78	-4	csBGA	100	COM
LCMXO256C-5M100C	256	1.8 V / 2.5 V / 3.3 V	78	-5	csBGA	100	COM
LCMXO640C-3T100C	640	1.8 V / 2.5 V / 3.3 V	74	-3	TQFP	100	COM
LCMXO640C-4T100C	640	1.8 V / 2.5 V / 3.3 V	74	-4	TQFP	100	COM
LCMXO640C-5T100C	640	1.8 V / 2.5 V / 3.3 V	74	-5	TQFP	100	COM
LCMXO640C-3M100C	640	1.8 V / 2.5 V / 3.3 V	74	-3	csBGA	100	COM
LCMXO640C-4M100C	640	1.8 V / 2.5 V / 3.3 V	74	-4	csBGA	100	COM
LCMXO640C-5M100C	640	1.8 V / 2.5 V / 3.3 V	74	-5	csBGA	100	COM
LCMXO640C-3T144C	640	1.8 V / 2.5 V / 3.3 V	113	-3	TQFP	144	COM
LCMXO640C-4T144C	640	1.8 V / 2.5 V / 3.3 V	113	-4	TQFP	144	COM
LCMXO640C-5T144C	640	1.8 V / 2.5 V / 3.3 V	113	-5	TQFP	144	COM
LCMXO640C-3M132C	640	1.8 V / 2.5 V / 3.3 V	101	-3	csBGA	132	COM
LCMXO640C-4M132C	640	1.8 V / 2.5 V / 3.3 V	101	-4	csBGA	132	COM
LCMXO640C-5M132C	640	1.8 V / 2.5 V / 3.3 V	101	-5	csBGA	132	COM
LCMXO640C-3B256C	640	1.8 V / 2.5 V / 3.3 V	159	-3	caBGA	256	COM
LCMXO640C-4B256C	640	1.8 V / 2.5 V / 3.3 V	159	-4	caBGA	256	COM
LCMXO640C-5B256C	640	1.8 V / 2.5 V / 3.3 V	159	-5	caBGA	256	COM
LCMXO640C-3FT256C	640	1.8 V / 2.5 V / 3.3 V	159	-3	ftBGA	256	COM
LCMXO640C-4FT256C	640	1.8 V / 2.5 V / 3.3 V	159	-4	ftBGA	256	COM
LCMXO640C-5FT256C	640	1.8 V / 2.5 V / 3.3 V	159	-5	ftBGA	256	COM
LCMXO1200C-3T100C	1200	1.8 V / 2.5 V / 3.3 V	73	-3	TQFP	100	COM
LCMXO1200C-4T100C	1200	1.8 V / 2.5 V / 3.3 V	73	-4	TQFP	100	COM
LCMXO1200C-5T100C	1200	1.8 V / 2.5 V / 3.3 V	73	-5	TQFP	100	COM
LCMXO1200C-3T144C	1200	1.8 V / 2.5 V / 3.3 V	113	-3	TQFP	144	COM
LCMXO1200C-4T144C	1200	1.8 V / 2.5 V / 3.3 V	113	-4	TQFP	144	COM
LCMXO1200C-5T144C	1200	1.8 V / 2.5 V / 3.3 V	113	-5	TQFP	144	COM
LCMXO1200C-3M132C	1200	1.8 V / 2.5 V / 3.3 V	101	-3	csBGA	132	COM
LCMXO1200C-4M132C	1200	1.8 V / 2.5 V / 3.3 V	101	-4	csBGA	132	COM
LCMXO1200C-5M132C	1200	1.8 V / 2.5 V / 3.3 V	101	-5	csBGA	132	COM
LCMXO1200C-3B256C	1200	1.8 V / 2.5 V / 3.3 V	211	-3	caBGA	256	COM
LCMXO1200C-4B256C	1200	1.8 V / 2.5 V / 3.3 V	211	-4	caBGA	256	COM
LCMXO1200C-5B256C	1200	1.8 V / 2.5 V / 3.3 V	211	-5	caBGA	256	COM
LCMXO1200C-3FT256C	1200	1.8 V / 2.5 V / 3.3 V	211	-3	ftBGA	256	COM
LCMXO1200C-4FT256C	1200	1.8 V / 2.5 V / 3.3 V	211	-4	ftBGA	256	COM
LCMXO1200C-5FT256C	1200	1.8 V / 2.5 V / 3.3 V	211	-5	ftBGA	256	COM
LCMXO2280C-3T100C	2280	1.8 V / 2.5 V / 3.3 V	73	-3	TQFP	100	COM
LCMXO2280C-4T100C	2280	1.8 V / 2.5 V / 3.3 V	73	-4	TQFP	100	COM
LCMXO2280C-5T100C	2280	1.8 V / 2.5 V / 3.3 V	73	-5	TQFP	100	COM
LCMXO2280C-3T144C	2280	1.8 V / 2.5 V / 3.3 V	113	-3	TQFP	144	COM
LCMXO2280C-4T144C	2280	1.8 V / 2.5 V / 3.3 V	113	-4	TQFP	144	COM
LCMXO2280C-5T144C	2280	1.8 V / 2.5 V / 3.3 V	113	-5	TQFP	144	COM
LCMXO2280C-3M132C	2280	1.8 V / 2.5 V / 3.3 V	101	-3	csBGA	132	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280C-4M132C	2280	1.8 V / 2.5 V / 3.3 V	101	-4	csBGA	132	COM
LCMXO2280C-5M132C	2280	1.8 V / 2.5 V / 3.3 V	101	-5	csBGA	132	COM
LCMXO2280C-3B256C	2280	1.8 V / 2.5 V / 3.3 V	211	-3	caBGA	256	COM
LCMXO2280C-4B256C	2280	1.8 V / 2.5 V / 3.3 V	211	-4	caBGA	256	COM
LCMXO2280C-5B256C	2280	1.8 V / 2.5 V / 3.3 V	211	-5	caBGA	256	COM
LCMXO2280C-3FT256C	2280	1.8 V / 2.5 V / 3.3 V	211	-3	ftBGA	256	COM
LCMXO2280C-4FT256C	2280	1.8 V / 2.5 V / 3.3 V	211	-4	ftBGA	256	COM
LCMXO2280C-5FT256C	2280	1.8 V / 2.5 V / 3.3 V	211	-5	ftBGA	256	COM
LCMXO2280C-3FT324C	2280	1.8 V / 2.5 V / 3.3 V	271	-3	ftBGA	324	COM
LCMXO2280C-4FT324C	2280	1.8 V / 2.5 V / 3.3 V	271	-4	ftBGA	324	COM
LCMXO2280C-5FT324C	2280	1.8 V / 2.5 V / 3.3 V	271	-5	ftBGA	324	COM
LCMXO256E-3T100C	256	1.2 V	78	-3	TQFP	100	COM
LCMXO256E-4T100C	256	1.2 V	78	-4	TQFP	100	COM
LCMXO256E-5T100C	256	1.2 V	78	-5	TQFP	100	COM
LCMXO256E-3M100C	256	1.2 V	78	-3	csBGA	100	COM
LCMXO256E-4M100C	256	1.2 V	78	-4	csBGA	100	COM
LCMXO256E-5M100C	256	1.2 V	78	-5	csBGA	100	COM
LCMXO640E-3T100C	640	1.2 V	74	-3	TQFP	100	COM
LCMXO640E-4T100C	640	1.2 V	74	-4	TQFP	100	COM
LCMXO640E-5T100C	640	1.2 V	74	-5	TQFP	100	COM
LCMXO640E-3M100C	640	1.2 V	74	-3	csBGA	100	COM
LCMXO640E-4M100C	640	1.2 V	74	-4	csBGA	100	COM
LCMXO640E-5M100C	640	1.2 V	74	-5	csBGA	100	COM
LCMXO640E-3T144C	640	1.2 V	113	-3	TQFP	144	COM
LCMXO640E-4T144C	640	1.2 V	113	-4	TQFP	144	COM
LCMXO640E-5T144C	640	1.2 V	113	-5	TQFP	144	COM
LCMXO640E-3M132C	640	1.2 V	101	-3	csBGA	132	COM
LCMXO640E-4M132C	640	1.2 V	101	-4	csBGA	132	COM
LCMXO640E-5M132C	640	1.2 V	101	-5	csBGA	132	COM
LCMXO640E-3B256C	640	1.2 V	159	-3	caBGA	256	COM
LCMXO640E-4B256C	640	1.2 V	159	-4	caBGA	256	COM
LCMXO640E-5B256C	640	1.2 V	159	-5	caBGA	256	COM
LCMXO640E-3FT256C	640	1.2 V	159	-3	ftBGA	256	COM
LCMXO640E-4FT256C	640	1.2 V	159	-4	ftBGA	256	COM
LCMXO640E-5FT256C	640	1.2 V	159	-5	ftBGA	256	COM
LCMXO1200E-3T100C	1200	1.2 V	73	-3	TQFP	100	COM
LCMXO1200E-4T100C	1200	1.2 V	73	-4	TQFP	100	COM
LCMXO1200E-5T100C	1200	1.2 V	73	-5	TQFP	100	COM
LCMXO1200E-3T144C	1200	1.2 V	113	-3	TQFP	144	COM
LCMXO1200E-4T144C	1200	1.2 V	113	-4	TQFP	144	COM
LCMXO1200E-5T144C	1200	1.2 V	113	-5	TQFP	144	COM
LCMXO1200E-3M132C	1200	1.2 V	101	-3	csBGA	132	COM
LCMXO1200E-4M132C	1200	1.2 V	101	-4	csBGA	132	COM
LCMXO1200E-5M132C	1200	1.2 V	101	-5	csBGA	132	COM
LCMXO1200E-3B256C	1200	1.2 V	211	-3	caBGA	256	COM
LCMXO1200E-4B256C	1200	1.2 V	211	-4	caBGA	256	COM
LCMXO1200E-5B256C	1200	1.2 V	211	-5	caBGA	256	COM
LCMXO1200E-3FT256C	1200	1.2 V	211	-3	ftBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200E-4FT256C	1200	1.2 V	211	-4	ftBGA	256	COM
LCMXO1200E-5FT256C	1200	1.2 V	211	-5	ftBGA	256	COM
LCMXO2280E-3T100C	2280	1.2 V	73	-3	TQFP	100	COM
LCMXO2280E-4T100C	2280	1.2 V	73	-4	TQFP	100	COM
LCMXO2280E-5T100C	2280	1.2 V	73	-5	TQFP	100	COM
LCMXO2280E-3T144C	2280	1.2 V	113	-3	TQFP	144	COM
LCMXO2280E-4T144C	2280	1.2 V	113	-4	TQFP	144	COM
LCMXO2280E-5T144C	2280	1.2 V	113	-5	TQFP	144	COM
LCMXO2280E-3M132C	2280	1.2 V	101	-3	csBGA	132	COM
LCMXO2280E-4M132C	2280	1.2 V	101	-4	csBGA	132	COM
LCMXO2280E-5M132C	2280	1.2 V	101	-5	csBGA	132	COM
LCMXO2280E-3B256C	2280	1.2 V	211	-3	caBGA	256	COM
LCMXO2280E-4B256C	2280	1.2 V	211	-4	caBGA	256	COM
LCMXO2280E-5B256C	2280	1.2 V	211	-5	caBGA	256	COM
LCMXO2280E-3FT256C	2280	1.2 V	211	-3	ftBGA	256	COM
LCMXO2280E-4FT256C	2280	1.2 V	211	-4	ftBGA	256	COM
LCMXO2280E-5FT256C	2280	1.2 V	211	-5	ftBGA	256	COM
LCMXO2280E-3FT324C	2280	1.2 V	271	-3	ftBGA	324	COM
LCMXO2280E-4FT324C	2280	1.2 V	271	-4	ftBGA	324	COM
LCMXO2280E-5FT324C	2280	1.2 V	271	-5	ftBGA	324	COM

5.2.2. Conventional Packaging

Industrial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3T100I	256	1.8 V / 2.5 V / 3.3 V	78	-3	TQFP	100	IND
LCMXO256C-4T100I	256	1.8 V / 2.5 V / 3.3 V	78	-4	TQFP	100	IND
LCMXO256C-3M100I	256	1.8 V / 2.5 V / 3.3 V	78	-3	csBGA	100	IND
LCMXO256C-4M100I	256	1.8 V / 2.5 V / 3.3 V	78	-4	csBGA	100	IND
LCMXO640C-3T100I	640	1.8 V / 2.5 V / 3.3 V	74	-3	TQFP	100	IND
LCMXO640C-4T100I	640	1.8 V / 2.5 V / 3.3 V	74	-4	TQFP	100	IND
LCMXO640C-3M100I	640	1.8 V / 2.5 V / 3.3 V	74	-3	csBGA	100	IND
LCMXO640C-4M100I	640	1.8 V / 2.5 V / 3.3 V	74	-4	csBGA	100	IND
LCMXO640C-3T144I	640	1.8 V / 2.5 V / 3.3 V	113	-3	TQFP	144	IND
LCMXO640C-4T144I	640	1.8 V / 2.5 V / 3.3 V	113	-4	TQFP	144	IND
LCMXO640C-3M132I	640	1.8 V / 2.5 V / 3.3 V	101	-3	csBGA	132	IND
LCMXO640C-4M132I	640	1.8 V / 2.5 V / 3.3 V	101	-4	csBGA	132	IND
LCMXO640C-3B256I	640	1.8 V / 2.5 V / 3.3 V	159	-3	caBGA	256	IND
LCMXO640C-4B256I	640	1.8 V / 2.5 V / 3.3 V	159	-4	caBGA	256	IND
LCMXO640C-3FT256I	640	1.8 V / 2.5 V / 3.3 V	159	-3	ftBGA	256	IND
LCMXO640C-4FT256I	640	1.8 V / 2.5 V / 3.3 V	159	-4	ftBGA	256	IND
LCMXO1200C-3T100I	1200	1.8 V / 2.5 V / 3.3 V	73	-3	TQFP	100	IND
LCMXO1200C-4T100I	1200	1.8 V / 2.5 V / 3.3 V	73	-4	TQFP	100	IND
LCMXO1200C-3T144I	1200	1.8 V / 2.5 V / 3.3 V	113	-3	TQFP	144	IND
LCMXO1200C-4T144I	1200	1.8 V / 2.5 V / 3.3 V	113	-4	TQFP	144	IND
LCMXO1200C-3M132I	1200	1.8 V / 2.5 V / 3.3 V	101	-3	csBGA	132	IND
LCMXO1200C-4M132I	1200	1.8 V / 2.5 V / 3.3 V	101	-4	csBGA	132	IND
LCMXO1200C-3B256I	1200	1.8 V / 2.5 V / 3.3 V	211	-3	caBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-4B256I	1200	1.8 V / 2.5 V / 3.3 V	211	-4	caBGA	256	IND
LCMXO1200C-3FT256I	1200	1.8 V / 2.5 V / 3.3 V	211	-3	ftBGA	256	IND
LCMXO1200C-4FT256I	1200	1.8 V / 2.5 V / 3.3 V	211	-4	ftBGA	256	IND
LCMXO2280C-3T100I	2280	1.8 V / 2.5 V / 3.3 V	73	-3	TQFP	100	IND
LCMXO2280C-4T100I	2280	1.8 V / 2.5 V / 3.3 V	73	-4	TQFP	100	IND
LCMXO2280C-3T144I	2280	1.8 V / 2.5 V / 3.3 V	113	-3	TQFP	144	IND
LCMXO2280C-4T144I	2280	1.8 V / 2.5 V / 3.3 V	113	-4	TQFP	144	IND
LCMXO2280C-3M132I	2280	1.8 V / 2.5 V / 3.3 V	101	-3	csBGA	132	IND
LCMXO2280C-4M132I	2280	1.8 V / 2.5 V / 3.3 V	101	-4	csBGA	132	IND
LCMXO2280C-3B256I	2280	1.8 V / 2.5 V / 3.3 V	211	-3	caBGA	256	IND
LCMXO2280C-4B256I	2280	1.8 V / 2.5 V / 3.3 V	211	-4	caBGA	256	IND
LCMXO2280C-3FT256I	2280	1.8 V / 2.5 V / 3.3 V	211	-3	ftBGA	256	IND
LCMXO2280C-4FT256I	2280	1.8 V / 2.5 V / 3.3 V	211	-4	ftBGA	256	IND
LCMXO2280C-3FT324I	2280	1.8 V / 2.5 V / 3.3 V	271	-3	ftBGA	324	IND
LCMXO2280C-4FT324I	2280	1.8 V / 2.5 V / 3.3 V	271	-4	ftBGA	324	IND
LCMXO256E-3T100I	256	1.2 V	78	-3	TQFP	100	IND
LCMXO256E-4T100I	256	1.2 V	78	-4	TQFP	100	IND
LCMXO256E-3M100I	256	1.2 V	78	-3	csBGA	100	IND
LCMXO256E-4M100I	256	1.2 V	78	-4	csBGA	100	IND
LCMXO640E-3T100I	640	1.2 V	74	-3	TQFP	100	IND
LCMXO640E-4T100I	640	1.2 V	74	-4	TQFP	100	IND
LCMXO640E-3M100I	640	1.2 V	74	-3	csBGA	100	IND
LCMXO640E-4M100I	640	1.2 V	74	-4	csBGA	100	IND
LCMXO640E-3T144I	640	1.2 V	113	-3	TQFP	144	IND
LCMXO640E-4T144I	640	1.2 V	113	-4	TQFP	144	IND
LCMXO640E-3M132I	640	1.2 V	101	-3	csBGA	132	IND
LCMXO640E-4M132I	640	1.2 V	101	-4	csBGA	132	IND
LCMXO640E-3B256I	640	1.2 V	159	-3	caBGA	256	IND
LCMXO640E-4B256I	640	1.2 V	159	-4	caBGA	256	IND
LCMXO640E-3FT256I	640	1.2 V	159	-3	ftBGA	256	IND
LCMXO640E-4FT256I	640	1.2 V	159	-4	ftBGA	256	IND
LCMXO1200E-3T100I	1200	1.2 V	73	-3	TQFP	100	IND
LCMXO1200E-4T100I	1200	1.2 V	73	-4	TQFP	100	IND
LCMXO1200E-3T144I	1200	1.2 V	113	-3	TQFP	144	IND
LCMXO1200E-4T144I	1200	1.2 V	113	-4	TQFP	144	IND
LCMXO1200E-3M132I	1200	1.2 V	101	-3	csBGA	132	IND
LCMXO1200E-4M132I	1200	1.2 V	101	-4	csBGA	132	IND
LCMXO1200E-3B256I	1200	1.2 V	211	-3	caBGA	256	IND
LCMXO1200E-4B256I	1200	1.2 V	211	-4	caBGA	256	IND
LCMXO1200E-3FT256I	1200	1.2 V	211	-3	ftBGA	256	IND
LCMXO1200E-4FT256I	1200	1.2 V	211	-4	ftBGA	256	IND
LCMXO2280E-3T100I	2280	1.2 V	73	-3	TQFP	100	IND
LCMXO2280E-4T100I	2280	1.2 V	73	-4	TQFP	100	IND
LCMXO2280E-3T144I	2280	1.2 V	113	-3	TQFP	144	IND
LCMXO2280E-4T144I	2280	1.2 V	113	-4	TQFP	144	IND
LCMXO2280E-3M132I	2280	1.2 V	101	-3	csBGA	132	IND
LCMXO2280E-4M132I	2280	1.2 V	101	-4	csBGA	132	IND
LCMXO2280E-3B256I	2280	1.2 V	211	-3	caBGA	256	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO2280E-4B256I	2280	1.2 V	211	-4	caBGA	256	IND
LCMXO2280E-3FT256I	2280	1.2 V	211	-3	ftBGA	256	IND
LCMXO2280E-4FT256I	2280	1.2 V	211	-4	ftBGA	256	IND
LCMXO2280E-3FT324I	2280	1.2 V	271	-3	ftBGA	324	IND
LCMXO2280E-4FT324I	2280	1.2 V	271	-4	ftBGA	324	IND

5.2.3. Lead-Free Packaging

Commercial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3TN100C	256	1.8 V / 2.5 V / 3.3 V	78	-3	Lead-Free TQFP	100	COM
LCMXO256C-4TN100C	256	1.8 V / 2.5 V / 3.3 V	78	-4	Lead-Free TQFP	100	COM
LCMXO256C-5TN100C	256	1.8 V / 2.5 V / 3.3 V	78	-5	Lead-Free TQFP	100	COM
LCMXO256C-3MN100C	256	1.8 V / 2.5 V / 3.3 V	78	-3	Lead-Free csBGA	100	COM
LCMXO256C-4MN100C	256	1.8 V / 2.5 V / 3.3 V	78	-4	Lead-Free csBGA	100	COM
LCMXO256C-5MN100C	256	1.8 V / 2.5 V / 3.3 V	78	-5	Lead-Free csBGA	100	COM
LCMXO640C-3TN100C	640	1.8 V / 2.5 V / 3.3 V	74	-3	Lead-Free TQFP	100	COM
LCMXO640C-4TN100C	640	1.8 V / 2.5 V / 3.3 V	74	-4	Lead-Free TQFP	100	COM
LCMXO640C-5TN100C	640	1.8 V / 2.5 V / 3.3 V	74	-5	Lead-Free TQFP	100	COM
LCMXO640C-3MN100C	640	1.8 V / 2.5 V / 3.3 V	74	-3	Lead-Free csBGA	100	COM
LCMXO640C-4MN100C	640	1.8 V / 2.5 V / 3.3 V	74	-4	Lead-Free csBGA	100	COM
LCMXO640C-5MN100C	640	1.8 V / 2.5 V / 3.3 V	74	-5	Lead-Free csBGA	100	COM
LCMXO640C-3TN144C	640	1.8 V / 2.5 V / 3.3 V	113	-3	Lead-Free TQFP	144	COM
LCMXO640C-4TN144C	640	1.8 V / 2.5 V / 3.3 V	113	-4	Lead-Free TQFP	144	COM
LCMXO640C-5TN144C	640	1.8 V / 2.5 V / 3.3 V	113	-5	Lead-Free TQFP	144	COM
LCMXO640C-3MN132C	640	1.8 V / 2.5 V / 3.3 V	101	-3	Lead-Free csBGA	132	COM
LCMXO640C-4MN132C	640	1.8 V / 2.5 V / 3.3 V	101	-4	Lead-Free csBGA	132	COM
LCMXO640C-5MN132C	640	1.8 V / 2.5 V / 3.3 V	101	-5	Lead-Free csBGA	132	COM
LCMXO640C-3BN256C	640	1.8 V / 2.5 V / 3.3 V	159	-3	Lead-Free caBGA	256	COM
LCMXO640C-4BN256C	640	1.8 V / 2.5 V / 3.3 V	159	-4	Lead-Free caBGA	256	COM
LCMXO640C-5BN256C	640	1.8 V / 2.5 V / 3.3 V	159	-5	Lead-Free caBGA	256	COM
LCMXO640C-3FTN256C	640	1.8 V / 2.5 V / 3.3 V	159	-3	Lead-Free ftBGA	256	COM
LCMXO640C-4FTN256C	640	1.8 V / 2.5 V / 3.3 V	159	-4	Lead-Free ftBGA	256	COM
LCMXO640C-5FTN256C	640	1.8 V / 2.5 V / 3.3 V	159	-5	Lead-Free ftBGA	256	COM
LCMXO1200C-3TN100C	1200	1.8 V / 2.5 V / 3.3 V	73	-3	Lead-Free TQFP	100	COM
LCMXO1200C-4TN100C	1200	1.8 V / 2.5 V / 3.3 V	73	-4	Lead-Free TQFP	100	COM
LCMXO1200C-5TN100C	1200	1.8 V / 2.5 V / 3.3 V	73	-5	Lead-Free TQFP	100	COM
LCMXO1200C-3TN144C	1200	1.8 V / 2.5 V / 3.3 V	113	-3	Lead-Free TQFP	144	COM
LCMXO1200C-4TN144C	1200	1.8 V / 2.5 V / 3.3 V	113	-4	Lead-Free TQFP	144	COM
LCMXO1200C-5TN144C	1200	1.8 V / 2.5 V / 3.3 V	113	-5	Lead-Free TQFP	144	COM
LCMXO1200C-3MN132C	1200	1.8 V / 2.5 V / 3.3 V	101	-3	Lead-Free csBGA	132	COM
LCMXO1200C-4MN132C	1200	1.8 V / 2.5 V / 3.3 V	101	-4	Lead-Free csBGA	132	COM
LCMXO1200C-5MN132C	1200	1.8 V / 2.5 V / 3.3 V	101	-5	Lead-Free csBGA	132	COM
LCMXO1200C-3BN256C	1200	1.8 V / 2.5 V / 3.3 V	211	-3	Lead-Free caBGA	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO1200C-4BN256C	1200	1.8 V / 2.5 V / 3.3 V	211	-4	Lead-Free caBGA	256	COM
LCMXO1200C-5BN256C	1200	1.8 V / 2.5 V / 3.3 V	211	-5	Lead-Free caBGA	256	COM
LCMXO1200C-3FTN256C	1200	1.8 V / 2.5 V / 3.3 V	211	-3	Lead-Free ftBGA	256	COM
LCMXO1200C-4FTN256C	1200	1.8 V / 2.5 V / 3.3 V	211	-4	Lead-Free ftBGA	256	COM
LCMXO1200C-5FTN256C	1200	1.8 V / 2.5 V / 3.3 V	211	-5	Lead-Free ftBGA	256	COM
LCMXO2280C-3TN100C	2280	1.8 V / 2.5 V / 3.3 V	73	-3	Lead-Free TQFP	100	COM
LCMXO2280C-4TN100C	2280	1.8 V / 2.5 V / 3.3 V	73	-4	Lead-Free TQFP	100	COM
LCMXO2280C-5TN100C	2280	1.8 V / 2.5 V / 3.3 V	73	-5	Lead-Free TQFP	100	COM
LCMXO2280C-3TN144C	2280	1.8 V / 2.5 V / 3.3 V	113	-3	Lead-Free TQFP	144	COM
LCMXO2280C-4TN144C	2280	1.8 V / 2.5 V / 3.3 V	113	-4	Lead-Free TQFP	144	COM
LCMXO2280C-5TN144C	2280	1.8 V / 2.5 V / 3.3 V	113	-5	Lead-Free TQFP	144	COM
LCMXO2280C-3MN132C	2280	1.8 V / 2.5 V / 3.3 V	101	-3	Lead-Free csBGA	132	COM
LCMXO2280C-4MN132C	2280	1.8 V / 2.5 V / 3.3 V	101	-4	Lead-Free csBGA	132	COM
LCMXO2280C-5MN132C	2280	1.8 V / 2.5 V / 3.3 V	101	-5	Lead-Free csBGA	132	COM
LCMXO2280C-3BN256C	2280	1.8 V / 2.5 V / 3.3 V	211	-3	Lead-Free caBGA	256	COM
LCMXO2280C-4BN256C	2280	1.8 V / 2.5 V / 3.3 V	211	-4	Lead-Free caBGA	256	COM
LCMXO2280C-5BN256C	2280	1.8 V / 2.5 V / 3.3 V	211	-5	Lead-Free caBGA	256	COM
LCMXO2280C-3FTN256C	2280	1.8 V / 2.5 V / 3.3 V	211	-3	Lead-Free ftBGA	256	COM
LCMXO2280C-4FTN256C	2280	1.8 V / 2.5 V / 3.3 V	211	-4	Lead-Free ftBGA	256	COM
LCMXO2280C-5FTN256C	2280	1.8 V / 2.5 V / 3.3 V	211	-5	Lead-Free ftBGA	256	COM
LCMXO2280C-3FTN324C	2280	1.8 V / 2.5 V / 3.3 V	271	-3	Lead-Free ftBGA	324	COM
LCMXO2280C-4FTN324C	2280	1.8 V / 2.5 V / 3.3 V	271	-4	Lead-Free ftBGA	324	COM
LCMXO2280C-5FTN324C	2280	1.8 V / 2.5 V / 3.3 V	271	-5	Lead-Free ftBGA	324	COM
LCMXO256E-3TN100C	256	1.2 V	78	-3	Lead-Free TQFP	100	COM
LCMXO256E-4TN100C	256	1.2 V	78	-4	Lead-Free TQFP	100	COM
LCMXO256E-5TN100C	256	1.2 V	78	-5	Lead-Free TQFP	100	COM
LCMXO256E-3MN100C	256	1.2 V	78	-3	Lead-Free csBGA	100	COM
LCMXO256E-4MN100C	256	1.2 V	78	-4	Lead-Free csBGA	100	COM
LCMXO256E-5MN100C	256	1.2 V	78	-5	Lead-Free csBGA	100	COM
LCMXO640E-3TN100C	640	1.2 V	74	-3	Lead-Free TQFP	100	COM
LCMXO640E-4TN100C	640	1.2 V	74	-4	Lead-Free TQFP	100	COM
LCMXO640E-5TN100C	640	1.2 V	74	-5	Lead-Free TQFP	100	COM
LCMXO640E-3MN100C	640	1.2 V	74	-3	Lead-Free csBGA	100	COM
LCMXO640E-4MN100C	640	1.2 V	74	-4	Lead-Free csBGA	100	COM
LCMXO640E-5MN100C	640	1.2 V	74	-5	Lead-Free csBGA	100	COM
LCMXO640E-3TN144C	640	1.2 V	113	-3	Lead-Free TQFP	144	COM
LCMXO640E-4TN144C	640	1.2 V	113	-4	Lead-Free TQFP	144	COM
LCMXO640E-5TN144C	640	1.2 V	113	-5	Lead-Free TQFP	144	COM
LCMXO640E-3MN132C	640	1.2 V	101	-3	Lead-Free csBGA	132	COM
LCMXO640E-4MN132C	640	1.2 V	101	-4	Lead-Free csBGA	132	COM
LCMXO640E-5MN132C	640	1.2 V	101	-5	Lead-Free csBGA	132	COM
LCMXO640E-3BN256C	640	1.2 V	159	-3	Lead-Free caBGA	256	COM
LCMXO640E-4BN256C	640	1.2 V	159	-4	Lead-Free	256	COM

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
					caBGA		
LCMXO640E-5BN256C	640	1.2 V	159	-5	Lead-Free caBGA	256	COM
LCMXO640E-3FTN256C	640	1.2 V	159	-3	Lead-Free ftBGA	256	COM
LCMXO640E-4FTN256C	640	1.2 V	159	-4	Lead-Free ftBGA	256	COM
LCMXO640E-5FTN256C	640	1.2 V	159	-5	Lead-Free ftBGA	256	COM
LCMXO1200E-3TN100C	1200	1.2 V	73	-3	Lead-Free TQFP	100	COM
LCMXO1200E-4TN100C	1200	1.2 V	73	-4	Lead-Free TQFP	100	COM
LCMXO1200E-5TN100C	1200	1.2 V	73	-5	Lead-Free TQFP	100	COM
LCMXO1200E-3TN144C	1200	1.2 V	113	-3	Lead-Free TQFP	144	COM
LCMXO1200E-4TN144C	1200	1.2 V	113	-4	Lead-Free TQFP	144	COM
LCMXO1200E-5TN144C	1200	1.2 V	113	-5	Lead-Free TQFP	144	COM
LCMXO1200E-3MN132C	1200	1.2 V	101	-3	Lead-Free csBGA	132	COM
LCMXO1200E-4MN132C	1200	1.2 V	101	-4	Lead-Free csBGA	132	COM
LCMXO1200E-5MN132C	1200	1.2 V	101	-5	Lead-Free csBGA	132	COM
LCMXO1200E-3BN256C	1200	1.2 V	211	-3	Lead-Free caBGA	256	COM
LCMXO1200E-4BN256C	1200	1.2 V	211	-4	Lead-Free caBGA	256	COM
LCMXO1200E-5BN256C	1200	1.2 V	211	-5	Lead-Free caBGA	256	COM
LCMXO1200E-3FTN256C	1200	1.2 V	211	-3	Lead-Free ftBGA	256	COM
LCMXO1200E-4FTN256C	1200	1.2 V	211	-4	Lead-Free ftBGA	256	COM
LCMXO1200E-5FTN256C	1200	1.2 V	211	-5	Lead-Free ftBGA	256	COM
LCMXO2280E-3TN100C	2280	1.2 V	73	-3	Lead-Free TQFP	100	COM
LCMXO2280E-4TN100C	2280	1.2 V	73	-4	Lead-Free TQFP	100	COM
LCMXO2280E-5TN100C	2280	1.2 V	73	-5	Lead-Free TQFP	100	COM
LCMXO2280E-3TN144C	2280	1.2 V	113	-3	Lead-Free TQFP	144	COM
LCMXO2280E-4TN144C	2280	1.2 V	113	-4	Lead-Free TQFP	144	COM
LCMXO2280E-5TN144C	2280	1.2 V	113	-5	Lead-Free TQFP	144	COM
LCMXO2280E-3MN132C	2280	1.2 V	101	-3	Lead-Free csBGA	132	COM
LCMXO2280E-4MN132C	2280	1.2 V	101	-4	Lead-Free csBGA	132	COM
LCMXO2280E-5MN132C	2280	1.2 V	101	-5	Lead-Free csBGA	132	COM
LCMXO2280E-3BN256C	2280	1.2 V	211	-3	Lead-Free caBGA	256	COM
LCMXO2280E-4BN256C	2280	1.2 V	211	-4	Lead-Free caBGA	256	COM
LCMXO2280E-5BN256C	2280	1.2 V	211	-5	Lead-Free caBGA	256	COM
LCMXO2280E-3FTN256C	2280	1.2 V	211	-3	Lead-Free ftBGA	256	COM
LCMXO2280E-4FTN256C	2280	1.2 V	211	-4	Lead-Free ftBGA	256	COM
LCMXO2280E-5FTN256C	2280	1.2 V	211	-5	Lead-Free ftBGA	256	COM
LCMXO2280E-3FTN324C	2280	1.2 V	271	-3	Lead-Free ftBGA	324	COM
LCMXO2280E-4FTN324C	2280	1.2 V	271	-4	Lead-Free ftBGA	324	COM
LCMXO2280E-5FTN324C	2280	1.2 V	271	-5	Lead-Free ftBGA	324	COM

5.2.4. Lead-Free Packaging

Industrial

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO256C-3TN100I	256	1.8 V / 2.5 V / 3.3 V	78	-3	Lead-Free TQFP	100	IND
LCMXO256C-4TN100I	256	1.8 V / 2.5 V / 3.3 V	78	-4	Lead-Free TQFP	100	IND
LCMXO256C-3MN100I	256	1.8 V / 2.5 V / 3.3 V	78	-3	Lead-Free csBGA	100	IND
LCMXO256C-4MN100I	256	1.8 V / 2.5 V / 3.3 V	78	-4	Lead-Free csBGA	100	IND
LCMXO640C-3TN100I	640	1.8 V / 2.5 V / 3.3 V	74	-3	Lead-Free TQFP	100	IND
LCMXO640C-4TN100I	640	1.8 V / 2.5 V / 3.3 V	74	-4	Lead-Free TQFP	100	IND
LCMXO640C-3MN100I	640	1.8 V / 2.5 V / 3.3 V	74	-3	Lead-Free csBGA	100	IND
LCMXO640C-4MN100I	640	1.8 V / 2.5 V / 3.3 V	74	-4	Lead-Free csBGA	100	IND
LCMXO640C-3TN144I	640	1.8 V / 2.5 V / 3.3 V	113	-3	Lead-Free TQFP	144	IND
LCMXO640C-4TN144I	640	1.8 V / 2.5 V / 3.3 V	113	-4	Lead-Free TQFP	144	IND
LCMXO640C-3MN132I	640	1.8 V / 2.5 V / 3.3 V	101	-3	Lead-Free csBGA	132	IND
LCMXO640C-4MN132I	640	1.8 V / 2.5 V / 3.3 V	101	-4	Lead-Free csBGA	132	IND
LCMXO640C-3BN256I	640	1.8 V / 2.5 V / 3.3 V	159	-3	Lead-Free caBGA	256	IND
LCMXO640C-4BN256I	640	1.8 V / 2.5 V / 3.3 V	159	-4	Lead-Free caBGA	256	IND
LCMXO640C-3FTN256I	640	1.8 V / 2.5 V / 3.3 V	159	-3	Lead-Free ftBGA	256	IND
LCMXO640C-4FTN256I	640	1.8 V / 2.5 V / 3.3 V	159	-4	Lead-Free ftBGA	256	IND
LCMXO1200C-3TN100I	1200	1.8 V / 2.5 V / 3.3 V	73	-3	Lead-Free TQFP	100	IND
LCMXO1200C-4TN100I	1200	1.8 V / 2.5 V / 3.3 V	73	-4	Lead-Free TQFP	100	IND
LCMXO1200C-3TN144I	1200	1.8 V / 2.5 V / 3.3 V	113	-3	Lead-Free TQFP	144	IND
LCMXO1200C-4TN144I	1200	1.8 V / 2.5 V / 3.3 V	113	-4	Lead-Free TQFP	144	IND
LCMXO1200C-3MN132I	1200	1.8 V / 2.5 V / 3.3 V	101	-3	Lead-Free csBGA	132	IND
LCMXO1200C-4MN132I	1200	1.8 V / 2.5 V / 3.3 V	101	-4	Lead-Free csBGA	132	IND
LCMXO1200C-3BN256I	1200	1.8 V / 2.5 V / 3.3 V	211	-3	Lead-Free caBGA	256	IND
LCMXO1200C-4BN256I	1200	1.8 V / 2.5 V / 3.3 V	211	-4	Lead-Free caBGA	256	IND
LCMXO1200C-3FTN256I	1200	1.8 V / 2.5 V / 3.3 V	211	-3	Lead-Free ftBGA	256	IND
LCMXO1200C-4FTN256I	1200	1.8 V / 2.5 V / 3.3 V	211	-4	Lead-Free ftBGA	256	IND
LCMXO2280C-3TN100I	2280	1.8 V / 2.5 V / 3.3 V	73	-3	Lead-Free TQFP	100	IND
LCMXO2280C-4TN100I	2280	1.8 V / 2.5 V / 3.3 V	73	-4	Lead-Free TQFP	100	IND
LCMXO2280C-3TN144I	2280	1.8 V / 2.5 V / 3.3 V	113	-3	Lead-Free TQFP	144	IND
LCMXO2280C-4TN144I	2280	1.8 V / 2.5 V / 3.3 V	113	-4	Lead-Free TQFP	144	IND
LCMXO2280C-3MN132I	2280	1.8 V / 2.5 V / 3.3 V	101	-3	Lead-Free csBGA	132	IND
LCMXO2280C-4MN132I	2280	1.8 V / 2.5 V / 3.3 V	101	-4	Lead-Free csBGA	132	IND
LCMXO2280C-3BN256I	2280	1.8 V / 2.5 V / 3.3 V	211	-3	Lead-Free caBGA	256	IND
LCMXO2280C-4BN256I	2280	1.8 V / 2.5 V / 3.3 V	211	-4	Lead-Free caBGA	256	IND
LCMXO2280C-3FTN256I	2280	1.8 V / 2.5 V / 3.3 V	211	-3	Lead-Free ftBGA	256	IND
LCMXO2280C-4FTN256I	2280	1.8 V / 2.5 V / 3.3 V	211	-4	Lead-Free ftBGA	256	IND
LCMXO2280C-3FTN324I	2280	1.8 V / 2.5 V / 3.3 V	271	-3	Lead-Free ftBGA	324	IND
LCMXO2280C-4FTN324I	2280	1.8 V / 2.5 V / 3.3 V	271	-4	Lead-Free ftBGA	324	IND
LCMXO256E-3TN100I	256	1.2 V	78	-3	Lead-Free TQFP	100	IND
LCMXO256E-4TN100I	256	1.2 V	78	-4	Lead-Free TQFP	100	IND
LCMXO256E-3MN100I	256	1.2 V	78	-3	Lead-Free csBGA	100	IND
LCMXO256E-4MN100I	256	1.2 V	78	-4	Lead-Free csBGA	100	IND
LCMXO640E-3TN100I	640	1.2 V	74	-3	Lead-Free TQFP	100	IND
LCMXO640E-4TN100I	640	1.2 V	74	-4	Lead-Free TQFP	100	IND
LCMXO640E-3MN100I	640	1.2 V	74	-3	Lead-Free csBGA	100	IND
LCMXO640E-4MN100I	640	1.2 V	74	-4	Lead-Free csBGA	100	IND

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LCMXO640E-3TN144I	640	1.2 V	113	-3	Lead-Free TQFP	144	IND
LCMXO640E-4TN144I	640	1.2 V	113	-4	Lead-Free TQFP	144	IND
LCMXO640E-3MN132I	640	1.2 V	101	-3	Lead-Free csBGA	132	IND
LCMXO640E-4MN132I	640	1.2 V	101	-4	Lead-Free csBGA	132	IND
LCMXO640E-3BN256I	640	1.2 V	159	-3	Lead-Free caBGA	256	IND
LCMXO640E-4BN256I	640	1.2 V	159	-4	Lead-Free caBGA	256	IND
LCMXO640E-3FTN256I	640	1.2 V	159	-3	Lead-Free ftBGA	256	IND
LCMXO640E-4FTN256I	640	1.2 V	159	-4	Lead-Free ftBGA	256	IND
LCMXO1200E-3TN100I	1200	1.2 V	73	-3	Lead-Free TQFP	100	IND
LCMXO1200E-4TN100I	1200	1.2 V	73	-4	Lead-Free TQFP	100	IND
LCMXO1200E-3TN144I	1200	1.2 V	113	-3	Lead-Free TQFP	144	IND
LCMXO1200E-4TN144I	1200	1.2 V	113	-4	Lead-Free TQFP	144	IND
LCMXO1200E-3MN132I	1200	1.2 V	101	-3	Lead-Free csBGA	132	IND
LCMXO1200E-4MN132I	1200	1.2 V	101	-4	Lead-Free csBGA	132	IND
LCMXO1200E-3BN256I	1200	1.2 V	211	-3	Lead-Free caBGA	256	IND
LCMXO1200E-4BN256I	1200	1.2 V	211	-4	Lead-Free caBGA	256	IND
LCMXO1200E-3FTN256I	1200	1.2 V	211	-3	Lead-Free ftBGA	256	IND
LCMXO1200E-4FTN256I	1200	1.2 V	211	-4	Lead-Free ftBGA	256	IND
LCMXO2280E-3TN100I	2280	1.2 V	73	-3	Lead-Free TQFP	100	IND
LCMXO2280E-4TN100I	2280	1.2 V	73	-4	Lead-Free TQFP	100	IND
LCMXO2280E-3TN144I	2280	1.2 V	113	-3	Lead-Free TQFP	144	IND
LCMXO2280E-4TN144I	2280	1.2 V	113	-4	Lead-Free TQFP	144	IND
LCMXO2280E-3MN132I	2280	1.2 V	101	-3	Lead-Free csBGA	132	IND
LCMXO2280E-4MN132I	2280	1.2 V	101	-4	Lead-Free csBGA	132	IND
LCMXO2280E-3BN256I	2280	1.2 V	211	-3	Lead-Free caBGA	256	IND
LCMXO2280E-4BN256I	2280	1.2 V	211	-4	Lead-Free caBGA	256	IND
LCMXO2280E-3FTN256I	2280	1.2 V	211	-3	Lead-Free ftBGA	256	IND
LCMXO2280E-4FTN256I	2280	1.2 V	211	-4	Lead-Free ftBGA	256	IND
LCMXO2280E-3FTN324I	2280	1.2 V	271	-3	Lead-Free ftBGA	324	IND
LCMXO2280E-4FTN324I	2280	1.2 V	271	-4	Lead-Free ftBGA	324	IND

6. Supplemental Information

For Further Information

A variety of technical notes for the MachXO family are available on the Lattice website.

- MachXO sysIO Usage Guide (FPGA-TN-02169)
- MachXO sysCLOCK Design and Usage Guide (FPGA-TN-02168)
- Memory Usage Guide for MachXO Devices (FPGA-TN-02170)
- Power Estimation and Management for MachXO Devices (FPGA-TN-02171)
- MachXO JTAG Programming and Configuration User's Guide (FPGA-TN-02167)
- Minimizing System Interruption During Configuration Using TransFR Technology
- MachXO Density Migration (FPGA-TN-02025)
- Boundary Scan Testability with Lattice sysIO Capability (AN8066)

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS): www.jedec.org
- PCI: www.pcisig.com

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 3.3, July 2022

Section	Change Summary
Pinout Information	Removed unnecessary VCCIOx/GND entries from LCMXO640, LCMXO1200 and LCMXO2280 Logic Signal Connections: 256 caBGA / 256 ftBGA and LCMXO2280 Logic Signal Connections: 324 ftBGA sections.

Revision 3.2, January 2020

Section	Change Summary
All	• Changed document number from DS1002 to FPGA-DS-02071. • Updated document template.
Disclaimers	Added this section.

Revision 3.1, June 2017

Section	Change Summary
All	Minor style/format changes.
Architecture	Clarified 'Off' Leakage reference in Figure 2.11., Characteristics of Normal, Off and Sleep Modes. Added footnote.
DC and Switching Characteristics	Updated MachXO256 and MachXO640 Hot Socketing Specifications table – Changed IPW to IPD in footnote 3.
Ordering Information	Updated logo in markings.

Revision 3.0, June 2013

Section	Change Summary
All	Updated document with new corporate logo.
Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.
DC and Switching Characteristics	• MachXO1200 and MachXO2280 Hot Socketing Specifications table –Removed footnote 4. • Added MachXO Programming/Erase Specifications table.

Revision 2.9, July 2010

Section	Change Summary
DC and Switching Characteristics	Updated sysCLOCK PLL Timing table.

Revision 2.8, June 2009

Section	Change Summary
Introduction	Added 0.8-mm 256-pin caBGA package to MachXO Family Selection Guide table.
Pinout Information	Added Logic Signal Connections table for 0.8-mm 256-pin caBGA package.
Ordering Information	Updated Part Number Description diagram and Ordering Part Number tables with 0.8-mm 256-pin caBGA package information.

Revision 2.7, November 2007

Section	Change Summary
DC and Switching Characteristics	Added JTAG Port Timing Waveforms diagram.
Pinout Information	Added Thermal Management text section.
Supplemental Information	Updated title list.

Revision 2.6, August 2007

Section	Change Summary
DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics table.

Revision 2.5, February 2007

Section	Change Summary
Architecture	Updated EBR Asynchronous Reset section.

Revision 2.4, December 2006

Section	Change Summary
Architecture	EBR Asynchronous Reset section added.
Pinout Information	Power Supply and NC table: Pin/Ball orientation footnotes added.

Revision 2.3, November 2006

Section	Change Summary
DC and Switching Characteristics	• Corrections to MachXO "C" Sleep Mode Timing table - value for tWSLEEPN (400ns) changed from max. to min. Value for tWAWAKE (100ns) changed from min. to max. • Added Flash Download Time table.

Revision 2.2, August 2006

Section	Change Summary
Multiple	Removed 256 fpBGA information for MachXO640.

Revision 2.1, May 2006

Section	Change Summary
Pinout Information	• Removed [LOC][0]_PLL_RST from Signal Description table. • PCLK footnote has been added to all appropriate pins.

Revision 2.0, April 2006

Section	Change Summary
Introduction	Introduction paragraphs updated.
Architecture	• Architecture Overview paragraphs updated. • "Top View of the MachXO1200 Device" figure updated. • "Top View of the MachXO640 Device" figure updated. • "Top View of the MachXO256 Device" figure updated. • "Slice Diagram" figure updated. • Slice Signal Descriptions table updated. • Routing section updated. • sysCLOCK Phase Lockecd Loops (PLLs) section updated. • PLL Diagram updated. • PLL Signal Descriptions table updated. • sysMEM Memory section has been updated. • PIO Groups section has been updated. • PIO section has been updated. • MachXO PIO Block Diagram updated. • Supported Input Standards table updated. • MachXO Configuration and Programming diagram updated.
DC and Switching Characteristics	• Recommended Operating Conditions table - footnotes updated. • MachXO256 and MachXO640 Hot Socketing Specifications – footnotes updated. • Added MachXO1200 and MachXO2280 Hot Socketing Specifications table. • DC Electrical Characteristics, footnotes have been updated. • Supply Current (Sleep Mode) table has been updated, removed "4W" references. Footnotes have been updated. • Supply Current (Standby) table and associated footnotes updated. • Intialization Supply Current table and footnotes updated. • Programming and Erase Flash Supply Current table and associated footnotes have been updated.

Section	Change Summary
	• Register-to-Register Performance table updated (rev. A 0.19). • MachXO External Switching Characteristics updated (rev. A 0.19). • MachXO Internal Timing Parameters updated (rev. A 0.19). • MachXO Family Timing Adders updated (rev. A 0.19). • sysCLOCK Timing updated (rev. A 0.19). • MachXO "C" Sleep Mode Timing updated (A 0.19). • JTAG Port Timing Specification updated (rev. A 0.19). • Test Fixture Required Components table updated.
Pinout Information	• Signal Descriptions have been updated. • Pin Information Summary has been updated. Footnote has been added. • Power Supply and NC Connection table has been updated. • Logic Signal Connections have been updated (PCLKTx_x --> PCLKx_x)
Ordering Information	• Removed "4W" references. • Added 256-ftBGA Ordering Part Numbers for MachXO640.

Revision 1.3, December 2005

Section	Change Summary
DC and Switching Characteristics	Supply Current (Standby) table updated with LCMXO1200/2280 data.
Ordering Information	Ordering Part Number section updated (added LCMXO2280C "4W").

Revision 1.2, November 2005

Section	Change Summary
Pinout Information	Added “Power Supply and NC Connections” summary information for LCMXO1200 and LCMXO2280 in 100 TQFP package.

Revision 1.1, October 2005

Section	Change Summary
Introduction	Distributed RAM information in family table updated. Added footnote 1 - fpBGA packaging to the family selection guide.
Architecture	• sysIO Buffer section updated. • Hot Socketing section updated. • Sleep Mode section updated. • SLEEP Pin Characteristics section updated. • Oscillator section updated. • Security section updated.
DC and Switching Characteristics	• Recommended Operating Conditions table updated. • DC Electrical Characteristics table updated. • Supply Current (Sleep Mode) table added with LCMXO256/640 data. • Supply Current (Standby) table updated with LCMXO256/640 data. • Initialization Supply Current table updated with LCMXO256/640 data. • Programming and Erase Flash Supply Current table updated with LCMXO256/640 data. • Register-to-Register Performance table updated (rev. A 0.16). • External Switching Characteristics table updated (rev. A 0.16). • Internal Timing Parameter table updated (rev. A 0.16). • Family Timing Adders updated (rev. A 0.16). • sysCLOCK Timing updated (rev. A 0.16). • MachXO "C" Sleep Mode Timing updated (A 0.16). • JTAG Port Timing Specification updated (rev. A 0.16).
Pinout Information	• SLEEPIN description updated. • Pin Information Summary updated. • Power Supply and NC Connection table has been updated. • Logic Signal Connection section has been updated to include all devices/packages.

Section	Change Summary
Ordering Information	• Part Number Description section has been updated. • Ordering Part Number section has been updated (added LCMXO256C/LCMXO640C "4W").
Supplemental Information	MachXO Density Migration Technical Note (TN1097) added.

Revision 1.0, February 2005

Section	Change Summary
All	Initial release.

LATTICE SEMICONDUCTOR®

www.latticesemi.com