National Semiconductor

ADVANCED INFORMATION

54F/74F597
8-Bit Shift Register

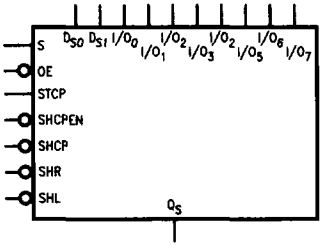
General Description

The 'F597 consists of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. The storage register and shift register have separate positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

Features

- High impedance NPN base inputs for reduced loading (20 μA in HIGH and LOW states)
- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Guaranteed shift frequency
- Separate clocks for storage and shift registers

Logic Symbols



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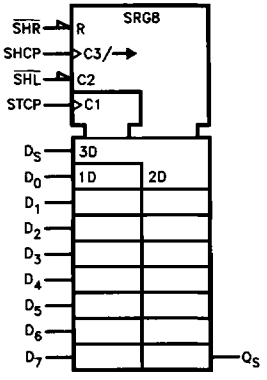
IEEE/IEC



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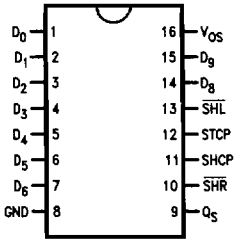
Connection Diagram

Pin Assignment for DIP, SOIC and Flatpak



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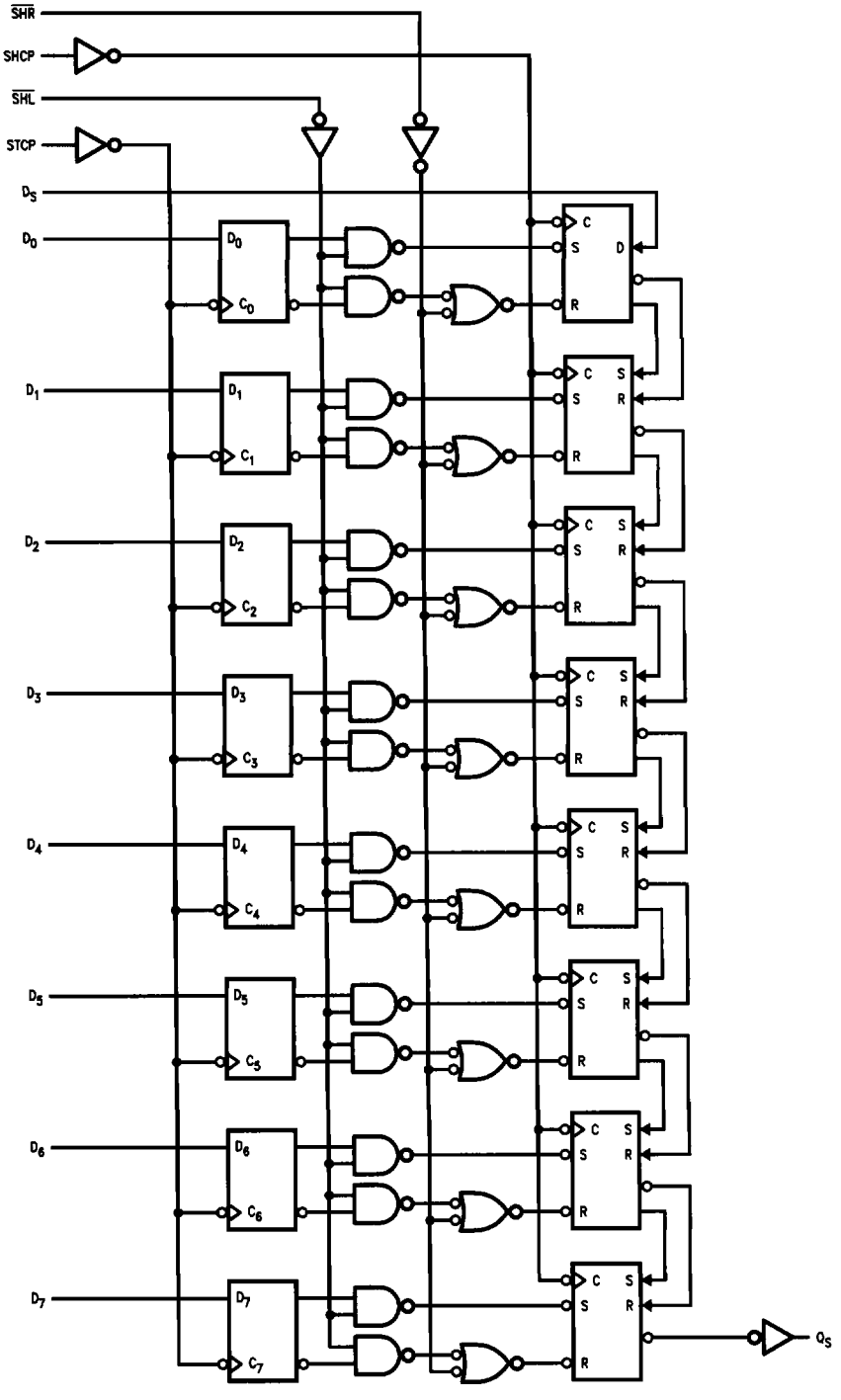
Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.