

# AN5819K

Sound multiplex demodulator IC for TV in the North American market

■ Overview

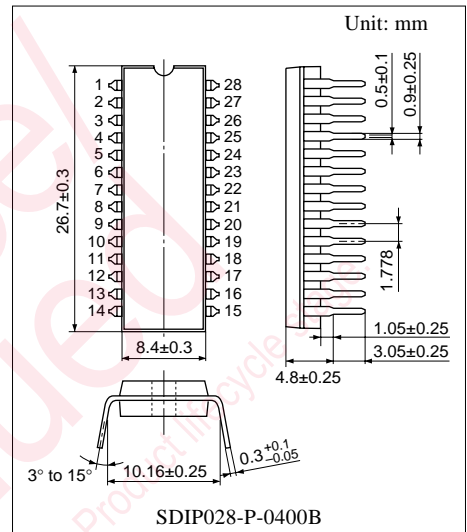
The AN5819K is a single chip IC, which includes a sound multiplex demodulator for Zenith TV system and the dbx TV sound noise reduction function.

■ Features

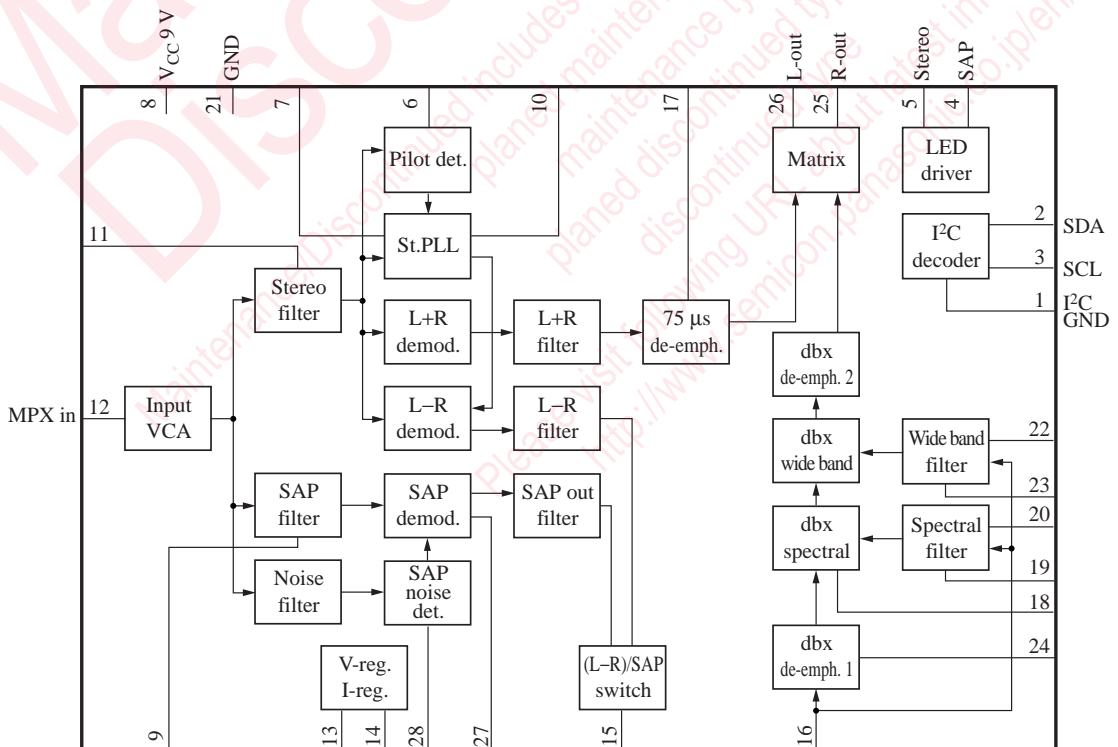
- Stereo demodulation, SAP demodulation and dbx noise reduction are integrated into a single chip
- Enabling various kinds of adjustment and mode changeover thanks to I<sup>2</sup>C bus
- Built-in input volume (I<sup>2</sup>C control) for interface with intermediate frequency processing IC

■ Applications

- TV and VCR for the North American market  
(A licensing agreement with THAT Corporation is necessary in order to use this IC with built-in dbx-TV noise reduction function.)



■ Block Diagram



### ■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	I <sup>2</sup> C GND	15	(L-R)/SAP demodulation output
2	SDA	16	dbx input
3	SCL	17	(L+R) demodulation output offset cancel
4	SAP LED	18	Spectral level adjustment
5	Stereo LED	19	Spectral timing
6	Pilot signal detection	20	Spectral level sensor input
7	Stereo PLL filter	21	GND
8	V <sub>CC</sub>	22	Wide band level sensor input
9	SAP trap filter	23	Wide band timing
10	Quasi sine-wave filter	24	dbx offset cancel
11	Stereo filter offset cancel	25	R output
12	Composite input	26	L output
13	dbx timing current	27	SAP carrier detection
14	Reference voltage source filter	28	SAP noise level detection

### ■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	11.0	V
Supply current	I <sub>CC</sub>	75	mA
LED drive current *3	I <sub>LED</sub>	10	mA
Power dissipation *2	P <sub>D</sub>	1 143	mW
Operating ambient temperature *1	T <sub>opr</sub>	-20 to +75	°C
Storage temperature *1	T <sub>stg</sub>	-55 to +150	°C

Note) \*1: Except for the operating ambient temperature and storage temperature, all ratings are for T<sub>a</sub> = 25°C.

\*2: Power dissipation shown is for the IC package in free air at T<sub>a</sub> = 70°C

\*3: LED drive currents are the currents flowing into pin 4 and pin 5.

### ■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V <sub>CC</sub>	8.5 to 9.5	V

■ Electrical Characteristics at  $V_{CC} = 9.0 \text{ V}$ ,  $T_a = 25^\circ\text{C}$

- Stereo PLL VCO adjustment:  $15.734 \text{ kHz} \pm 50 \text{ Hz}$
- Input level (at 100% modulation)
  - L+R:  $0.424 \text{ V[p-p]}$  (pre-emphasis off)
  - L-R:  $0.848 \text{ V[p-p]}$  (dbx noise reduction off)
  - Pilot:  $0.084 \text{ V[p-p]}$
  - SAP:  $0.254 \text{ V[p-p]}$  (dbx noise reduction off)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Total circuit current	$I_{CC}$	No signal	35	55	75	mA
Mono output level	$V_{0(MON)}$	$f = 1 \text{ kHz}$ , (mono) 100% mod.	480	530	580	mV[rms]
Mono frequency characteristics-1	$V_{1(MON)}$	$f = 300 \text{ Hz}$ , (mono) 30% mod.	-0.5	0	+0.5	dB
Mono frequency characteristics-2	$V_{2(MON)}$	$f = 8 \text{ kHz}$ , (mono) 30% mod.	-1.5	-0.4	+0.4	dB
Mono distortion ratio	$THD_{(MON)}$	$f = 1 \text{ kHz}$ , (mono) 100% mod.	—	—	0.7	%
Mono noise level	$V_{N(MON)}$	Input short-circuit, BPF (A curve)	—	—	-60	dBV
(L), (R) output voltage difference	$V_{LR(MON)}$	$f = 1 \text{ kHz}$ , (mono) 100% mod.	-0.5	0	+0.5	dB
Stereo output level	$V_{0(ST)}$	$f = 1 \text{ kHz}$ , (L(R)-only) 100% mod.	420	520	620	mV[rms]
Stereo frequency characteristics-1	$V_{1(ST)}$	$f = 300 \text{ Hz}$ , (L(R)-only) 30% mod.	-0.7	0	+0.7	dB
Stereo frequency characteristics-2	$V_{2(ST)}$	$f = 3 \text{ kHz}$ , (L(R)-only) 30% mod.	-1	0	+1	dB
Stereo frequency characteristics-3	$V_{3(ST)}$	$f = 8 \text{ kHz}$ , (L(R)-only) 30% mod.	-2.5	-0.5	+1.5	dB
Stereo distortion ratio	$THD_{(ST)}$	$f = 1 \text{ kHz}$ , (L(R)-only) 100% mod.	—	—	1	%
Stereo noise level	$V_{N(ST)}$	$f = 15.73 \text{ kHz}$ , ( $f_H$ ), $V = 0.084 \text{ V[p-p]}$ , BPF	—	—	-60	dBV
Stereo discrimination level	$V_{TH(ST)}$	$f = 15.73 \text{ kHz}$ ( $f_H$ )	9	17	26	mV[rms]
Stereo discrimination hysteresis	$V_{HY(ST)}$	$f = 15.73 \text{ kHz}$ ( $f_H$ )	-6	—	-0.5	dB
SAP output level	$V_{0(SAP)}$	$f = 1 \text{ kHz}$ , (SAP) 100% mod.	350	500	700	mV[rms]
SAP frequency characteristics-1	$V_{1(SAP)}$	$f = 300 \text{ Hz}$ , (SAP) 30% mod.	-1.0	0	+1.0	dB
SAP frequency characteristics-2	$V_{2(SAP)}$	$f = 3 \text{ kHz}$ , (SAP) 30% mod.	-3	-1.5	+0.5	dB
SAP distortion ratio	$THD_{(SAP)}$	$f = 1 \text{ kHz}$ , (SAP) 100%	—	—	1.5	%
SAP noise level	$V_{N(SAP)}$	$f = 78.7 \text{ kHz}$ , ( $5f_H$ ), $V = 0.42 \text{ V[p-p]}$ , BPF	—	—	-65	dBV
SAP discrimination level	$V_{TH(SAP)}$	$f = 78.7 \text{ kHz}$ , ( $5f_H$ )	22	—	53	mV[rms]
SAP discrimination hysteresis	$V_{HY(SAP)}$	$f = 78.7 \text{ kHz}$ , ( $5f_H$ )	-4	—	-0.5	dB
SAP → Stereo crosstalk	$CT_1$	(SAP) 1 kHz, 100% mod. (Stereo) pilot-signal	—	—	-50	dB
Stereo → SAP crosstalk	$CT_2$	(Stereo) 1 kHz, 100% mod. (SAP) carrier-signal	—	—	-50	dB
Noise discrimination level	$V_{TH(NOI)}$	Pin 27: $f = 240 \text{ kHz}$ at 5 V applied	38	—	84	mV[rms]
Noise discrimination hysteresis	$V_{HY(NOI)}$	Pin 27: $f = 240 \text{ kHz}$ at 5 V applied	-5.5	—	-0.3	dB

**■ Electrical Characteristics at  $V_{CC} = 9.0\text{ V}$ ,  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>I<sup>2</sup>C interface</b>						
Sink current at ACK	$I_{ACK}$	Maximum pin-2 sink current at ACK	2.0	10	20	mA
SCL, SDA signal input high level	$V_{IHI}$	—	3.5	—	5.0	V
SCL, SDA signal input low level	$V_{ILO}$	—	0	—	0.9	V
Input available maximum frequency	$f_{IMAX}$	—	—	—	100	kbit/s

**• Design reference data**

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Stereo separation (30%)-1	Sep <sub>30-1</sub>	f = 300 Hz, (L(R)-only) 30%mod.	22	30	—	dB
Stereo separation (30%)-2	Sep <sub>30-2</sub>	f = 1 kHz, (L(R)-only) 30%mod.	22	30	—	dB
Stereo separation (30%)-3	Sep <sub>30-3</sub>	f = 3 kHz, (L(R)-only) 30%mod.	22	30	—	dB
Stereo separation (30%)-4	Sep <sub>30-4</sub>	f = 8 kHz, (L(R)-only) 30%mod.	12	18	—	dB
Stereo separation (100%)-1	Sep <sub>100-1</sub>	f = 300 Hz, (L(R)-only) 100%mod.	20	30	—	dB
Stereo separation (100%)-2	Sep <sub>100-2</sub>	f = 1 kHz, (L(R)-only) 100%mod.	20	25	—	dB
Stereo separation (100%)-3	Sep <sub>100-3</sub>	f = 3 kHz, (L(R)-only) 100%mod.	20	30	—	dB
Stereo separation (100%)-4	Sep <sub>100-4</sub>	f = 8 kHz, (L(R)-only) 100%mod.	8	11	—	dB
Stereo separation (10%)-1	Sep <sub>10-1</sub>	f = 300 Hz, (L(R)-only) 10%mod.	20	30	—	dB
Stereo separation (10%)-2	Sep <sub>10-2</sub>	f = 1 kHz, (L(R)-only) 10%mod.	20	30	—	dB
Stereo separation (10%)-3	Sep <sub>10-3</sub>	f = 3 kHz, (L(R)-only) 10%mod.	20	30	—	dB
Stereo separation (10%)-4	Sep <sub>10-4</sub>	f = 8 kHz, (L(R)-only) 10%mod.	12	18	—	dB
SAP → Mono crosstalk	CT <sub>3</sub>	(SAP) 1 kHz, 100% mod. (Mono) 1 kHz, 0% mod.	—	—	-53	dB
Mono → SAP crosstalk	CT <sub>4</sub>	(SAP) 1 kHz, 0% mod. (Mono) 1 kHz, 100% mod.	—	—	-56	dB

**I<sup>2</sup>C interface**

Bus free before start	$t_{BUF}$	—	4.0	—	—	μs
Start condition set-up time	$t_{SU,STA}$	—	4.0	—	—	μs
Start condition hold time	$t_{HD,STA}$	—	4.0	—	—	μs
Low period SCL, SDA	$t_{LO}$	—	4.0	—	—	μs
High period SCL	$t_{HI}$	—	4.0	—	—	μs
Rise time SCL, SDA	$t_r$	—	—	—	1.0	μs
Fall time SCL, SDA	$t_f$	—	—	—	0.35	μs
Data set-up time (write)	$t_{SU,DAT}$	—	0.25	—	—	μs
Data hold time (write)	$t_{HD,DAT}$	—	0	—	—	μs

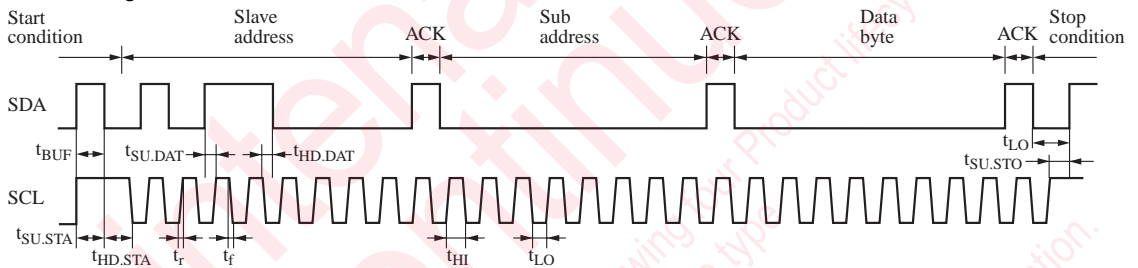
■ Electrical Characteristics at  $V_{CC} = 9.0\text{ V}$ ,  $T_a = 25^\circ\text{C}$  (continued)

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I <sup>2</sup> C interface (continued)						
Acknowledge set-up time	$t_{SU,ACK}$	—	—	—	3.5	$\mu\text{s}$
Acknowledge hold time	$t_{HD,ACK}$	—	0	—	—	$\mu\text{s}$
Stop condition set-up time	$t_{SU,STO}$	—	4.0	—	—	$\mu\text{s}$
DAC						
6-bit DAC DNLE	$L_6$	$1\text{LSB} = (\text{data (max.)} - \text{data (00)})/63$	0.1	1.0	1.9	$\frac{\text{LSB}}{\text{Step}}$

• DAC timing chart



■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	Voltage (V)
1	—	I <sup>2</sup> C GND: • I <sup>2</sup> C bus DAC GND pin	0
2		SDA: • I <sup>2</sup> C bus data input pin	—
3		SCL: • I <sup>2</sup> C bus clock input pin	—

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
4		<p>SAP LED:</p> <ul style="list-style-type: none"> <li>• SAP LED connection pin</li> </ul>	—
5		<p>Stereo LED:</p> <ul style="list-style-type: none"> <li>• Stereo LED connection pin</li> </ul>	—
6		<p>Pilot signal detection:</p> <ul style="list-style-type: none"> <li>• Stereo pilot signal detection pin</li> </ul>	$\frac{V_{CC}}{2}$
7		<p>Stereo PLL filter:</p> <ul style="list-style-type: none"> <li>• Stereo PLL low-pass filter connection pin</li> </ul>	2.8
8	—	<p><math>V_{CC}</math>:</p> <ul style="list-style-type: none"> <li>• <math>V_{CC}</math> pin</li> </ul>	$V_{CC}$
9		<p>SAP trap filter:</p> <ul style="list-style-type: none"> <li>• SAP trap filter</li> </ul>	$\frac{V_{CC}}{2}$

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
10		<p>Quasi sine-wave filter:</p> <ul style="list-style-type: none"> <li>• Low-pass filter pin in quasi-sine wave circuit</li> </ul>	$\frac{V_{CC}}{2}$
11		<p>Stereo filter offset cancel:</p> <ul style="list-style-type: none"> <li>• Offset cancel pin for stereo filter output</li> </ul>	$\frac{V_{CC}}{2}$
12		<p>Composite input:</p> <ul style="list-style-type: none"> <li>• Composite signal input pin</li> </ul>	$\frac{V_{CC}}{2}$
13		<p>dbx timing current:</p> <ul style="list-style-type: none"> <li>• Timing current setting pin for dbx RMS detection</li> </ul>	1.3
14		<p>Reference:</p> <ul style="list-style-type: none"> <li>• Reference power supply stabilization pin</li> </ul>	$\frac{V_{CC}}{2}$

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
15		(L-R)/SAP demodulation output: • (L-R)/SAP demodulation signal output pin	$\frac{V_{CC}}{2} - 0.7$
16		dbx input: • Input signal of (L-R)/SAP signal to dbx NR	$\frac{V_{CC}}{2}$
17		(L+R) demodulation output offset cancel: • (L+R) demodulation signal offset cancel pin	$\frac{V_{CC}}{2}$
18		Spectral level adjustment: • Variable emphasis level adjustment pin	$\frac{V_{CC}}{2}$
19		Spectral timing: • RMS detection recovery time setting pin for variable emphasis	0.2

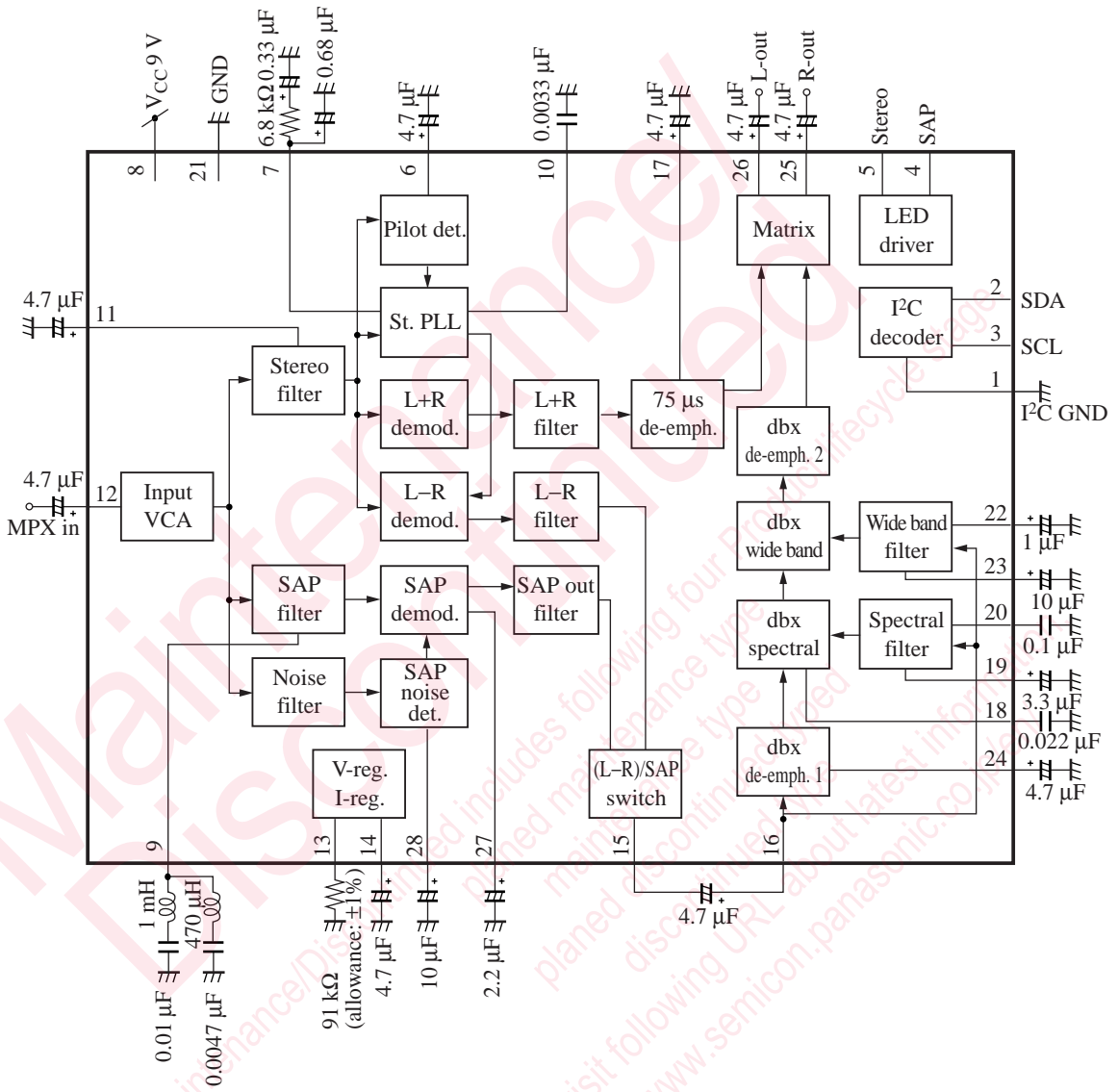
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
20		Spectral level sensor input: • RMS detection circuit input pin for variable emphasis	$\frac{V_{CC}}{2}$
21	—	GND: • GND pin	0
22		Wideband level sensor input: • RMS detection circuit input pin for wide band expander	$\frac{V_{CC}}{2}$
23		Wideband timing: • RMS detection recovery time setting pin for wide band expander	0.2
24		dbx offset cancel: • dbx NR output offset cancel pin	$\frac{V_{CC}}{2}$
25		R output: • R line-out output pin	$\frac{V_{CC}}{2}$

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)						
26		L output: • L line-out output pin	$\frac{V_{CC}}{2}$						
27		SAP carrier detection: • SAP signal carrier level detection pin	$\frac{V_{CC}}{2}$						
28	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>SW</th> </tr> </thead> <tbody> <tr> <td><math>V_{28} &gt; V_{27}</math></td> <td>a</td> </tr> <tr> <td><math>V_{28} &lt; V_{27}</math></td> <td>b</td> </tr> </tbody> </table>		SW	$V_{28} > V_{27}$	a	$V_{28} < V_{27}$	b	SAP noise level setting: • Noise detection pin for SAP malfunction prevention circuit (Mute SAP demodulation at detecting noise)	$\frac{V_{CC}}{2}$
	SW								
$V_{28} > V_{27}$	a								
$V_{28} < V_{27}$	b								

■ Application Circuit Example



## Request for your special attention and precautions in using the technical information and semiconductors described in this book

- (1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.
- (2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products, and no license is granted under any intellectual property right or other right owned by our company or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.
- (3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).  
Consult our sales staff in advance for information on the following applications:
  - Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
  - Any applications other than the standard applications intended.
- (4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.
- (5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
  - Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
- (6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.
- (7) This book may be not reprinted or reproduced whether wholly or partially, without the prior written permission of Matsushita Electric Industrial Co., Ltd.