T-46-23-17

November 1990
Edition 3.0

FUJITSU

DATA SHEET

MB81C4256A-60/-70/-80/-10

CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 256 x 4 Bits Fast Page Mode DRAM

The Fujitsu MB81C4256A is a CMOS, fully decoded dynamic RAM organized as 262,144 words x 4 bits. The MB81C4256A has been designed for mainframe memories, buffer memories, and video image memories requiring high speed and high bandwidth output with low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C4256A high α-ray soft error immunity. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

This specification applies to the BC die revision that was developed to realize faster access time. Faster speed versions (70 and 80 ns) are available on this chip.

Features

Parameter	MB81C4256A -60	MB81C4256A -70	MB81C4256A -80	MB81C4256A -10
$\overline{RAS}$ Access Time	60 ns max.	70 ns max.	80 ns max.	100 ns max.
Random Cycle Time	130 ns min.	140 ns min.	155 ns min.	180 ns min.
Address Access Time	30 ns max.	35 ns max.	40 ns max.	50 ns max.
$\overline{CAS}$ Access Time	15 ns max.	20 ns max.	20 ns max.	25 ns max.
Fast Page Mode Cycle Time	45 ns min.	50 ns min.	55 ns min.	65 ns min.
Low Power Dissipation • Operating Current	407 mW max.	374 mW max.	341 mW max.	297 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)			

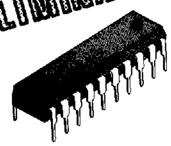
- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

Absolute Maximum Ratings (See Note)

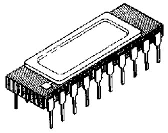
Parameter		Symbol	Value	Unit
Voltage at any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY



DIP-20P-M03



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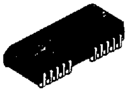
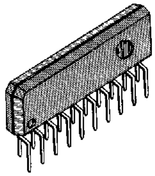


LCC-26P-M04



ZIP-20P-M02

* FPT-24P-M04 /*FPT-24P-M05
*. Available for 70/80/100ns versions

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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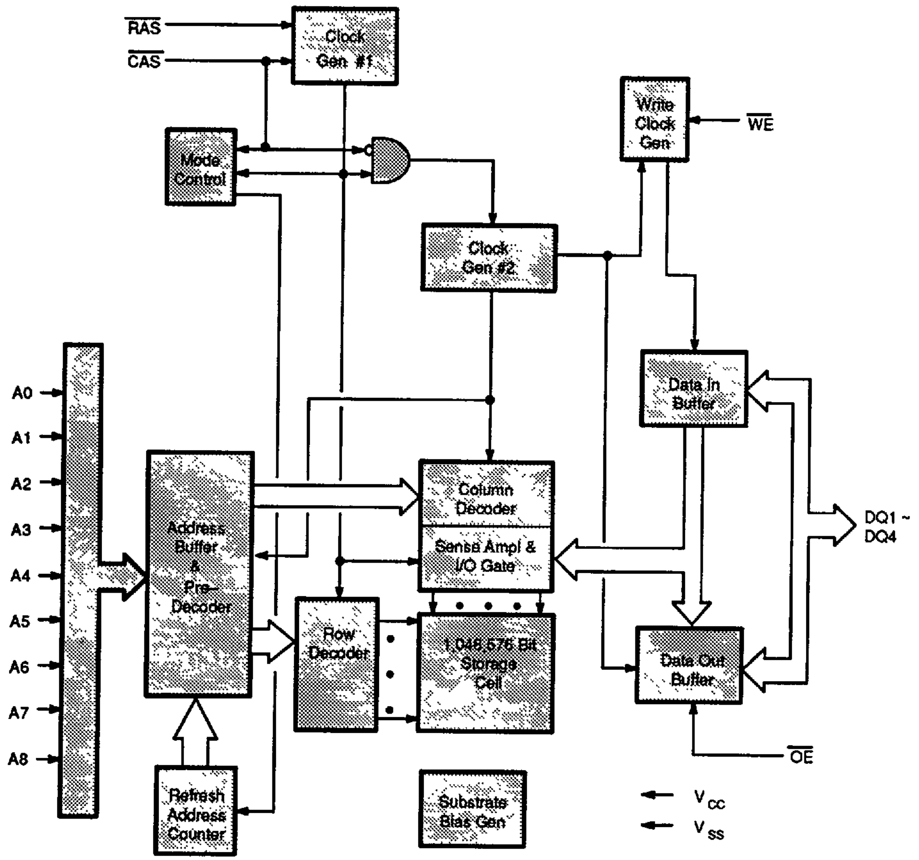
Fig. 1 – MB81C4256A DYNAMIC RAM – BLOCK DIAGRAM

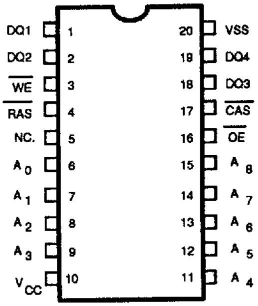


CAPACITANCE ($T_A = 25°C$, f = 1MHz)

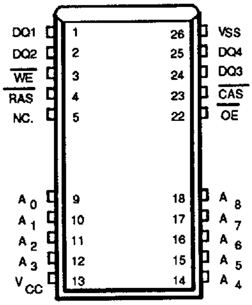
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

20–Pin DIP :
(TOP VIEW)

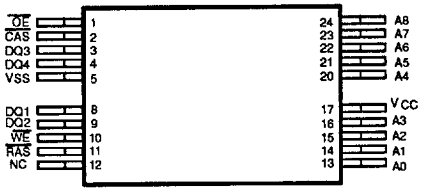


26–Pin SOJ:
(TOP VIEW)



24–Pin FPT :
(TOP VIEW)

<Normal Bend : FPT–24P–M04>



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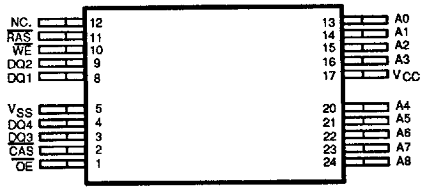
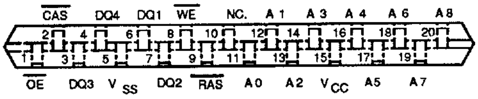


Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{\text{WE}}$	Write Enable.
$\overline{\text{RAS}}$	Row address strobe.
NC	No connection
A0 to A8	Address inputs.
VCC	+5 volt power supply.
$\overline{\text{OE}}$	Output enable.
$\overline{\text{CAS}}$	Column address strobe
VSS	Circuit ground.

20–Pin ZIP:
(TOP VIEW)



RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	–1.0	—	0.8	V	

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 celladdresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A8 and latched with the row address strobe ($\overline{\text{RAS}}$) then, nine column address bits are input and latched with the column address strobe ($\overline{\text{CAS}}$). Both row and column addresses must be stable on or before the fallingedge of $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{\text{WE}}$. When $\overline{\text{WE}}$ is active Low, a write cycle is initiated; when $\overline{\text{WE}}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{\text{OE}}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{\text{CAS}}$ and the setup/hold times are referenced to $\overline{\text{CAS}}$ because $\overline{\text{WE}}$ goes Low before $\overline{\text{CAS}}$. In a delayed write or a read–modify–write cycle, $\overline{\text{WE}}$ goes Low after $\overline{\text{CAS}}$; thus, input data is strobed by $\overline{\text{WE}}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{\text{RAS}}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{\text{CAS}}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

tOEA : from the falling edge of $\overline{\text{OE}}$ when $\overline{\text{OE}}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}

The data remains valid until either $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter		Notes	Symbol	Conditions	Values			Unit
					Min	Typ	Max	
Output high voltage			V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output low voltage			V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	
Input leakage current (any input)			$I_{I(L)}$	0V≤V_{IN}≤5.5V; 4.5V≤V_{CC}≤5.5V; V_{SS} = 0V; All other pins under test = 0V	–10	—	10	µA
Output leakage current			$I_{O(L)}$	0V≤V_{OUT}≤5.5V; Data out disabled	–10	—	10	
Operating current (Average Power supply Current)	MB81C4256A–60	2	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	74	mA
	MB81C4256A–70						68	
	MB81C4256A–80						62	
	MB81C4256A–10						54	
Standby current (Power supply current)	TTL level		I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level			$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2V			1.0	
Refresh current #1 (Average power supply current)	MB81C4256A–60	2	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	74	mA
	MB81C4256A–70						68	
	MB81C4256A–80						62	
	MB81C4256A–10						54	
Fast Page Mode current	MB81C4256A–60	2	I_{CC4}	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	60	mA
	MB81C4256A–70						55	
	MB81C4256A–80						50	
	MB81C4256A–10						43	
Refresh current #2 (Average power supply current)	MB81C4256A–60	2	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	74	mA
	MB81C4256A–70						68	
	MB81C4256A–80						62	
	MB81C4256A–10						54	

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AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256A-60 Min	MB81C4256A-60 Max	MB81C4256A-70 Min	MB81C4256A-70 Max	MB81C4256A-80 Min	MB81C4256A-80 Max	MB81C4256A-10 Min	MB81C4256A-10 Max	Unit
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	130	—	140	—	155	—	180	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	170	—	180	—	205	—	240	—	ns
4	Access Time from $\overline{\text{RAS}}$	6,9	t_{RAC}	—	60	—	70	—	80	—	100	ns
5	Access Time from $\overline{\text{CAS}}$	7,9	t_{CAC}	—	15	—	20	—	20	—	25	ns
6	Column Address Access Time	8,9	t_{AA}	—	30	—	35	—	40	—	50	ns
7	Output Hold Time		t_{OH}	0	—	0	—	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	15	—	20	—	25	ns
10	Transition Time		t_{T}	2	50	2	50	2	50	2	50	ns
11	$\overline{\text{RAS}}$ Precharge Time		t_{RP}	60	—	60	—	65	—	70	—	ns
12	$\overline{\text{RAS}}$ Pulse Width		t_{RAS}	60	100000	70	100000	80	100000	100	100000	ns
13	$\overline{\text{RAS}}$ Hold Time		t_{RSH}	15	—	20	—	20	—	25	—	ns
14	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	11,12	t_{RCD}	20	45	20	50	22	60	25	75	ns
16	$\overline{\text{CAS}}$ Pulse Width		t_{CAS}	15	—	20	—	20	—	25	—	ns
17	$\overline{\text{CAS}}$ Hold Time		t_{CSH}	60	—	70	—	80	—	100	—	ns
18	$\overline{\text{CAS}}$ Precharge Time (C–B–R cycle)	19	t_{CPN}	20	—	20	—	20	—	20	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	12	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	12	—	15	—	15	—	ns
23	$\overline{\text{RAS}}$ to Column Address Delay Time	13	t_{RAD}	15	30	15	35	17	40	20	50	ns
24	Column Address to $\overline{\text{RAS}}$ Lead Time		t_{RAL}	30	—	35	—	40	—	50	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	10	—	10	—	12	—	15	—	ns
30	$\overline{\text{WE}}$ Pulse Width		t_{WP}	10	—	10	—	12	—	15	—	ns
31	Write Command to $\overline{\text{RAS}}$ Lead Time		t_{RWL}	15	—	15	—	20	—	25	—	ns
32	Write Command to $\overline{\text{CAS}}$ Lead Time		t_{CWL}	12	—	12	—	15	—	20	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	10	—	10	—	12	—	15	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256A-60		MB81C4256A-70		MB81C4256A-80		MB81C4256A-10		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before–$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before–$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	12	—	15	—	ns
38	Access Time from $\overline{OE}$	9	t_{OEA}	—	15	—	20	—	20	—	25	ns
39	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	15	—	15	—	20	—	25	ns
40	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	10	—	ns
41	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	0	—	0	—	0	—	0	—	ns
42	$\overline{OE}$ to Data In Delay Time		t_{OED}	15	—	15	—	20	—	25	—	ns
43	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	0	—	0	—	ns
44	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	0	—	0	—	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	45	—	50	—	55	—	65	—	ns
51	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	82	—	87	—	100	—	120	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,18	t_{CPA}	—	40	—	45	—	50	—	60	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	10	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ =VIH) of 200µs is required after power–up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max). If $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA} .
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min)
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min)
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is shortened, t_{CPA} is longer than t_{CPA} (max).
19. Assumes that $\overline{CAS}$ -before-$\overline{RAS}$ refresh, $\overline{CAS}$ -before-$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

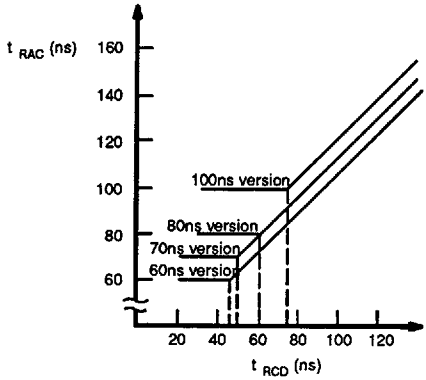
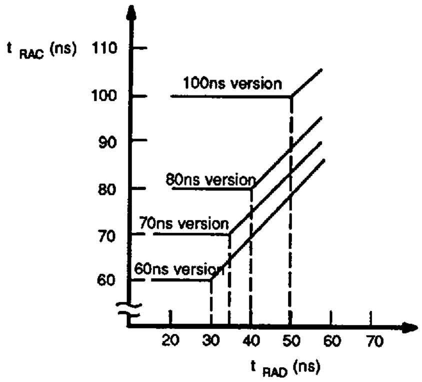


Fig. 3 – t_{RAC} vs. t_{RAD}

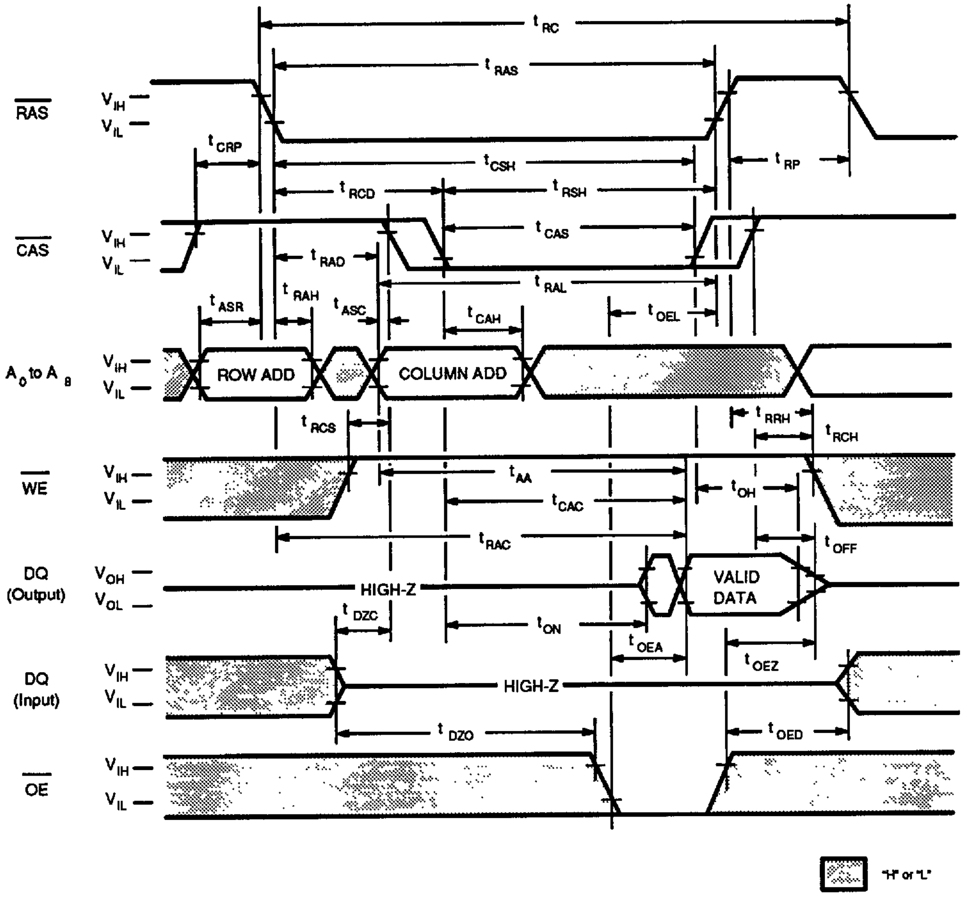


FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High–Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High–Z	Yes *	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes *	
$\overline{RAS}$–only Refresh Cycle	L	H	X	X	Valid	—	—	High–Z	Yes	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High–Z	Yes	$t_{CSR} \geq t_{WCSR}$ (min)
Hidden Refresh	H→L	L	X	L	—	—	—	Valid	Yes	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

Fig. 4 – READ CYCLE



DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ address strobes and with $\overline{\text{WE}}$ set to a High level and $\overline{\text{OE}}$ set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{\text{RAS}}$(tRAC), $\overline{\text{CAS}}$(tCAC), $\overline{\text{OE}}$ (tOEA) or column addresses (tAA) under the following conditions:

If tRCD > tRCD (max), access time = tCAC.
If tRAD > tRAD (max), access time = tAA.
If $\overline{\text{OE}}$ is brought Low after tRAC, tCAC, or tAA (which ever occurs later), access time = tOEA.

However, if either $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ goes High, the output returns to a high-impedance state after tOH is satisfied.

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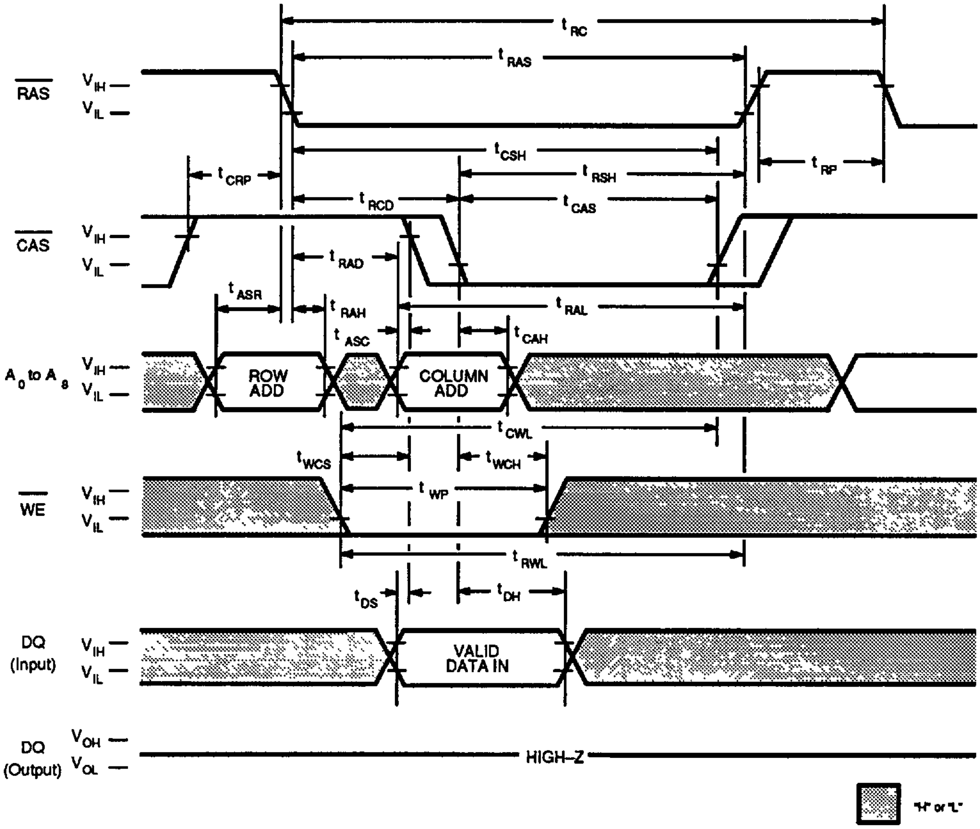
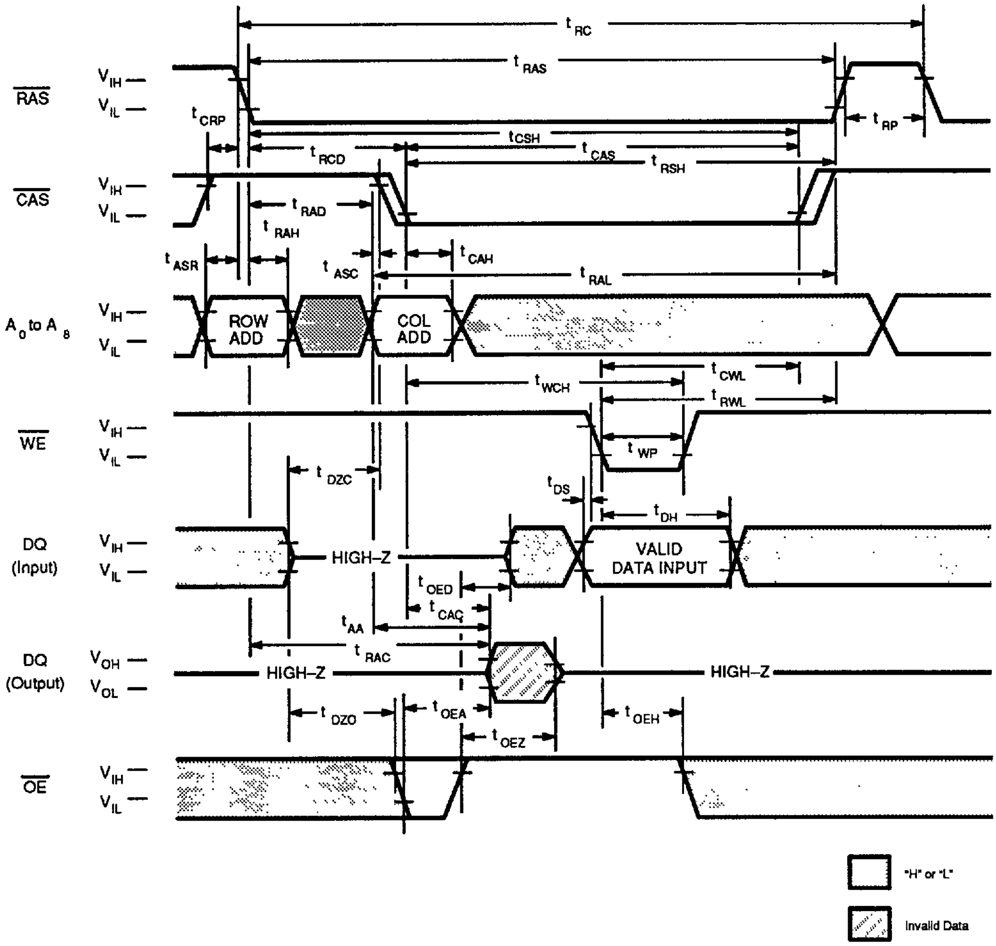
Fig. 5 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, $\overline{OE}$ write (delayed write), or read–modify–write. During all write cycles, timing parameters tRWL, tCWL and tRAL must be satisfied. In the early write cycle shown above tWCS satisfied, data on the DQ pin is latched with the falling edge of $\overline{CAS}$ and written into memory.

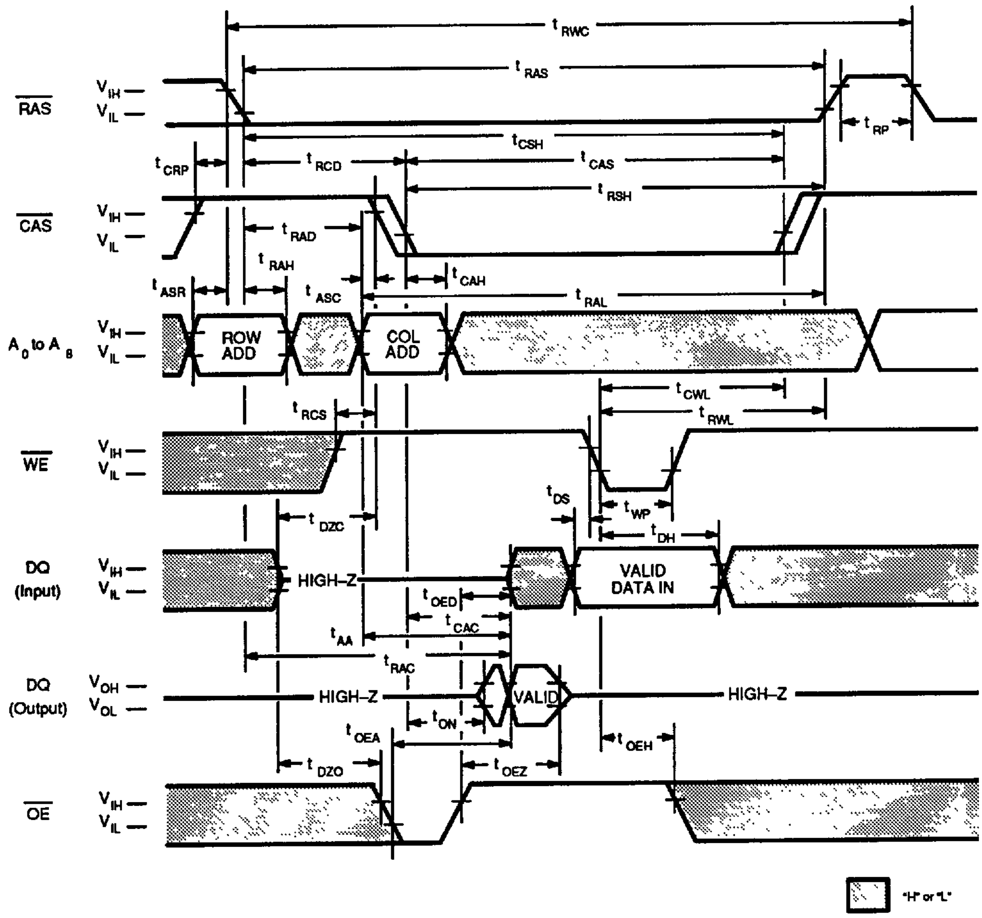
Fig. 6 – $\overline{\text{OE}}$ (DELAYED WRITE CYCLE)



DESCRIPTION

In the $\overline{\text{OE}}$ (delayed write) cycle, tWCS is not satisfied ; thus, the data on the DQpins is latched with the falling edge of $\overline{\text{WE}}$ and written into memory. The Output Enable ($\overline{\text{OE}}$) signal must be changed from Low to High before $\overline{\text{WE}}$ goes Low (tOED + tDS).

Fig. 7 – READ–MODIFY–WRITE CYCLE



DESCRIPTION

The read–modify–write cycle is executed by changing $\overline{\text{WE}}$ from High to Low after the data appears on the DQ pins. In the read–modify–write cycle, $\overline{\text{OE}}$ must be changed from Low to High after the memory access time.

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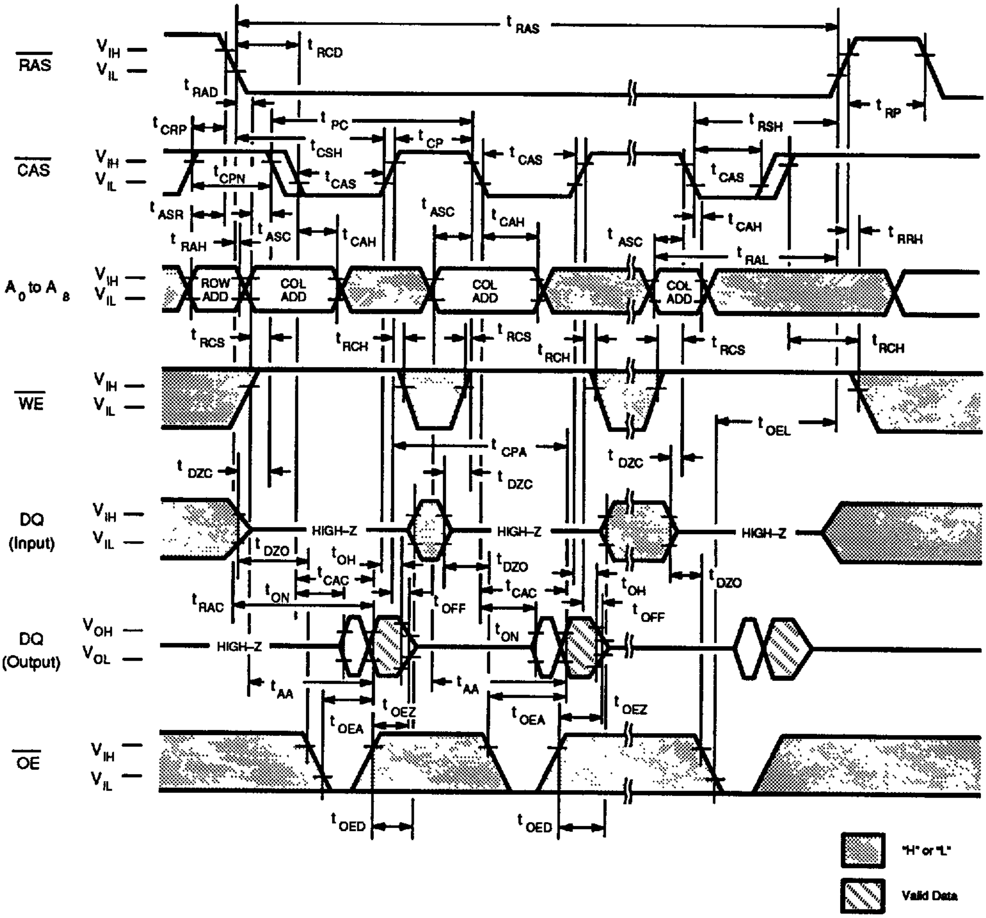
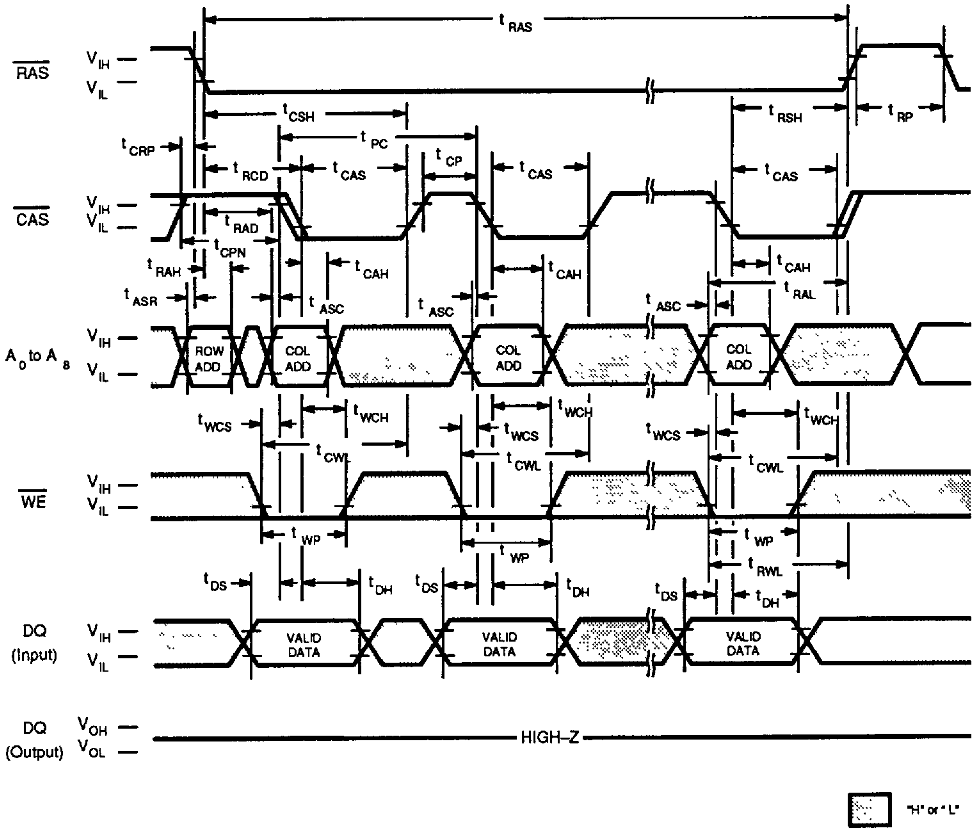
Fig. 8 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by tCAC, tAA, tCPA, or tOEA, whichever one is the latest in occuring.

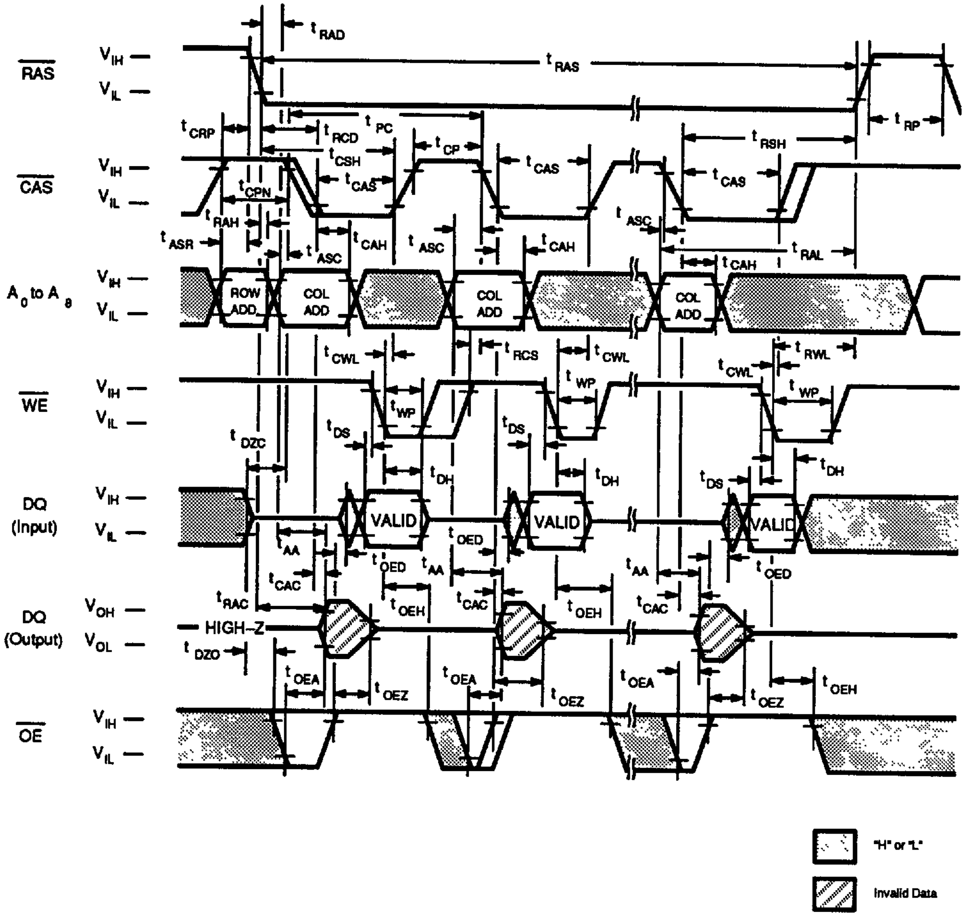
Fig. 9 – FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fastpage mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read–modify–write cycles, tCWL must be satisfied.

Fig. 10 – FAST PAGE MODE $\overline{\text{OE}}$ WRITE CYCLE



DESCRIPTION

The fast page mode $\overline{\text{OE}}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{\text{WE}}$ and $\overline{\text{OE}}$. Input data on the DQ pins are latched on the falling edge of $\overline{\text{WE}}$ and written into memory. In the fast page mode delayed write cycle, $\overline{\text{OE}}$ must be changed from Low to High before $\overline{\text{WE}}$ goes Low (tOED + tDS).

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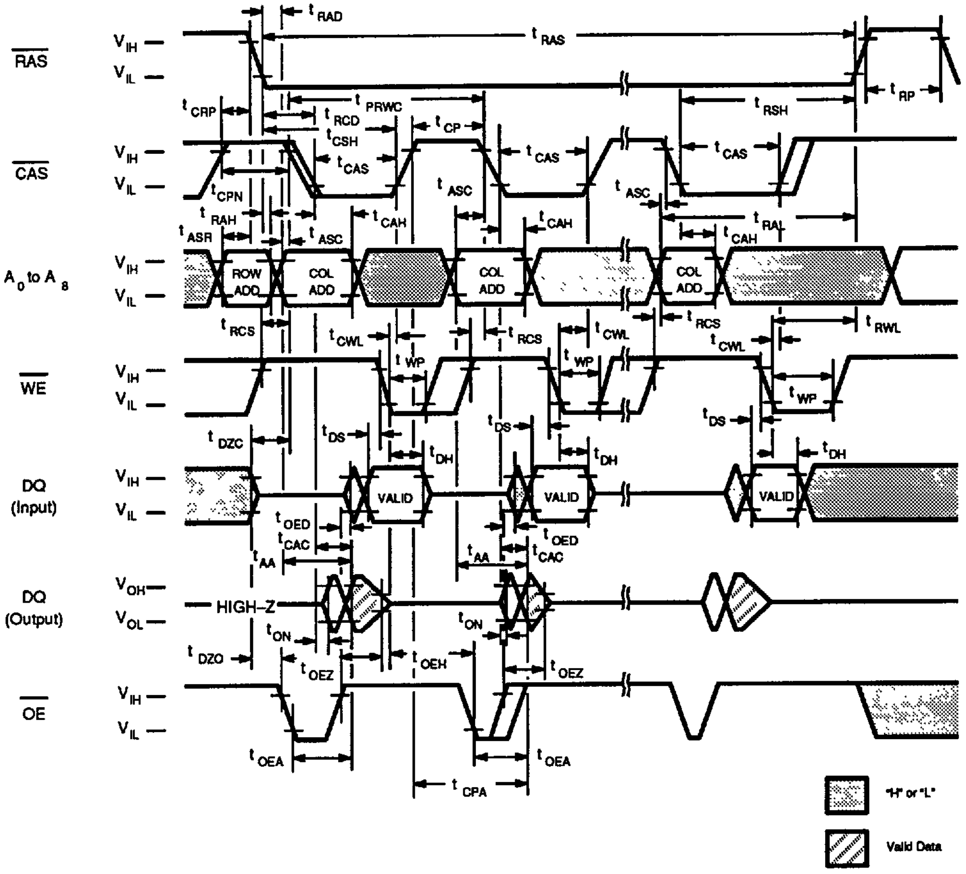
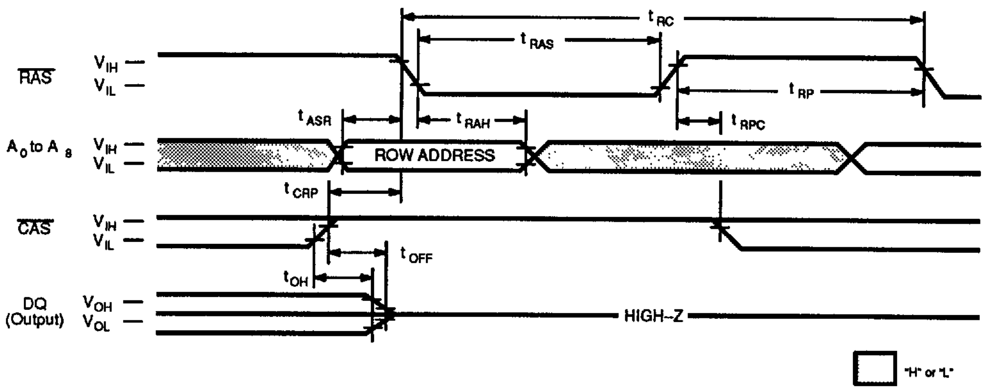
Fig. 11 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read–modify–write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

Fig. 12 – $\overline{\text{RAS}}$–ONLY REFRESH ($\overline{\text{WE}}$ = $\overline{\text{OE}}$ = "H" or "L")

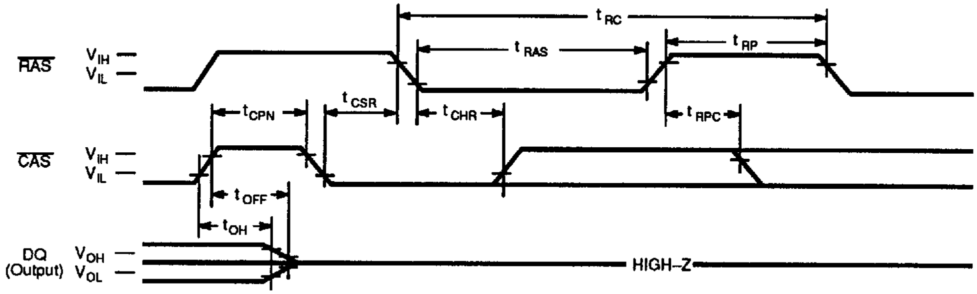


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{\text{RAS}}$–only refresh, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, and hidden refresh.

$\overline{\text{RAS}}$–only refresh is performed by keeping $\overline{\text{RAS}}$ Low and $\overline{\text{CAS}}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{\text{RAS}}$. During $\overline{\text{RAS}}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 13 – $\overline{\text{CAS}}$–BEFORE–$\overline{\text{RAS}}$ REFRESH (ADDRESSES = $\overline{\text{WE}}$ = $\overline{\text{OE}}$ = "H" or "L")



DESCRIPTION

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CAS}}$ is held Low for the specified setup time (tCSR) before $\overline{\text{RAS}}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operation.

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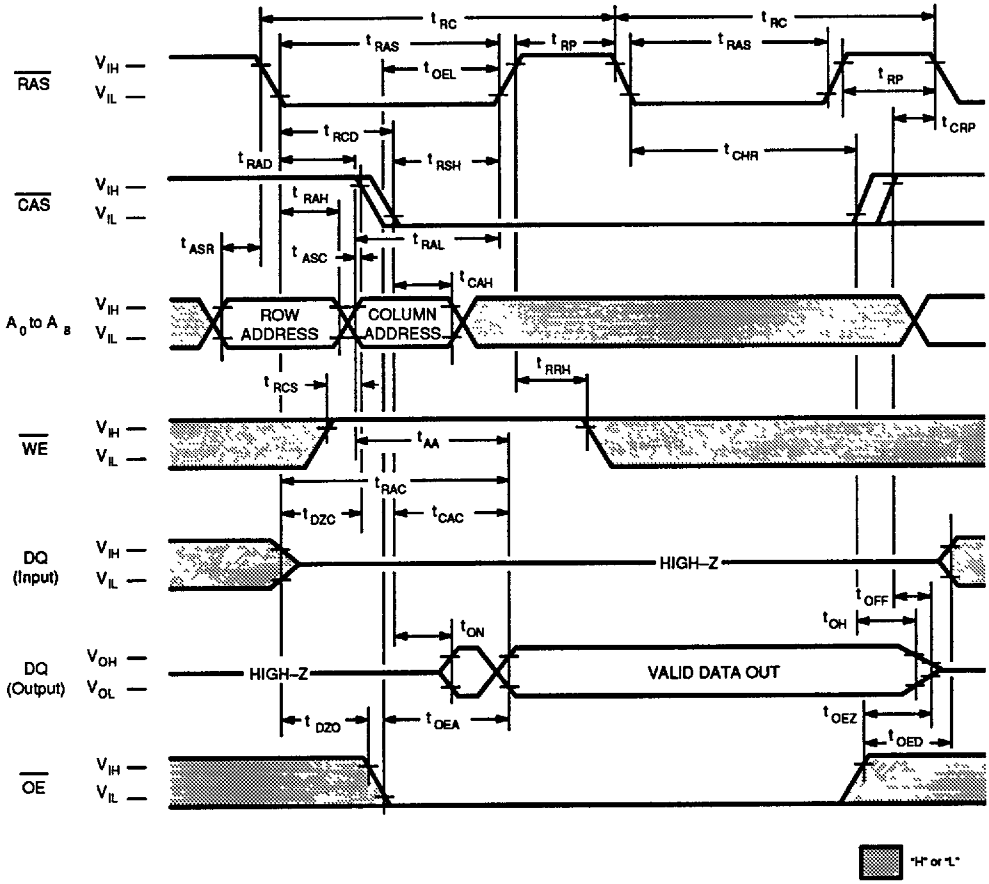
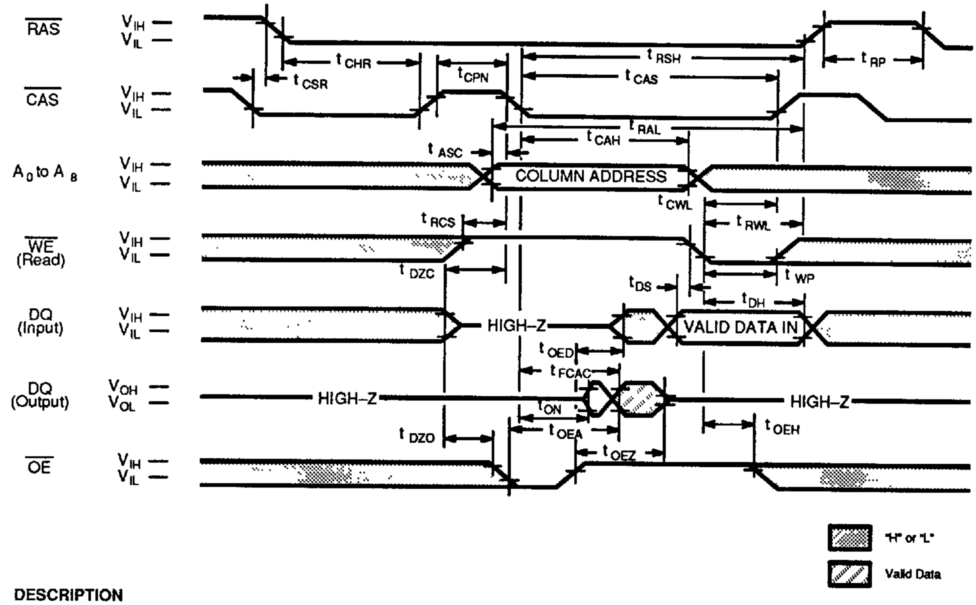
Fig. 14 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{\text{CAS}}$ and cycling $\overline{\text{RAS}}$. The refresh row address is provided by the on-chip refresh addresscounter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability.

Fig. 15 – $\overline{\text{CAS}}$–BEFORE–$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh circuitry. If, after a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle $\overline{\text{CAS}}$ makes a transition from High to Low while $\overline{\text{RAS}}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of $\overline{\text{CAS}}$.

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 512 row addresses (DQ1 to DQ4) at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check, simultaneously write "1" to the same addresses by using $\overline{\text{CAS}}$–before–$\overline{\text{RAS}}$ refresh counter test (read–modify–write cycles). Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 512 (DQ1 to DQ4) memory locations.
6) Complement test pattern and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81C4256A-60		MB81C4256A-70		MB81C4256A-80		MB81C4256A-10		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{\text{CAS}}$	t_{FCAC}	—	40	—	45	—	50	—	60	ns

Note . Assumes that $\overline{\text{CAS}}$–before–$\overline{\text{RAS}}$ refresh counter test cycle only.

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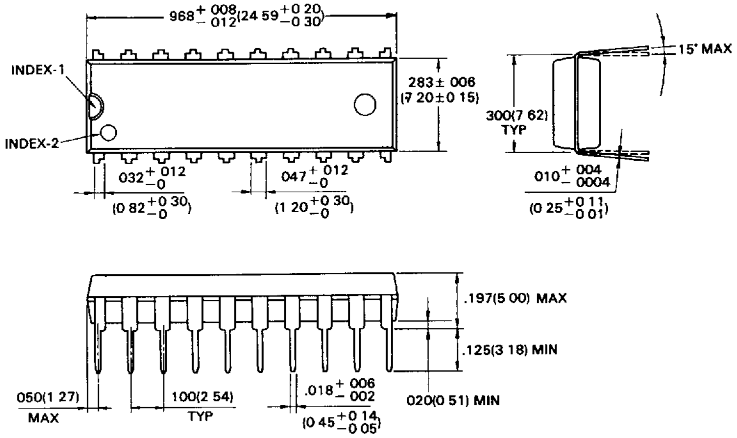
PACKAGE DIMENSIONS

(Suffix : -P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M03)

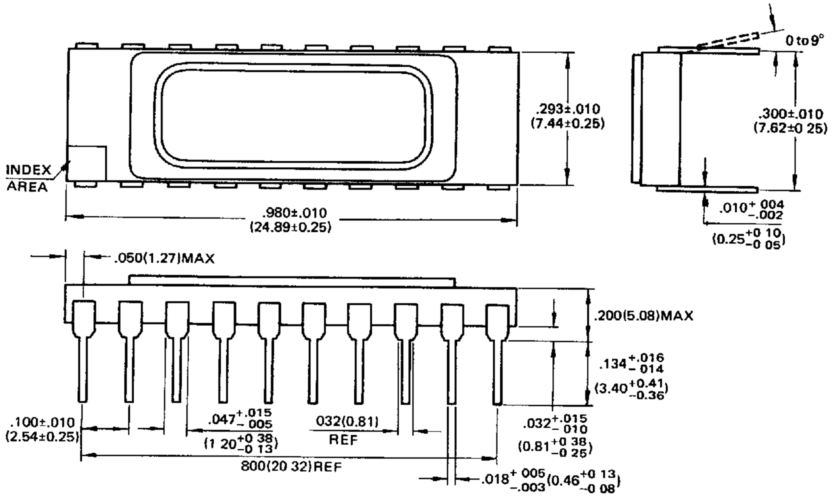


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –C)

20–LEAD CERAMIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20C–A03)

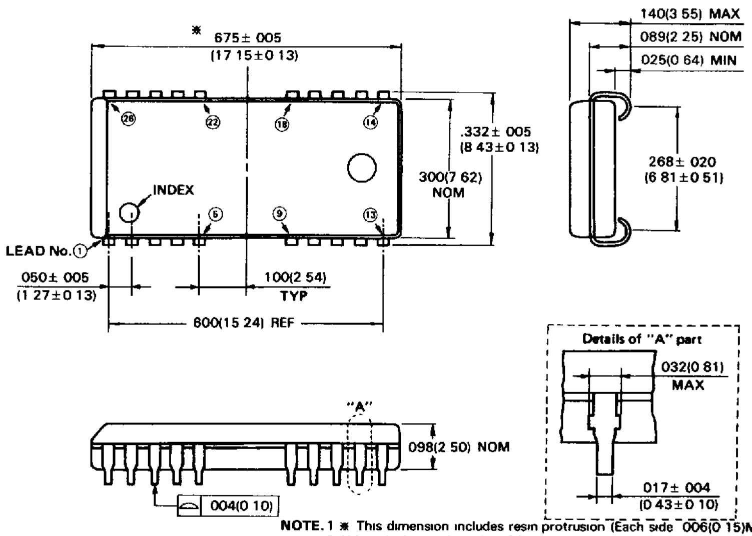


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26–LEAD PLASTIC LEADED CHIP CARRIER (SOJ–26)
(CASE No.: LCC–26P–M04)

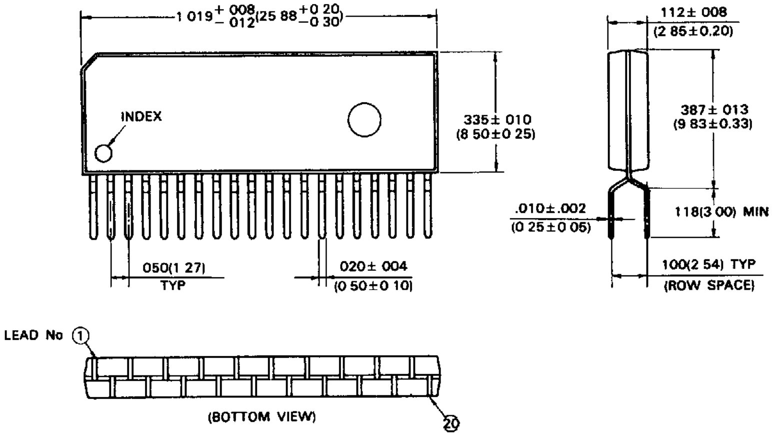


NOTE. 1 ✱ This dimension includes resin protrusion (Each side 006(0 15)MAX)
2 Although this package has 20 leads only, its pin positions are the same as that that of 26-lead package
3 Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20–LEAD PLASTIC ZIG–ZAG IN–LINE PACKAGE
(CASE No.: ZIP–20P–M02)



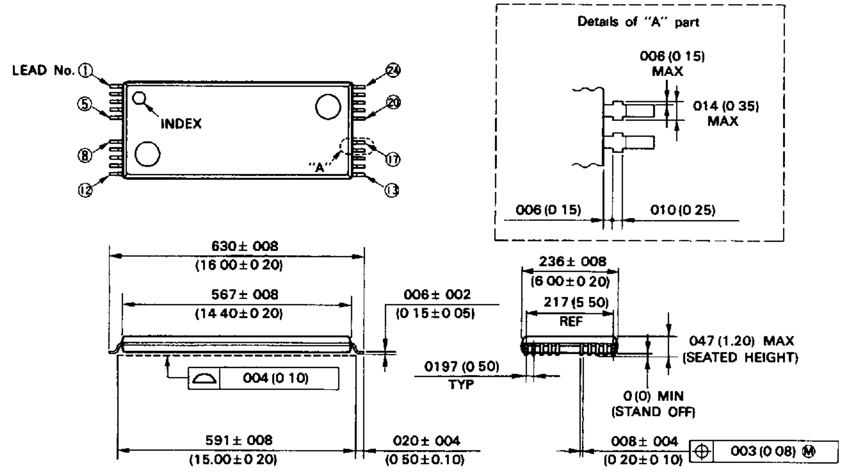
Dimensions in
inches (millimeters)

T-46-23-17

PACKAGE DIMENSIONS (Continued)

(Suffix: – PFTN)

24–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–24P–M04)



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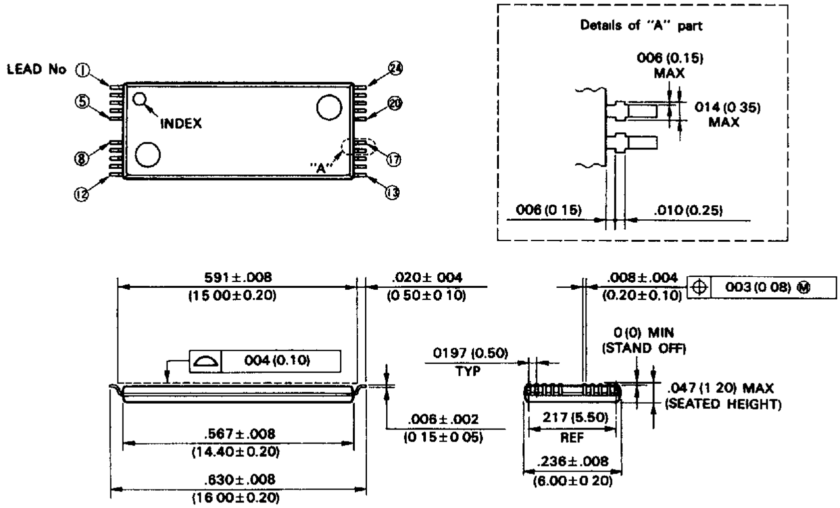
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: – PFTR)

24–LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT–24P–M05)



Dimensions in
inches (millimeters)