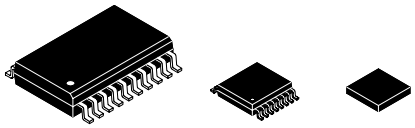


SLOS365 – AUGUST 2001

1.2-A HIGH-EFFICIENCY PWM POWER DRIVER

FEATURES

- **1.22-A DC (82% Duty Cycle) Output Current ($T_J \leq 89°C$)**
- **1-A DC (100% Duty Cycle) Output Current ($T_J \leq 89°C$)**
- **Low Supply Voltage Operation from 2.7 V to 5.5 V**
- **High Efficiency Generates Less Heat**
- **Over-Temperature Protection**
- **Short-Circuit Protection**
- **PowerPAD™ SOIC, TSSOP, and 4 × 4 mm MicroStar Junior™ Packages**

APPLICATIONS

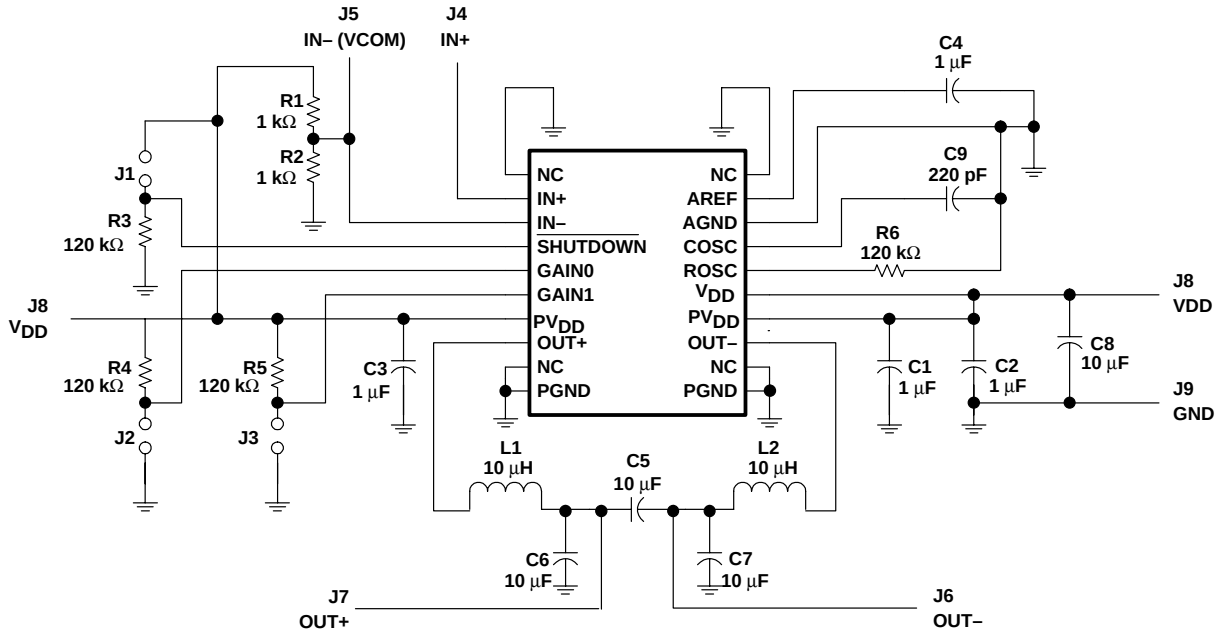
- **Thermoelectric Cooler (TEC) Driver**
- **Laser Diode Biasing**

DESCRIPTION

The DRV590 is a high-efficiency power amplifier ideal for driving a wide variety of thermoelectric cooler elements in systems powered from 2.7 V to 5.5 V. PWM operation and low output stage on-resistance significantly decrease power dissipation in the amplifier.

The DRV590 is internally protected against over temperature conditions and current overloads due to short circuits. The over temperature protection activates at a junction temperature of 190°C and will deactivate once the temperature is less than 130°C. If the overcurrent circuitry is tripped, the amplifier will automatically reset after 3–5 ms.

The gain of the DRV590 is controlled by two input terminals, GAIN1 and GAIN0. The amplifier may be configured for a gain of 6, 12, 18, and 23.5 dB.



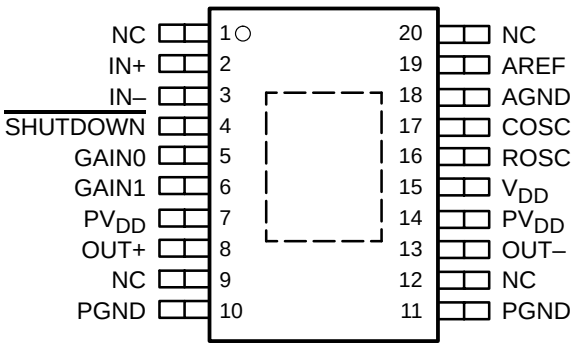
Typical Circuit Schematic for Driving a Thermoelectric Cooler Element

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		
	SOIC (DWP)	TSSOP (PW)†	GQC
–40°C to 85°C	DRV590DWP	DRV590PW	DRV590GQC

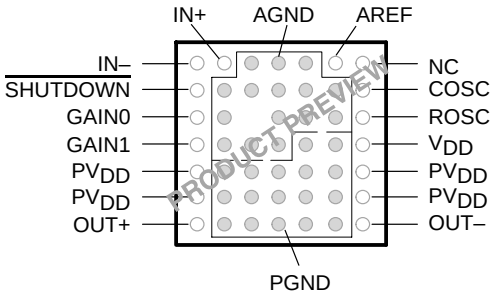
† The PW package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., DRV590PWR).

DWP PACKAGE
(TOP VIEW)



NC – No internal connection

MicroStar Junior™ (GQC) Package
(TOP VIEW)



(SIDE VIEW)

NC – No internal connection
NOTE: The shaded terminals are used for thermal connections to the ground plane.

Terminal Functions

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
AGND	18	I	Analog ground
AREF	19	O	Connect capacitor to ground for AREF voltage filtering (1 μF).
COSC	17	I	Connect capacitor to ground to set oscillation frequency (220 pF).
GAIN0	5	I	Bit 0 of gain control (TTL logic level)
GAIN1	6	I	Bit 1 of gain control (TTL logic level)
IN–	3	I	Negative differential input
IN+	2	I	Positive differential input
NC	1, 9, 12, 20		Not connected
OUT–	13	O	Negative BTL output
OUT+	8	O	Positive BTL output
PGND	10, 11	I	High-current grounds (2)
PV_{DD}	7, 14	I	High-current power supplies (2)
ROSC	16	I	Connect resistor to ground to set oscillation frequency (120 kΩ).
$\overline{SHUTDOWN}$	4	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal, and normal operation if a TTL logic high is placed on this terminal.
V_{DD}	15	I	Analog power supply

† DWP package only

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{DD}, PV_{DD} . . . . . –0.3 V to 5.5 V
Input voltage, V_I . . . . . –0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PW§	774 mW	6.19 mW/°C	495 mW	402 mW
GQC§	2.61 W	20.9 mW/°C	1.67 W	1.36 W
DWP	3.66 W	29.3 mW/°C	2.34 W	1.9 W

§ Product preview stage of development

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}, PV_{DD}		2.7	5.5	V
High-level input voltage, V_{IH}	GAIN0, GAIN1, $\overline{\text{SHUTDOWN}}$	2		V
Low-level input voltage, V_{IL}	GAIN0, GAIN1, $\overline{\text{SHUTDOWN}}$		0.8	V
Operating free-air temperature, T_A		–40	85	°C
Load impedance		1		Ω

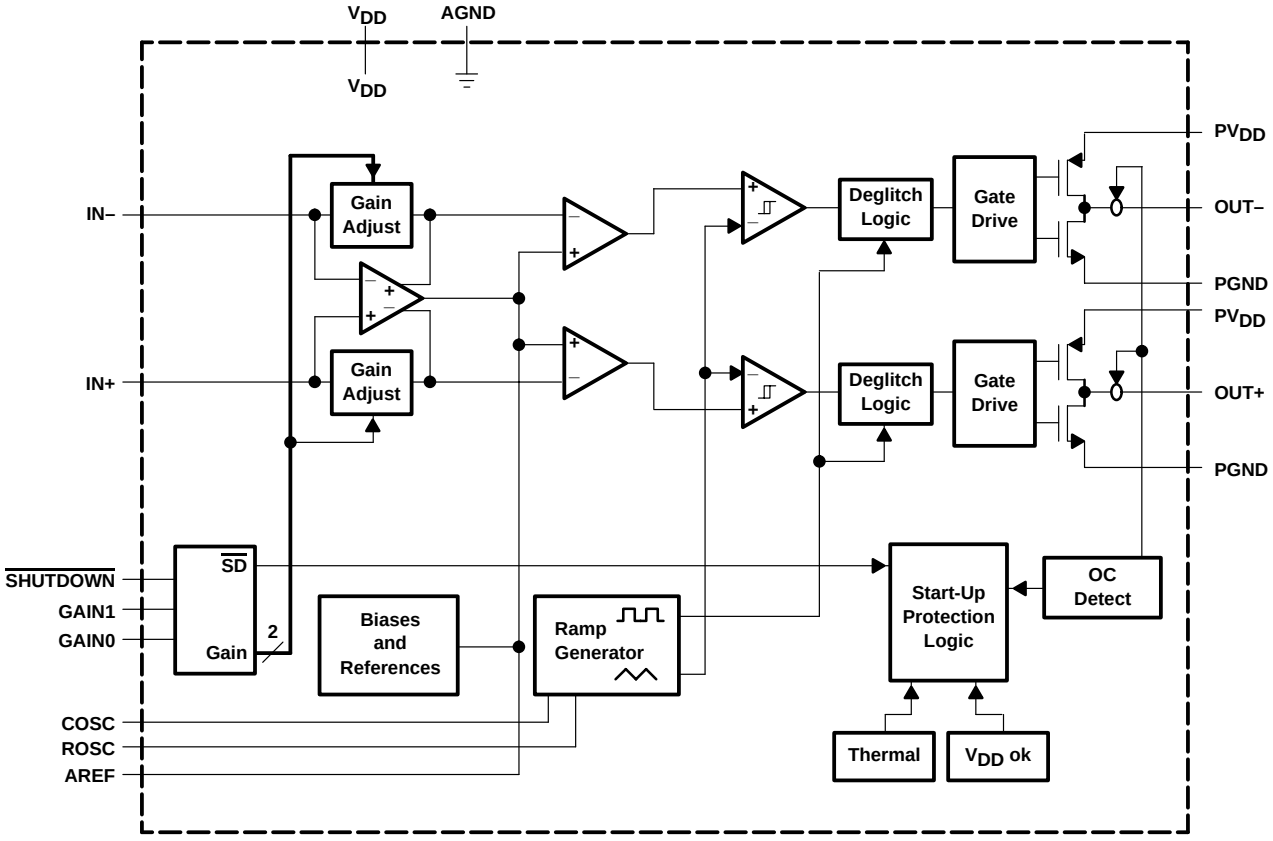
electrical characteristics at specified free-air temperature, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS}\rvert$	Output offset voltage (measured differentially)		V_I = 0 V, A_V = any gain			25	mV
PSRR	Power supply rejection ratio		PV_{DD} = 4.9 V to 5.1 V		77		dB
			PV_{DD} = 3.2 V to 3.4 V		61		
$\lvert I_{IH}\rvert$	High-level input current		$V_I = PV_{DD}$			1	µA
$\lvert I_{IL}\rvert$	Low-level input current		V_I = 0 V			1	µA
I_{DD}	Supply current, no filter				4.5	6.5	mA
$I_{DD(SD)}$	Supply current, shutdown mode				0.05	5	µA
	Gain		GAIN0 = low, GAIN1 = low	5.1	6	6.5	dB
			GAIN0 = high, GAIN1 = low	11	12	12.5	
			GAIN0 = low, GAIN1 = high	17	18	19	
			GAIN0 = high, GAIN1 = high	23	23.5	24	
f_S	Switching frequency	Single ended	R_{osc} = 120 kΩ, C_{osc} = 220 pF		250		kHz
		Differential			500		

operating characteristics, T_A = 25°C, R_L = 2 Ω, gain = 6 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_O	Maximum output current	Duty cycle = 82%		1.22		A
PSRR	Power supply rejection ratio	f = 1 kHz, $C_{(AREF)}$ = 1 µF		70		dB
Z_I	Input impedance			>15		kΩ
V_{ICR}	Common-mode input voltage range	PV_{DD} = 5 V	1.2		3.8	V
		PV_{DD} = 3.3 V	1.2		2.1	
$r_{ds(on)}$	Output on-resistance	PV_{DD} = 5 V		0.5		Ω
		PV_{DD} = 3.3 V		0.65		
η	Efficiency	PV_{DD} = 5 V		64%		
		PV_{DD} = 3.3 V		60%		
V_n	Integrated noise floor	f = 10 Hz to 5 kHz, Gain = 6 dB		23		µV rms

functional block diagram



TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Gain and phase	vs Frequency	1
	Efficiency	vs Load resistance	2, 3
PSRR	Power supply rejection ratio	vs Frequency	4
$r_{ds(on)}$	Small-signal drain-source on-state resistance	vs Supply voltage	5, 6
		vs Ambient temperature	7, 8
I_O	Maximum output current	vs Differential output voltage	9

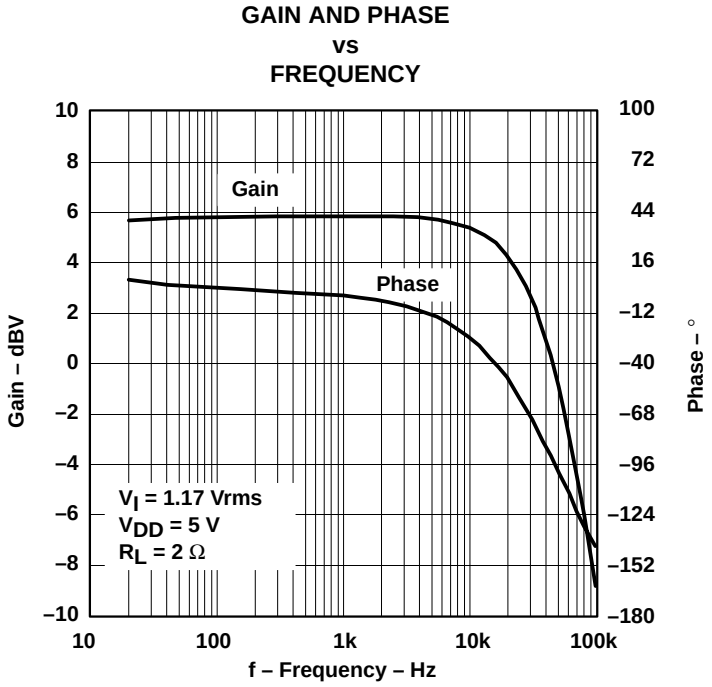


Figure 1

TYPICAL CHARACTERISTICS

EFFICIENCY
vs
LOAD RESISTANCE

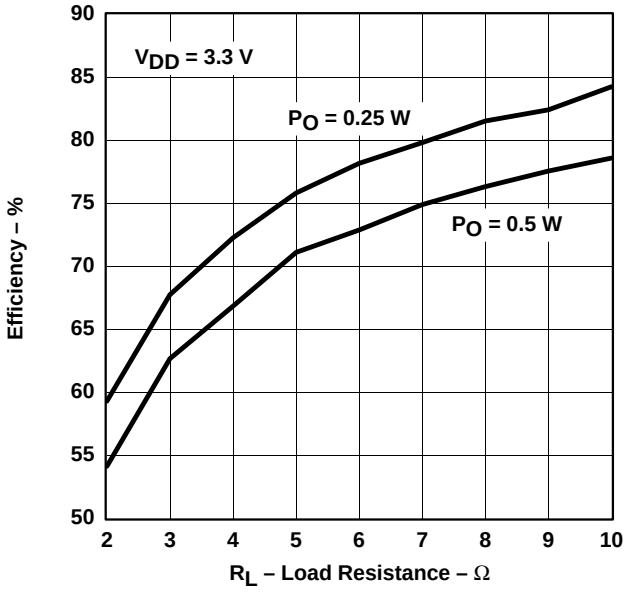


Figure 2

EFFICIENCY
vs
LOAD RESISTANCE

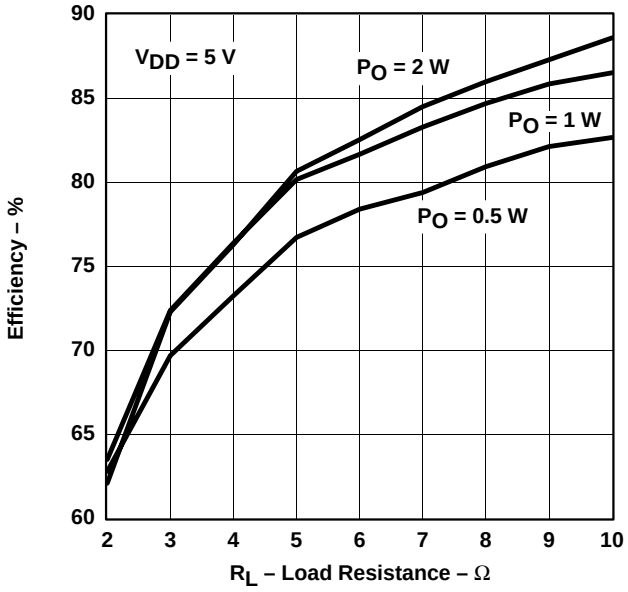


Figure 3

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

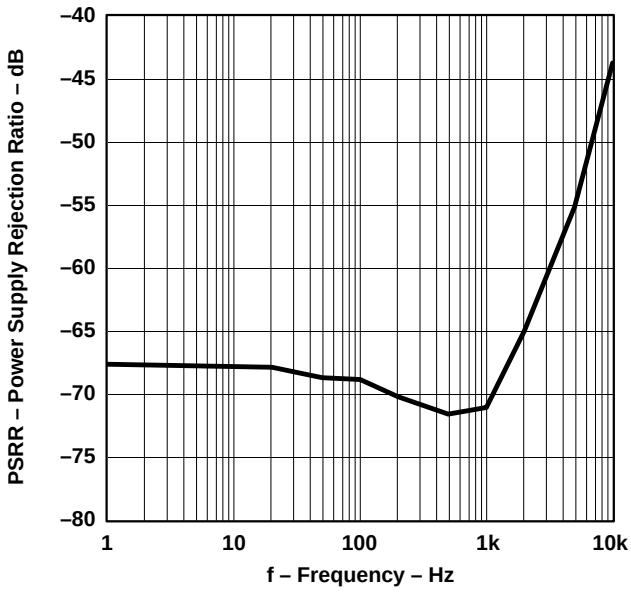


Figure 4

SMALL-SIGNAL DRAIN-SOURCE
ON-STATE RESISTANCE
vs
SUPPLY VOLTAGE

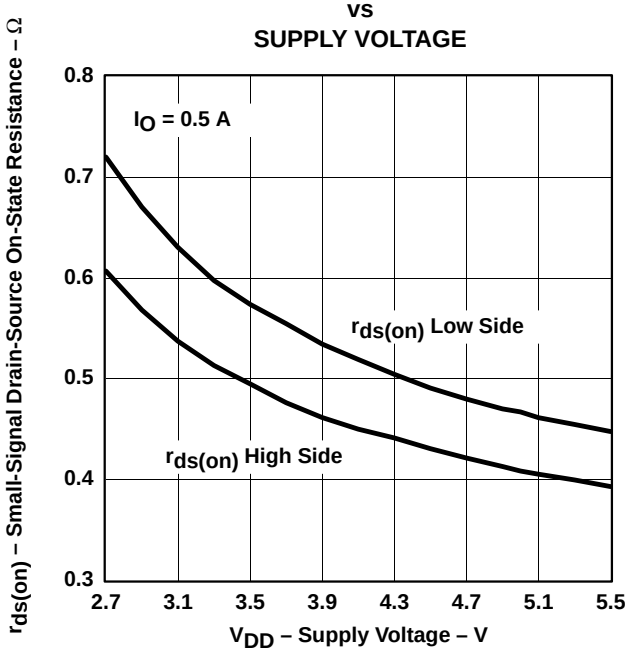


Figure 5

TYPICAL CHARACTERISTICS

SMALL-SIGNAL DRAIN-SOURCE ON-STATE RESISTANCE vs SUPPLY VOLTAGE

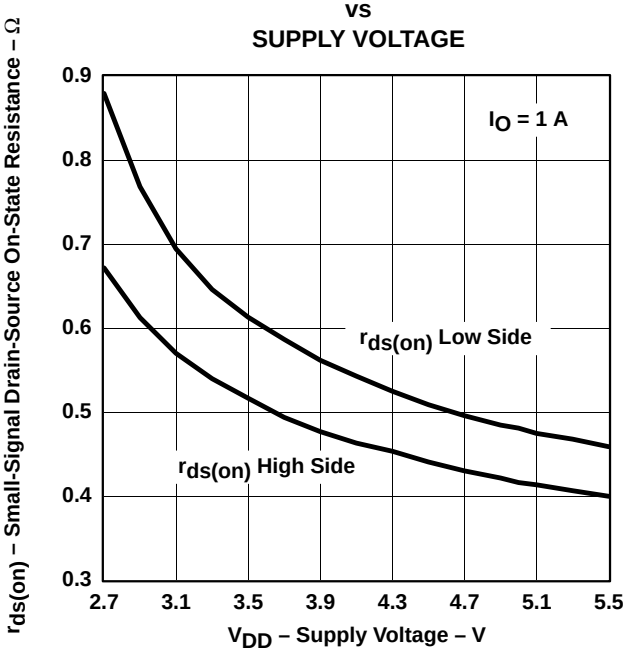


Figure 6

SMALL-SIGNAL DRAIN-SOURCE ON-STATE RESISTANCE vs AMBIENT TEMPERATURE

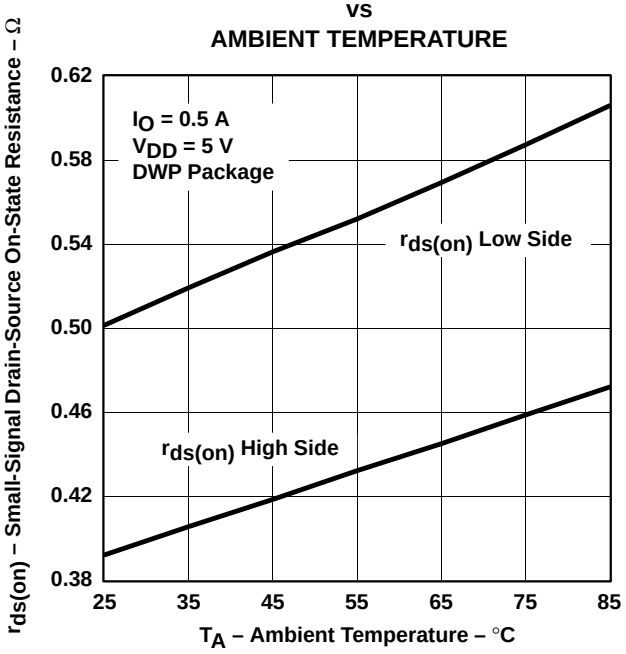


Figure 7

SMALL-SIGNAL DRAIN-SOURCE ON-STATE RESISTANCE vs AMBIENT TEMPERATURE

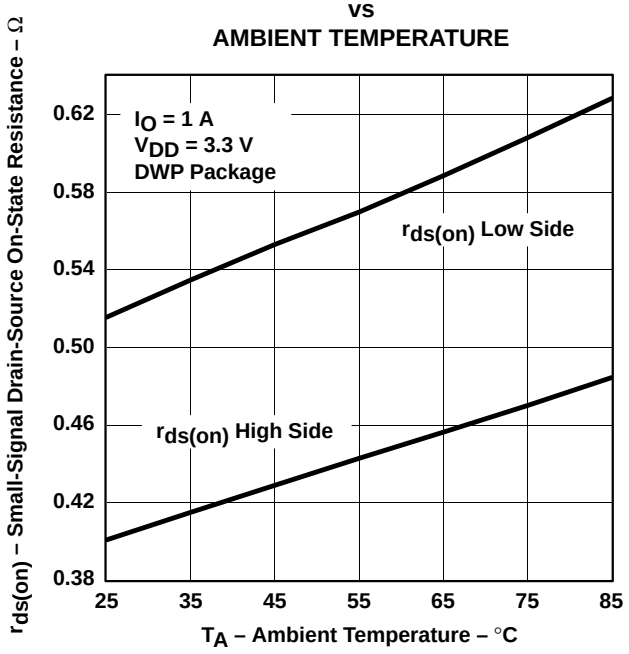


Figure 8

MAXIMUM OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

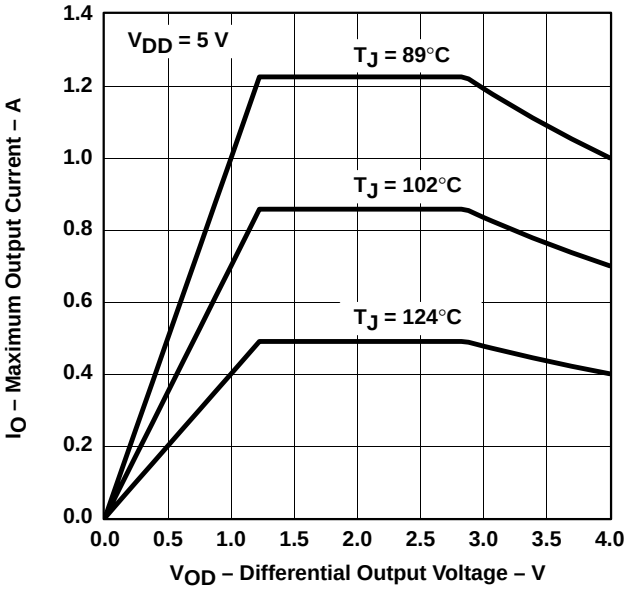
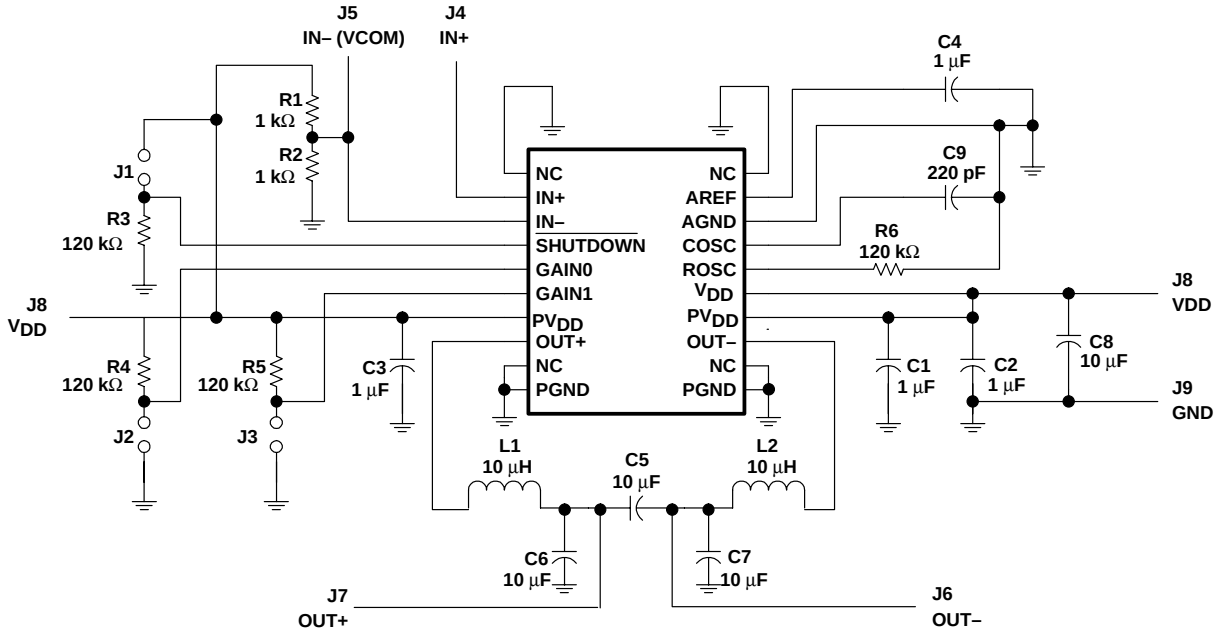


Figure 9

APPLICATION INFORMATION

driving TEC elements

Below is a typical application schematic.



output filter considerations

TEC element manufacturers provide electrical specifications for maximum dc current and maximum output voltage for each particular element. The maximum ripple current, however, is typically only recommended to be less than 10%. The maximum temperature differential across the element decreases as ripple current increases and can be calculated using equation 1.

$$\Delta T = \frac{1}{(1 + N^2) \times \Delta T_{max}} \quad (1)$$

ΔT = actual temperature differential
ΔT_{max} = maximum temperature differential (specified by manufacturer)
N = ratio of ripple current to dc current

According to this relationship, a 10% ripple current reduces the maximum temperature differential by 1%. A LC network may be used to filter the current flowing to the TEC to reduce the amount of ripple and, more importantly, protect the rest of the system from any electromagnetic interference (EMI).

APPLICATION INFORMATION

driving TEC elements (continued)

filter component selection

The LC filter may be designed from a couple of different perspectives, both of which may help estimate the overall performance of the system. The filter should be designed for the worst-case conditions during operation, which is typically when the differential output is at 50% duty cycle. The following section serves as a starting point for the design, and any calculations should be confirmed with a prototype circuit.

To simplify the design, half-circuit analysis may also be used. This should only be done if the TEC element is close to the output of the filter. Any filter should always be placed as close to the DRV590 as possible to reduce EMI.

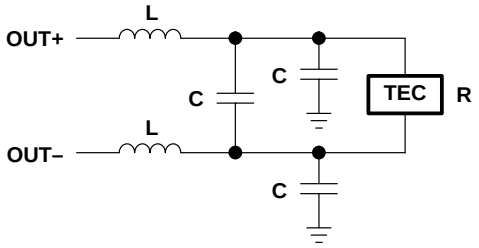


Figure 10. LC Output Filter

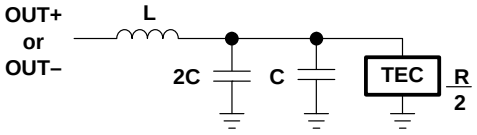


Figure 11. LC Half-Circuit Equivalent

LC filter in the frequency domain

The transfer function for the second order low-pass filter in Figure 10 and Figure 11 is shown in equation 2.

$$H_{LP}(j\omega) = \frac{1}{-\left(\frac{\omega}{\omega_0}\right)^2 + \frac{1}{Q}\frac{j\omega}{\omega_0} + 1} \quad (2)$$

$$\omega_0 = \frac{1}{\sqrt{L \times 3C}}$$

Q = quality factor

ω = DRV590 differential switching frequency

For the DRV590, the differential output switching frequency is 500 kHz. The resonant frequency for the filter should be chosen to be at least one order of magnitude lower than the switching frequency. Equation 2 may then be simplified to give the following magnitude equation 3. These equations assume the use of the filter in Figure 10, which effectively triples the capacitance.

$$\left|H_{LP}\right|_{dB} = -40 \log\left(\frac{f_s}{f_o}\right) \quad (3)$$

$$f_o = \frac{1}{2\pi\sqrt{L \times 3C}}$$

f_s = 500 kHz (DRV590 differential switching frequency)

APPLICATION INFORMATION

LC filter in the frequency domain (continued)

If L = 10 μH and C = 10 μF, the resonant frequency is 9.2 kHz, which corresponds to –69 dB of attenuation at the 500-kHz switching frequency. For V_{DD} = 5 V, the amount of ripple voltage at the TEC element will be approximately 1.7 mV.

The average TEC element has a resistance of 1.5 Ω, so the ripple current through the TEC is approximately 1.13 mA. At the 1-A maximum output current of the DRV590, this 1.13 mA corresponds to 0.113% ripple current, causing less than 0.0001% reduction of the maximum temperature differential of the TEC element (see equation 1).

LC filter in the time domain

The ripple current of an inductor can be calculated using equation 4.

$$\Delta I_L = \frac{\left(V_{DD} - V_{TEC}\right)DT_S}{L} \quad (4)$$

D = duty cycle (0.5 worst case)

$T_S = 1/f_S$ = 1/500 kHz

For V_{DD} = 5 V, V_{TEC} = 2.5 V, and L = 10 μH, the inductor ripple current is 250 mA. To calculate how much of that ripple current will flow through the TEC element, however, the properties of the filter capacitor must be considered.

For relatively small capacitors (less than 10 μF) with very low equivalent series resistance (ESR, less than 10 mΩ), such as ceramic capacitors, equation 5 may be used to estimate the ripple voltage on the capacitor due to the change in charge.

$$\Delta V_C = \frac{\pi^2}{2}(1–D)\left(\frac{f_o}{f_s}\right)^2 V_{TEC} \quad (5)$$

D = duty cycle

f_S = 500 kHz

$$f_o = \frac{1}{2\pi\sqrt{L \times 3C}}$$

For L = 10 μH and C = 10 μF, the cutoff frequency f_o = 9.2 kHz. For a worst case duty cycle of 0.5 and V_{TEC} = 2.5, the ripple voltage on the capacitors is 2 mV. The ripple current may be simply calculated by dividing the ripple voltage by the TEC resistance of 1.5 Ω, resulting in a ripple current through the TEC element of 1.33 mA. Note that this is similar to the value calculated using the frequency domain approach.

For larger capacitors (greater than 10 μF) with relatively high ESR (greater than 100 mΩ), such as electrolytic capacitors, the ESR drop dominates over the charging-discharging of the capacitor. Equation 6 can be used to estimate the ripple voltage.

$$\Delta V_C = \Delta I_L \times R_{ESR} \quad (6)$$

Δ_L = inductor ripple current

R_{ESR} = filter capacitor ESR

For a 100-μF electrolytic capacitor, an ESR of 0.1 Ω is common. If the 10-μH inductor is used, delivering 250 mA of ripple current to the capacitor (as calculated above), then the ripple voltage is 25 mV. This is over ten times that of the 10-μF ceramic capacitor, as ceramic capacitors typically have negligible ESR.

APPLICATION INFORMATION

LC filter in the time domain (continued)

For worst case conditions, the on-resistance of the output transistors has been ignored to give the maximum theoretical ripple current. In reality, the voltage drop across the output transistors will decrease the maximum V_O as the output current increases. It can be shown using equation 4 that this will decrease the inductor ripple current, and therefore the TEC ripple current.

general operation

oscillator components R_{OSC} and C_{OSC}

The onboard ramp generator requires an external resistor and capacitor to set the oscillation frequency. For proper operation, the resistor R_{OSC} should be 120 kΩ with 1% tolerance. The capacitor C_{OSC} should be a ceramic 220 pF with 10% tolerance. Both components should be grounded to AGND, which should be connected to PGND at a single point, typically where the power and ground physically connect to the printed circuit board.

AREF capacitor

The AREF terminal is the output of an internal mid-rail voltage regulator used for the on-board oscillator and ramp generator. The regulator may not be used to provide power to any additional circuitry. A 1-µF ceramic capacitor must be connected from AREF to AGND for stability (see the *oscillator components R_{OSC} and C_{OSC}* section for AGND connection information).

gain settings

The differential output voltage may be calculated using equation 7.

$$V_O = V_{OUT+} - V_{OUT-} = Av\left(V_{IN+} - V_{IN-}\right) \quad (7)$$

Av is the voltage gain, which may be selected by configuring GAIN0 and GAIN1 according to the table below. The input resistance also varies with the gain setting, as shown by the typical values in Table 1. Though these values may vary by up to 30% due to process variations, the gain settings themselves vary little, as they are determined by resistor ratios.

Table 1. Gain Settings

GAIN0	GAIN1	AMPLIFIER GAIN (dB, TYPICAL)	INPUT RESISTANCE (kΩ, TYPICAL)
0	0	6	104
0	1	12	74
1	0	18	44
1	1	23.5	24

APPLICATION INFORMATION

general operation (continued)

input configuration—differential and single-ended

If a differential input is used, it should be biased around the mid-rail of the DRV590 and must not exceed the common-mode input range of the input stage (see the operating characteristics at the beginning of the data sheet).

The most common configuration employs a single-ended input. The unused input should be tied to the mid-rail, which may be simply accomplished with a resistive voltage divider. For the best performance, the resistor values chosen should be at least an order of magnitude lower than the input resistance of the DRV590 at the selected gain setting. This prevents the bias voltage at the unused input from shifting when the signal input is applied. A small ceramic capacitor should also be placed from the input to ground to filter noise and keep the voltage stable.

power supply decoupling

To reduce the effects of high-frequency transients or spikes, a small ceramic capacitor, typically 0.1 μF to 1 μF, should be placed as close to each PVDD pin of the DRV590 as possible. For bulk decoupling, a 10-μF to 100-μF tantalum or aluminum electrolytic capacitor should be placed relatively close to the DRV590.

SHUTDOWN operation

The DRV590 includes a shutdown mode that disables the outputs and places the device in a low supply current state. The SHUTDOWN pin may be controlled with a TTL logic signal. When SHUTDOWN is held high, the device operates normally. When SHUTDOWN is held low, the device is placed in shutdown. The SHUTDOWN pin must not be left floating. If the shutdown feature is unused, the pin may simply be connected to V_{DD}.

power dissipation and maximum ambient temperature

Though the DRV590 is much more efficient than traditional linear solutions, the IR drop across the on-resistance of the output transistors generates some heat in the package, which may be calculated using equation 8.

$$P_{DISS} = \left(I_{OUT}\right)^2 \times r_{ds(on),\ total} \tag{8}$$

For example, at the maximum output current of 1.2 A through a total on-resistance of 1 Ω, the power dissipated in the package is 1.44 W.

The maximum ambient temperature can be calculated using equation 9.

$$T_A = T_J\left(\theta_{JA} \times P_{DISS}\right) \tag{9}$$

Continuing the example above, the maximum ambient temperature driving 1.2 A without exceeding 89°C junction temperature for a DRV590 in the DWP package (see the *maximum output current vs duty cycle* section) is 39°C.

maximum output current vs duty cycle

At 100% duty cycle across the load, the reliability of the DRV590 is degraded if more than 1 A is driven through the outputs. Furthermore, the junction temperature must not exceed 89°C at the maximum output current levels to prevent further degradation. However, as the duty cycle across the load decreases, the maximum allowable output current increases.

Table 2 shows the typical maximum output current, voltage across the load, and junction temperature versus duty cycle. The dissipation and junction temperatures were calculated using equations 8 and 9. The total on-resistance was assumed to be 1 Ω, the ambient temperature to be 25°C, and the θ_{JA} to be 34.1°C/W.

APPLICATION INFORMATION

maximum output current vs duty cycle (continued)

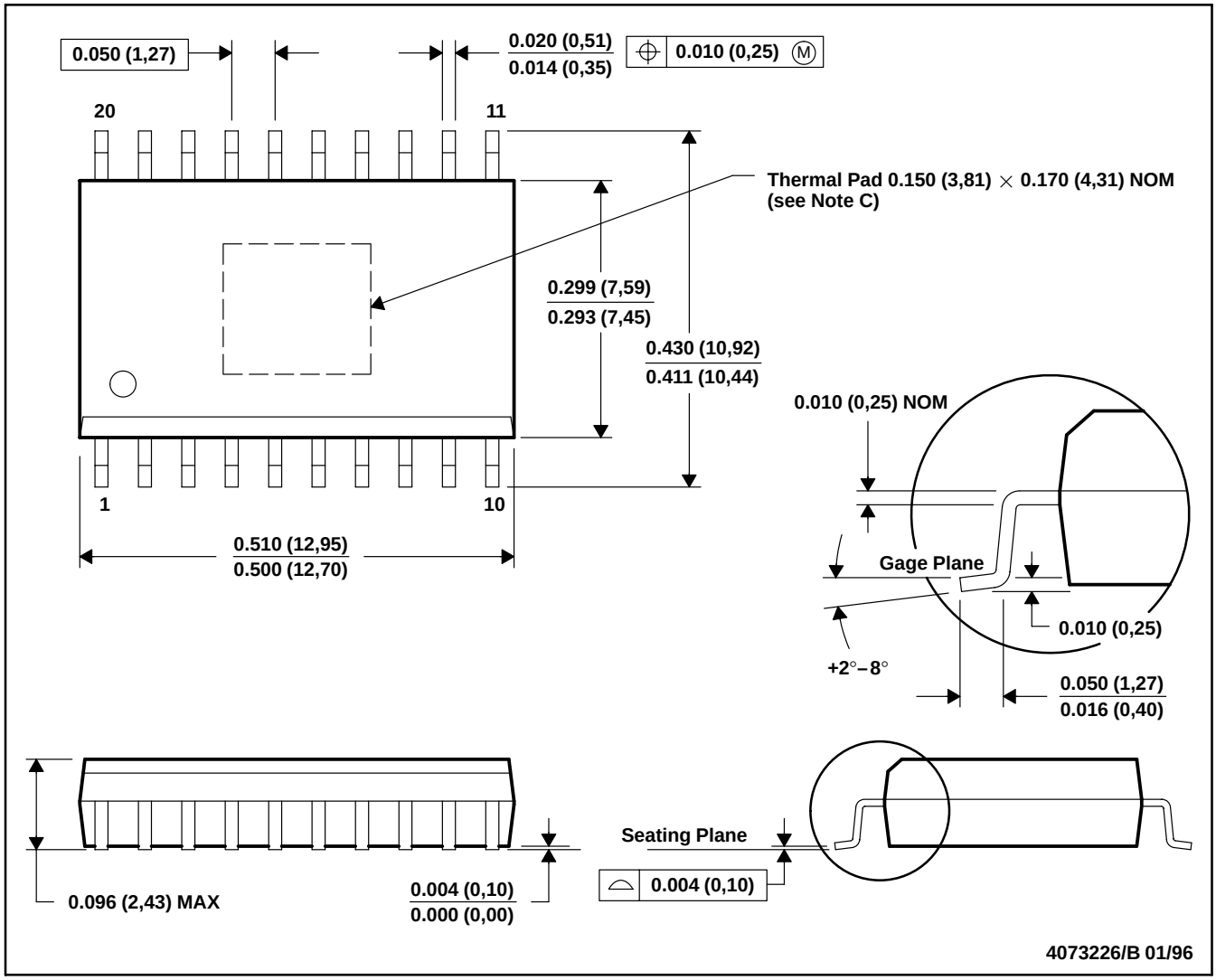
Table 2. Typical Maximum Output Specifications vs Duty Cycle (V_{DD} = 5 V)

DUTY CYCLE	MAX I_O (A)	MAX V_{LOAD} (V)	P_{DISS} (W)	T_J (°C)
100%	1	4	1	67.6
95%	1.05	3.69	1.11	72.2
90%	1.11	3.38	1.24	77.6
85%	1.17	3.07	1.39	83.9
84%	1.19	3.01	1.42	85.3
83%	1.2	2.94	1.45	86.8
82%	1.22	2.88	1.49	88.3

At duty cycles less than 82%, the power dissipated from the theoretical maximum current flowing through the on-resistance causes the junction temperature to exceed 89°C. See Figure 9 for more details.

MECHANICAL DATA

DWP (R-PDSO-G20) **PowerPad™ PLASTIC SMALL-OUTLINE PACKAGE**



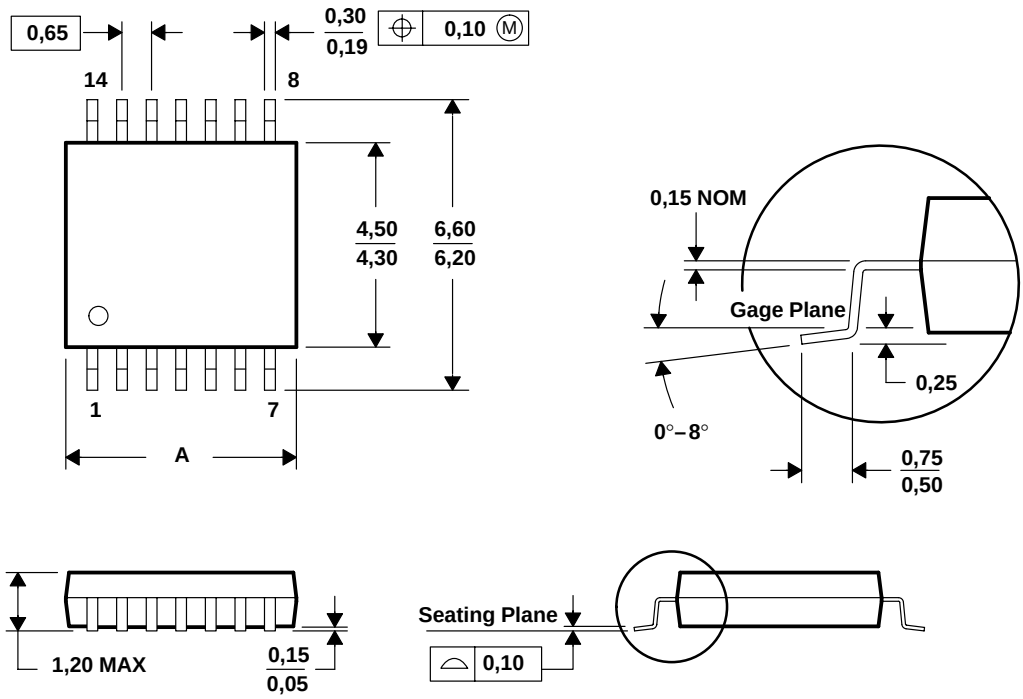
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This solderable pad is electrically and thermally connected to the backside of the die and leads 1, 10, 11 and 20.

PowerPad is a trademark of Texas Instruments.

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

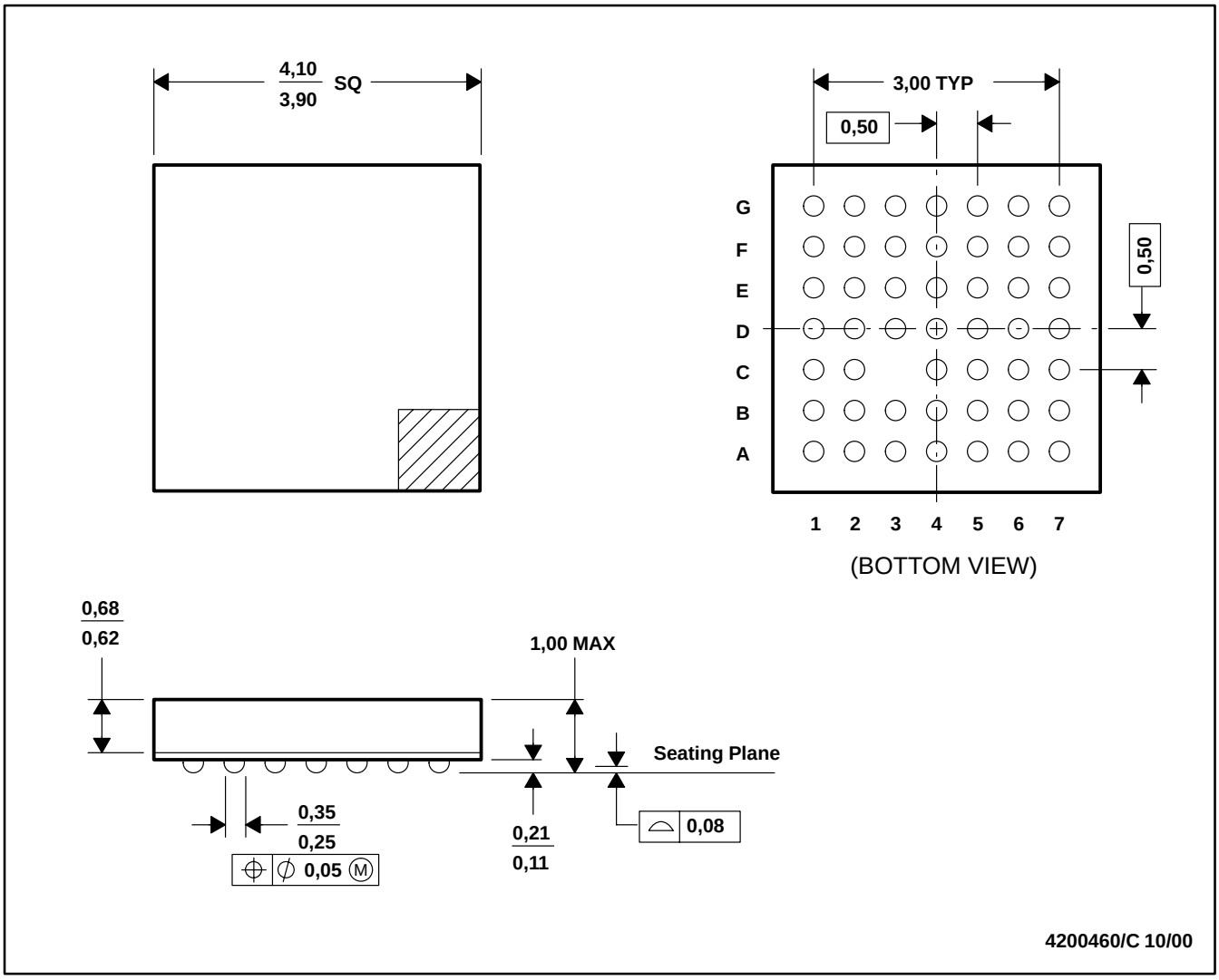
4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

MECHANICAL DATA

GQC (S-PBGA-N48) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior BGA ™ configuration
D. Falls within JEDEC MO-225

MicroStar Junior BGA is a trademark of Texas Instruments.

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

DRV590, High Efficiency PWM Power Driver

DEVICE STATUS: **ACTIVE**

RECOMMENDED REPLACEMENT DEVICES

Part Number	Comments
DRV591	The device has the SAME FUNCTIONALITY as the compared device, but is not pin-for-pin equivalent and may not be parametrically equivalent.Consider the DRV591 for a smaller, more efficient solution.

PARAMETER NAME	DRV590
IO (max) (A)	1.2
VCC / VDD (max) (V)	5.5
VCC / VDD (min) (V)	2.7
Fs (Single-Ended) (kHz)	250
Fs (Differential) (kHz)	500
rDS(on) (Ohms)	0.4
VICM (max) (V)	3.8
VICM (min) (V)	1.2
PSRR (dB)	77
Iq (mA)	4

FEATURES

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- 1.22-A DC (82% Duty Cycle) Output Current ($T_J \leq 89°C$)
- 1-A DC (100% Duty Cycle) Output Current ($T_J \leq 89°C$)
- Low Supply Voltage Operation from 2.7 V to 5.5 V
- High Efficiency Generates Less Heat
- Over-Temperature Protection
- Short-Circuit Protection
- PowerPAD™ SOIC, TSSOP, and 4 × 4 mm MicroStar Junior™ Packages
- APPLICATIONS
  - Thermoelectric Cooler (TEC) Driver
  - Laser Diode Biasing

DESCRIPTION

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The DRV590 is a high-efficiency power amplifier ideal for driving a wide variety of thermoelectric cooler elements in systems powered from 2.7 V to 5.5 V. PWM operation and low output stage on-resistance significantly decrease power dissipation in the amplifier.

The DRV590 is internally protected against over temperature conditions and current overloads due to short circuits. The over temperature protection activates at a junction temperature of 190°C and will deactivate once the temperature is less than 130°C. If the overcurrent circuitry is tripped, the amplifier will automatically reset after 3-5 ms.

The gain of the DRV590 is controlled by two input terminals, GAIN1 and GAIN0. The amplifier may be configured for a gain of 6, 12, 18, and 23.5 dB.

TECHNICAL RESOURCES

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: drv590.pdf (253 KB) (Updated: 09/04/2001)

APPLICATION NOTES

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- AB-172: Current Feedback Amplifiers: Review, Stability Analysis,and Applications (SBOA081 - Updated: 11/20/2000)
- Analysis of the Sallen-Key Architecture (Rev. A) (SLOA024A - Updated: 07/27/1999)
- Burr-Brown SPICE Based Macromodels (SBFA009 - Updated: 10/04/2000)
- Handbook of Operational Amplifier Active RC Networks (Rev. A) (SBOA093A - Updated: 10/04/2001)
- Handbook of Operational Amplifier Applications (Rev. A) (SBOA092A - Updated: 10/24/2001)
- PWM Power Driver Modulation Schemes (SLOA092 - Updated: 10/29/2001)

RELATED DOCUMENTS

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- Military Analog Selection Guide (SGLB002, 318 KB - Updated: 11/09/2000)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

BLOCK DIAGRAMS

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- Optical Networking - Erbium Doped Fiber Amplifier
- Optical Networking - Transmission Laser (2.5 GHz/Analog control)
- Optical Networking - Transmission Laser (2.5 GHz/Digital control)

SAMPLES

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ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	SAMPLES
DRV590DWP	DWP	20	-40 TO 85	ACTIVE	Request Samples

PRICING/AVAILABILITY/PKG

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ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	BUDGETARY PRICE US$/UNIT QTY=1000+	PACK QTY	PRICING/AVAILABILITY/PKG
DRV590DWP	DWP	20	-40 TO 85	ACTIVE	6.96	100	Check stock or order
DRV590DWPR	DWP	20	-40 TO 85	ACTIVE	6.96	2000	Check stock or order

Table Data Updated on: 7/25/2002