NE502-N

DESCRIPTION

The NE502 is a MOS monolithic integrated circuit, generally intended to delay analogue signals (e.g. delay time = $512/2f_0$).

It can be used with clock frequencies in the range 5kHz to 500kHz.

The device contains 512 stages, so the input signal can be delayed from 51.2ms to 0.512ms.

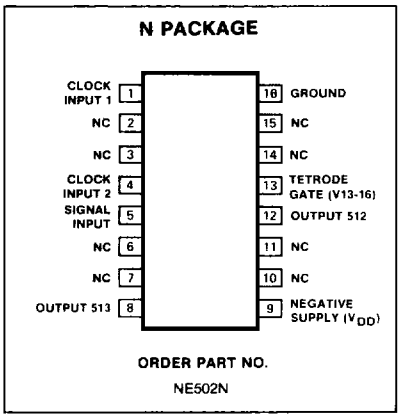
APPLICATIONS

- **Fixed analog delay**
- **V_{OX} control**
- **Equalizing speech delay in PA systems**
- **Vibrato and chorus effects**
- **Reverberation**
- **Variable compression/expansion of speech**
- **Speech scrambling and time scale conversion**

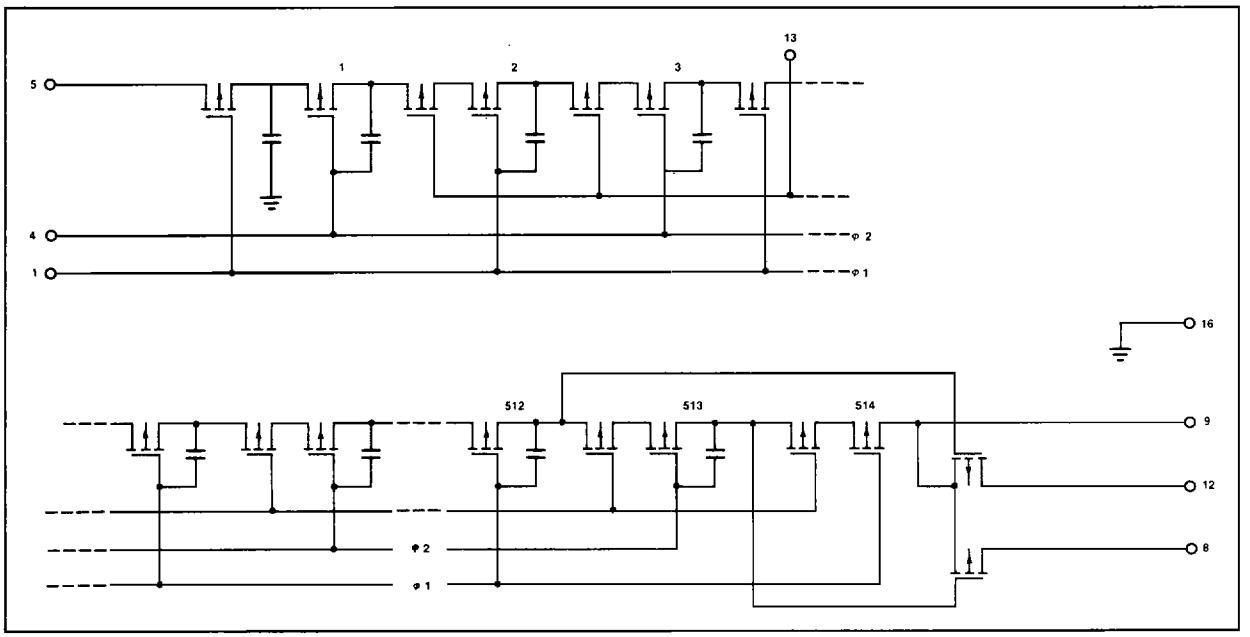
FEATURES

- **5 to 500kHz clock frequency**
- **512 stages**
- **Signal delay of 51.2 to .512ms**
- **Signal frequency to 45kHz**

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Voltages*		
V_{9-16}	Supply voltage	0 to -20	V
	Clock input, data input, output voltage and V_{13-16}	0 to -18	V
	Current		
I_8, I_{12}	Output current	0 to +5	mA
	Temperatures		
T_{STG}	Storage temperature	-40 to +150	°C
T_A	Operating ambient temperature	-20 to +85	°C

*NOTE

Though MOS integrated circuits incorporate protection against electrostatic discharge, they can nevertheless be damaged by accidental over-voltages. To be totally safe, it is desirable to take handling precautions into account.

DC ELECTRICAL CHARACTERISTICS

T_A = -20°C to +55°C, V_{DD} = -15V, $V\phi_1 = V\phi_2$ = -15V, V_{13-16} = -14V, R_L = 47kΩ unless otherwise specified.

PARAMETER		TEST CONDITIONS	NE502			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage[1]		-18		-10	V
I_{DD}	Supply current			.3		mA
$V\phi_{1H}$, $V\phi_{2H}$	Clock voltage high		-1.5		0	V
$V\phi_{1L}$, $V\phi_{2L}$	Clock voltage low[1]		-18	-15	-10	V
V_{IN}	Input voltage	$V_{OUT} \leq$ 1% THD		2.5		Vrms
R_L	Load resistance[1]		10	47		kΩ

AC ELECTRICAL CHARACTERISTICS

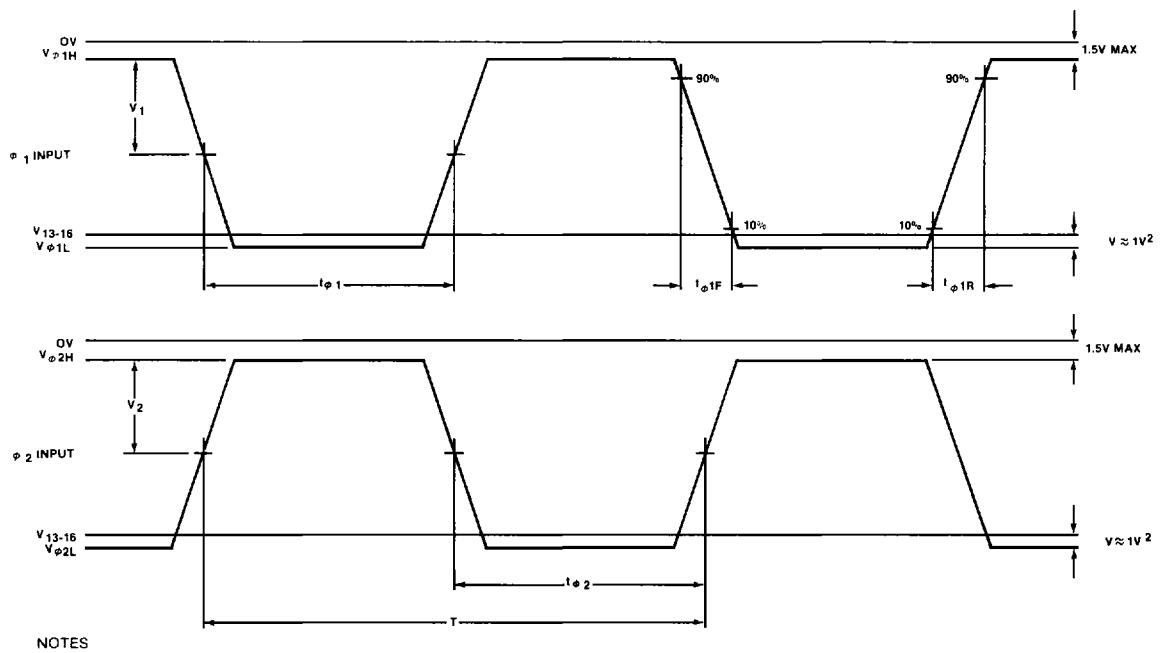
T_A = -20°C to +55°C, V_{DD} = -15V, $V\phi_1 = V\phi_2$ = -15V, V_{13-16} = -14V, R_L = 47kΩ unless otherwise specified.

PARAMETER		TEST CONDITIONS	NE502			UNIT
			Min	Typ	Max	
$f\phi_1$, $f\phi_2$	Clock frequency[2]		5		500	kHz
$T\phi_1$, $T\phi_2$	Clock pulse width[3]				.5	T
$T_r\phi_1$, $T_r\phi_2$	Clock rise time[3]			0.05		T
$T_f\phi_1$, $T_f\phi_2$	Clock fall time[3]			0.05		T
f_S	Signal frequency		0		45	kHz
	Signal attenuation[1]	$f\phi$ = 40kHz, f_S = 1kHz		4	7	dB
	Output signal variation	f_S = 1kHz, V_S = 1Vrms, 5kHz ≤ $f\phi$ ≤ 100kHz		.5	1	dB
	Output signal variation	f_S = 1kHz, V_S = 1Vrms, 100kHz ≤ $f\phi$ ≤ 300kHz		.5	1	dB
ΔV_{OUT}	DC voltage shift	5kHz ≤ $f\phi$ ≤ 300kHz			.5	V
V_N	Noise voltage	$f\phi$ = 100kHz (weighted by "A" curve)		.25		mVrms
S/N	Signal to noise			74		dB

NOTES

1. It is recommended that $V_{13-16} = V\phi_{1L} + 1V = V\phi_{2L} + 1V$; V_{DD} more negative than $V\phi_L$.
2. In theory the clock frequency must be higher than twice the highest signal frequency, in practice $f_S \leq 0.3f\phi$ to $0.5f\phi$ is recommended, depending on the characteristics of the output filter
3. T = period time = $1/f\phi$. The data on fall and rise times are given to eliminate overlap between the two clock pulses. To be independent of these rise and fall times a clock generator with simple gating can be used. See also pages 5 and 8

TIMING DIAGRAM

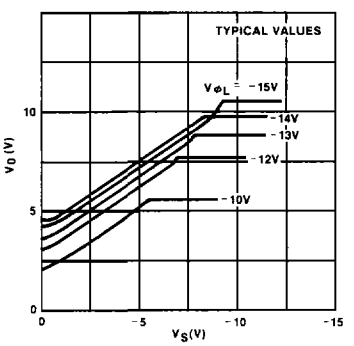


NOTES

1. $|V_1 + V_2| \leq |V_{\phi 1L}| = V_{\phi 2L}$.
2. For maximum dynamic range adjust V_{13-16} so that $\Delta V = V_{13-16} - V_{\phi L} \approx 1V$.

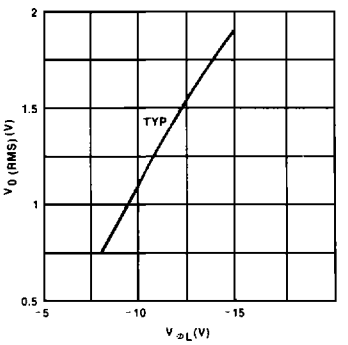
TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE vs SIGNAL VOLTAGE



V_{DD} = -15V
V_{13-16} = -14V
$V_{\phi H}$ = 0V
f_ϕ = 40kHz
R_L = 47kΩ

V_{OUT} vs $V_{\phi LOW}$

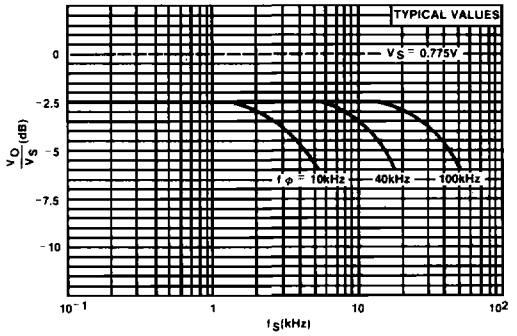


V_{DD} = -15V
V_{13-16} = -14V
$V_{\phi H}$ = 0V
f_ϕ = 40kHz
f_s = 1kHz
R_L = 47kΩ

9

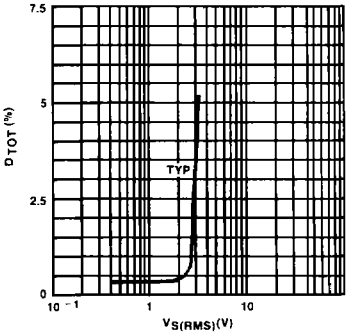
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

OUTPUT ATTENUATION



V_{DD} = -15V
V_{13-16} = -14V
V_ϕ = 0 to -15V

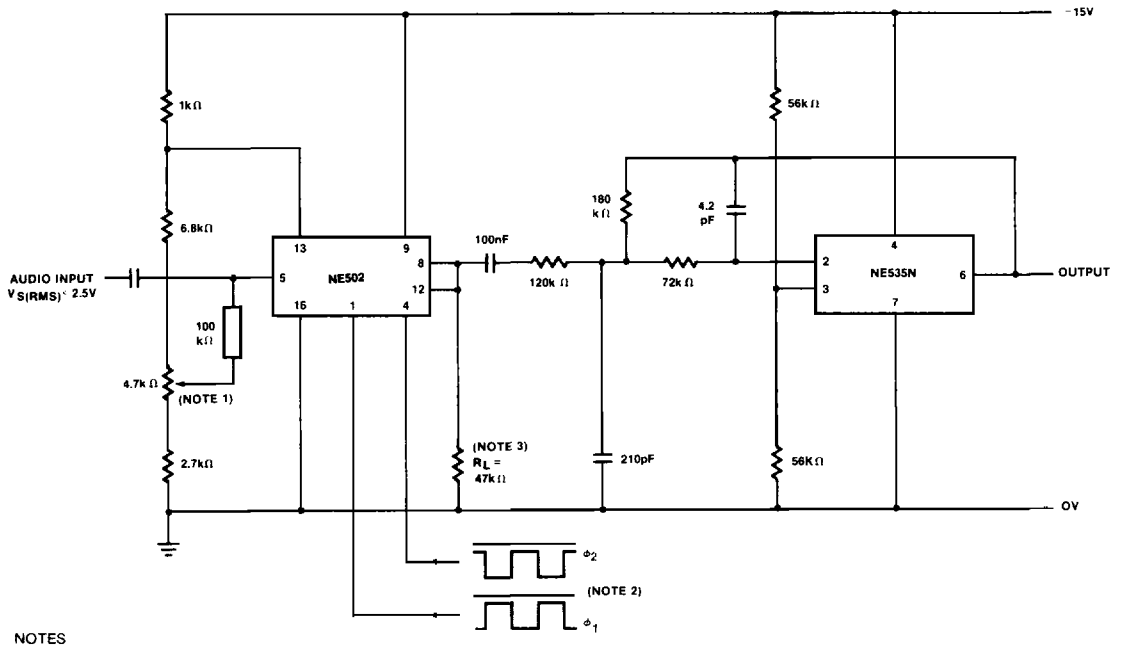
DISTORTION vs INPUT SIGNAL LEVEL



f_S = 1kHz
V_S = -5. 2V
V_{DD} = -15V
V_{13-16} = -14V
V_ϕ = 0 to -15V
f_ϕ = 40kHz

TYPICAL APPLICATIONS

SINGLE DELAY LINE CONNECTION

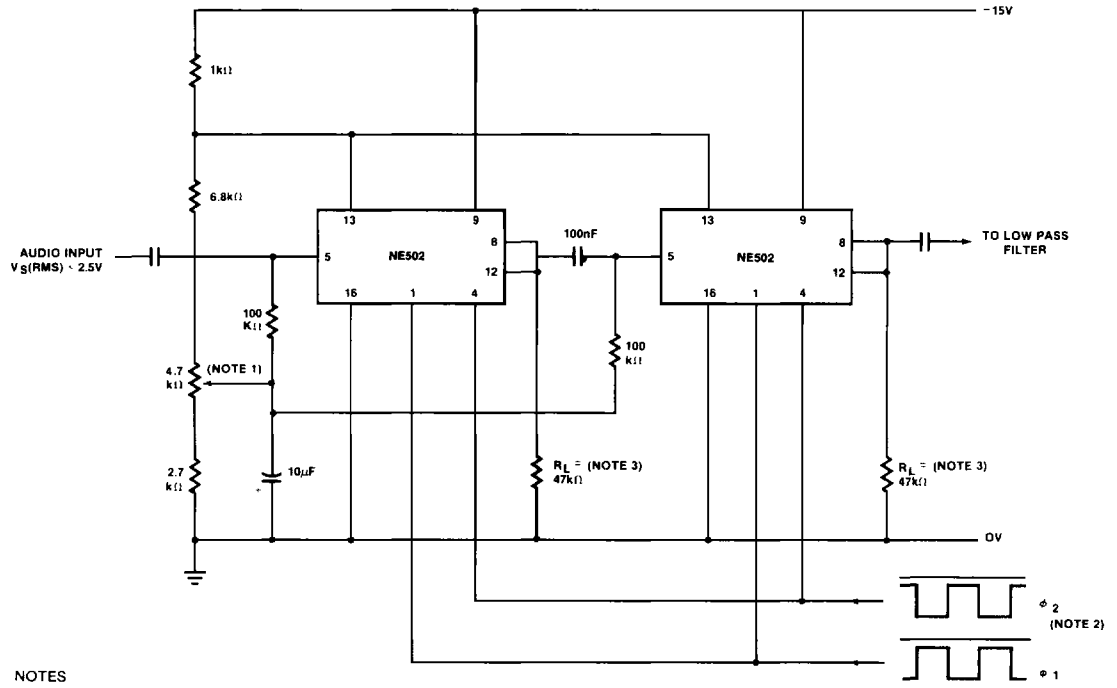


NOTES

1. Adjust dc voltage for class-A operation (≈ 5V).
   Conditions: low pass filter μA741CV (12dB per octave);
   gain = +3.5dB (compensation for line attenuation);
   f_ϕ = 50kHz (min.);
   cut-off frequency = 15kHz.
2. Clock input voltage amplitude: V_{CL} = -15V.
3. Can be replaced by a current source of 100 to 400μA

TYPICAL APPLICATIONS (Cont'd)

SERIES CONNECTION OF TWO LINES NE502



NOTES

1. Adjust dc voltage for class-A operation (≈ 5V).
2. Clock input voltage amplitude: V_{CL} = -15V.
3. Can be replaced by a current source of 100 to 400μA (see also note 1 on page 4).

TYPICAL APPLICATIONS (Cont'd)

CLOCK OSCILLATOR AND DRIVER CIRCUIT WITH ELIMINATION OF OVERLAP (FOR MAX. 6xNE502)