PARADIGM®

Preliminary

PDM4M6110
PDM4M6111
PDM4M6112

256KB and 512KB Second Cache Modules for the PowerPC

Features

- ☐ 256KB asynchronous and 256KB/512KB pipelined cache modules.
- ☐ Ideal for use with PowerPC™ based systems.
- ☐ Separate 5V and 3.3V power supplies.
- ☐ Operates with external PowerPC CPU speeds up to 66 MHz.
- ☐ Low cost, low profile cardedge 178-pin module.
- ☐ Uses Burndy Computerbus™ Connector part number ELF182JSC-3Z50 (PDM4M6110) and ELF182KSC-3Z50 (PDM4M6111/6112).
- ☐ Multiple ground pins and decoupling capacitors for maximum noise immunity.
- ☐ Presence detect output pins allow the system to determine the particular cache configuration.

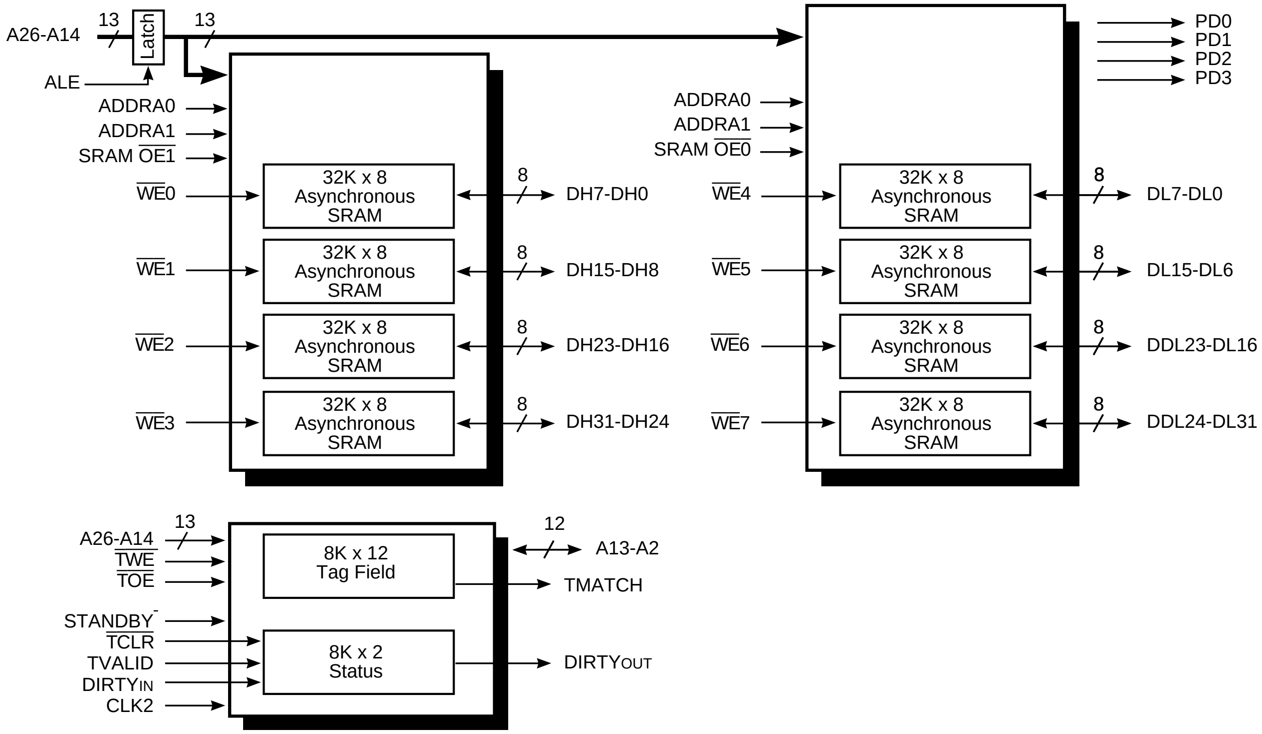
Description

The PDM4M6110/6111/6112 are high-performance CMOS static RAM modules designed for use as second level cache for PowerPC CPU-based systems. The PDM4M6110 is based on an asynchronous 32K x 8 static RAM and provides 256KB of second level cache. The PDM4M6111 and PDM4M6112 are based on 32K x 32 pipelined synchronous burst static RAMs providing 256KB and 512KB of second level cache, respectively. In addition, each of the modules are designed with 16K x 15 cache-tag static RAMs and on-board logic. The presence detect pins allow the system to determine the cache configuration.

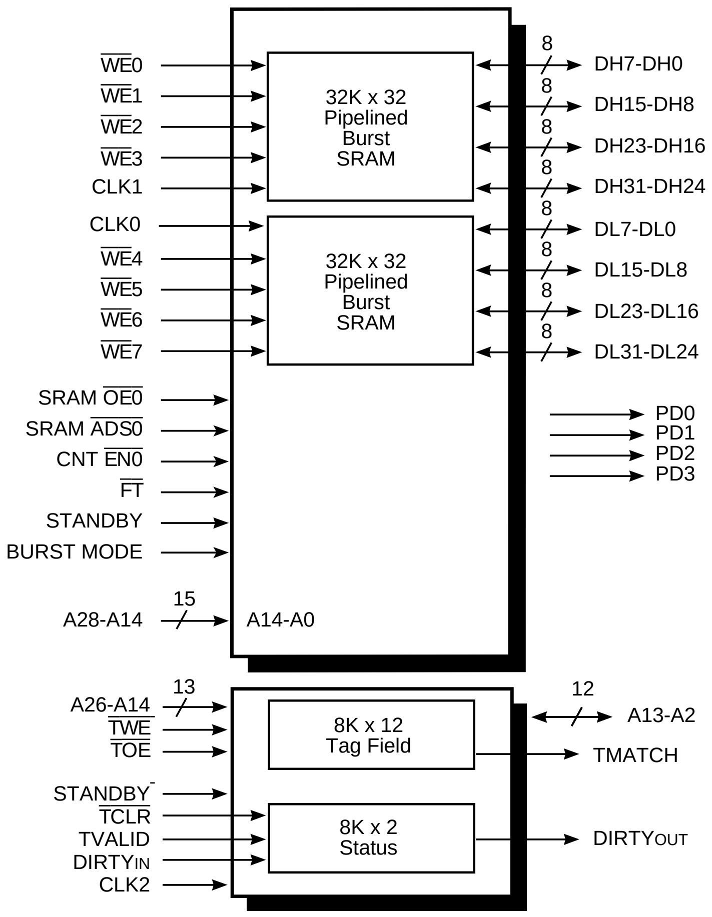
These modules are available in a 178-pin package. This low profile package allows for modules with a maximum height of 1.08", a maximum length of 5.06", and a maximum thickness of 0.250".

The modules operated from separate 5V (±5%) and 3.3V (±10%) power supplies. Multiple ground pins and decoupling capacitors ensure maximum protection from noise.

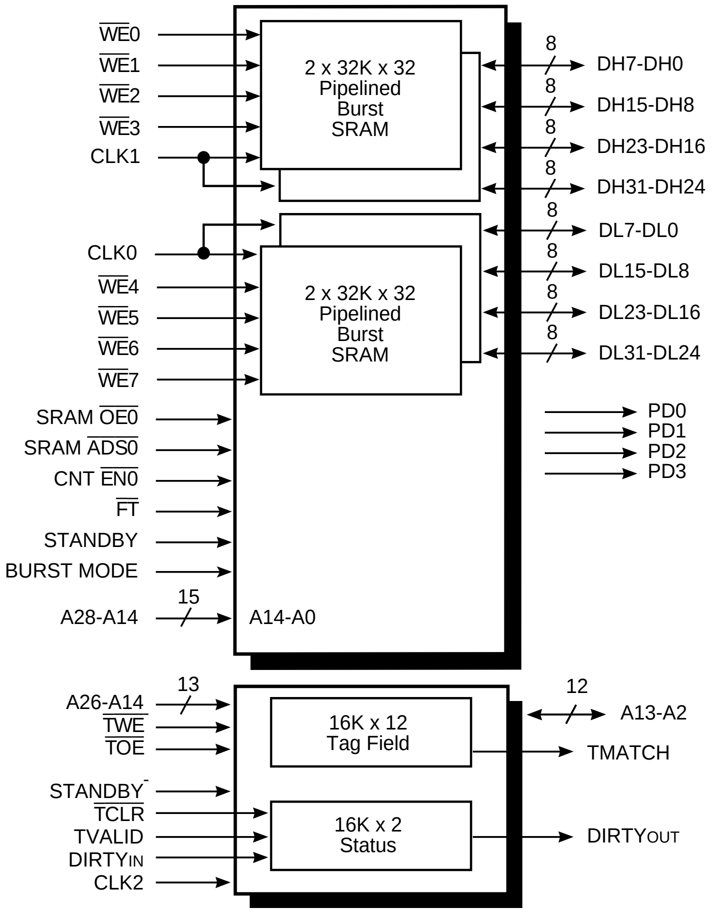
Functional Block Diagram
PDM4M6110 - 256KB Asynchronous Version



Functional Block Diagram PDM4M6111 - 256KB Pipelined Burst Version



Functional Block Diagram PDM4M6112 - 512KB Pipelined Burst Version



Presence Detection Code

Part No.	Description	PD3	PD2	PD1	PD0
	No Cache Present	NC	NC	NC	NC
PDM4M6110	256KB Asynchronous	NC	GND	GND	GND
PDM4M6111	256KB Pipelined Burst	GND	GND	NC	NC
PDM4M6112	512KB Pipelined Burst	GND	NC	NC	NC

SRAM Access Times

Module Speed	Asynch	Burst(1)	Tag
66 MHz	15 ns	8.5 ns	10 ns

NOTE: 1. Burst SRAMs are measured by Clock to Data Out.

PIN CONFIGURATION

Signal	Pin	Pin	Signal
VSS	90	1	VSS
PD1	91	2	PD0
PD3	92	3	PD2
DH31	93	4	DH30
DH29	94	5	DH28
DH27	95	6	DH26
DH25	96	7	DH24
VCC3	97	8	VCC3
SRAM WE3	98	9	DP3
DH23	99	10	DH22
DH21	100	11	DH20
DH18	101	12	DH19
VSS	102	13	VSS
DH16	103	14	DH17
SRAM WE2	104	15	DP2
DH14	105	16	DH15
DH13	106	17	DH12
VCC5	107	18	VCC5
DH10	108	19	DH11
DH8	109	20	DH9
SRAM WE1	110	21	DP1
DH6	111	22	DH7
VCC3	112	23	VCC3
DH4	113	24	DH5
VSS	114	25	DH3
CLK0	115	26	DH2
VSS	116	27	DH0
DH1	117	28	DP0
SRAM WE0	118	29	VSS
DL31	119	30	CLK1
DL30	120	31	VSS
VSS	121	32	DL28
DL29	122	33	DL26
DL27	123	34	DL24
DL25	124	35	DP7
VCC5	125	36	VCC5
SRAM WE7	126	37	DL22
DL23	127	38	DL20
DL21	128	39	DL18
DL19	129	40	DL16
VSS	130	41	VSS
DL17	131	42	DP6
SRAM WE6	132	43	DL14
DL15	133	44	DL12
DL13	134	45	DL11
VSS	135	46	VSS
DL10	136	47	DL9
DL8	137	48	DP5
SRAM WE5	138	49	DL7
DL6	139	50	DL4
VCC3	140	51	VCC3
DL5	141	52	DL3
DL2	142	53	DL1
VSS	143	54	DL0
CLK3	144	55	VSS
VSS	145	56	CLK2 (TAG)
CLK4	146	57	VSS
VSS	147	58	DP4
SRAM WE4	148	59	SRAM OE0
SRAM ALE	149	60	SRAM OE1
VCC3	150	61	VCC3
ADDR1	151	62	ADDR0
RES	152	63	RES
SRAM CNT EN0	153	64	SRAM ADS0
SRAM CNT EN1	154	65	SRAM ADS1
A27	155	66	A28
A24	156	67	A26
A22	157	68	A25
A20	158	69	A23
VSS	159	70	VSS
A18	160	71	A21
A16	161	72	A19
A15	162	73	A17
A14	163	74	A13
VCC3	164	75	VCC3
A10	165	76	A12
A8	166	77	A11
A6	167	78	A9
VSS	168	79	VSS
A4	169	80	A7
A2	170	81	A5
A1	171	82	A3
BURST MODE	172	83	A0
VCC5	173	84	VCC5
TAG VALID	174	85	TAG CLR
TAG WE	175	86	TAG MATCH
STANDBY	176	87	TAG OE
DIRTYOUT	177	88	DIRTYIN
VSS	178	89	VSS

Pin Names

Pin	Signal
A28-A0	Address Inputs
ADDR1-ADDR0	Address Inputs (6110 only)
CLK4-CLK0	Clock Inputs
DH31-DH0	High Order Cache Data
DL31-DL0	Low Order Cache Data
PD3-PD0	Presence Detect Pins
SRAM ADS0- SRAM ADS1	SRAM Address Strobe
SRAM ALE	SRAM Address Latch Enable
SRAM CNT EN0 SRAM CNT EN1	SRAM Control Enable
SRAM OE0 SRAM OE1	SRAM Output Enable
SRAM WE0 SRAM WE7	SRAM Write Enable
BURST MODE	Burst Mode: 0 = Linear, 1 = Interleaved
TAG CLR	Tag Clear
TAG MATCH	Tag Match
TAG VALID	Tag Valid
TAG OE	Tag Output Enable
TAG WE	Tag Write Enable
DIRTYIN	Dirty Input Bit
DIRTYOUT	Dirty Output Bit
STANDBY	Standby Mode
VCC3	3.3V Power Supply
VCC5	5.0V Power Supply
VSS	Ground

Absolute Maximum Ratings(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}	Terminal Voltage with Respect to V_{SS}	–0.5 to V_{CC} + 0.5	V
V_{TERM} for V_{CC3}	Terminal Voltage with Respect to V_{SS}	–0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC3}	Supply Voltage	3.0	3.3	3.6	V
V_{CC5}	Supply Voltage	4.75	5.0	5.25	V
V_{SS}	Supply Voltage	0	0	0.0	V
Commercial	Ambient Temperature	0	25	70	°C

PDM4M6110 Capacitance(1)

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max	Unit
C_{IN1}	Input Capacitance, V_{IN} = 0V (Address)	15	pF
C_{IN2}	Input Capacitance, V_{IN} = 0V (CA3-CA4)	25	pF
C_{IN3}	Input Capacitance, V_{IN} = 0V ($\overline{OE}$)	45	pF
C_{IN4}	Input Capacitance, V_{IN} = 0V ($\overline{WE}$, $\overline{TWE}$)	8	pF
CI/O	I/O Capacitance, V_{OUT} = 0V	10	pF

PDM4M6111/6112 Capacitance(1)

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max	Unit
C_{IN1}	Input Capacitance, V_{IN} = 0V (Address)	15/30	pF
C_{IN2}	Input Capacitance, V_{IN} = 0V (CA3-CA4)	—	pF
C_{IN3}	Input Capacitance, V_{IN} = 0V ($\overline{OE}$)	15/25	pF
C_{IN4}	Input Capacitance, V_{IN} = 0V ($\overline{WE}$, $\overline{TWE}$)	8	pF
CI/O	I/O Capacitance, V_{OUT} = 0V	10/20	pF

NOTE: 1. This parameter is determined by device characteristics but is not production tested.

DC Electrical Characteristics (V_{CC5} = 5.0V ± 5%, V_{CC3} = 3.3V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Conditions	Min.	6110 Max.	6111 Max.	6112 Max.	Unit
I_{LI}	Input Leakage Current (Address)	V_{CC} = MAX., V_{IN} = V_{SS} to V_{CC}	—	20	30	50	µA
I_{LI}	Input Leakage Current (Data and Control)	V_{CC} = MAX., V_{IN} = V_{SS} to V_{CC}	—	10	10	20	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	10	20	µA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CC} = Min.	—	0.4	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OL} = –4 mA, V_{CC} = Min.	2.4	—	—	—	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V_{CC} + 0.3	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		–0.5(1)	0.8	0.8	0.8	V

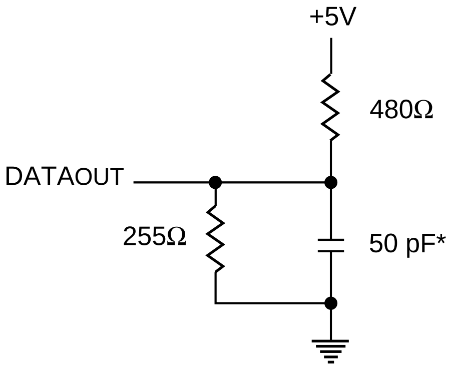
NOTE: 1. V_{IL} (Min.) = –3.0V for pulse widths less than 20 ns.

Power Supply Characteristics (V_{CC5} = 5.0V ± 5%, V_{CC3} = 3.3V ± 10%)

Symbol	Parameter	6110 Max.	6111 Max.	6112 Max.	Unit
I_{CC3}	Operating Current, 3.3V $\overline{CS} \leq V_{IL}$, V_{CC3} = Max., f = f_{MAX}, Outputs Open	1000	500	620	mA
I_{CC5}	Operating Current, 5V $\overline{CS} \leq V_{IL}$, V_{CC5} = Max., f = f_{MAX}, Outputs Open	180	180	180	mA
I_{SB3}	3.3V Standby Current, $\overline{CE} \geq V_{IH}$ f = f_{MAX}, Outputs Open	—	60	120	mA
I_{SB31}	Full 3.3V Standby Current, $\overline{CE} \geq V_{CC}$ – 0.2V, f = 0 $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V, Outputs Open	—	30	60	mA

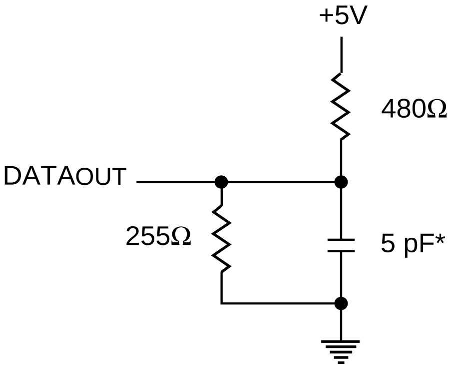
AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise/Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



* Including scope and jig capacitances

Figure 1. Output Load



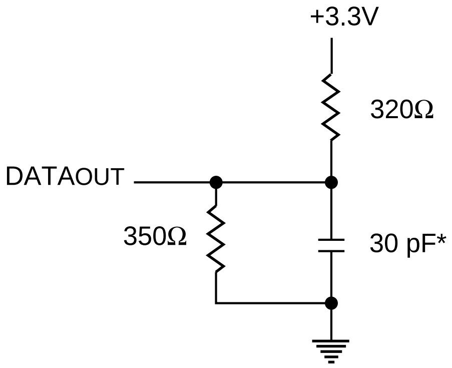
* Including scope and jig capacitances

Figure 2. Output Load

(for tOHZ, tCHZ, tOLZ, and tCLZ)

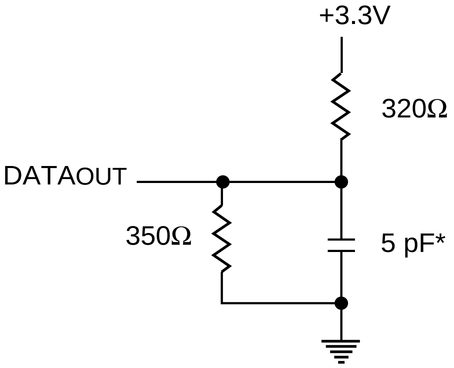
AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 3 and 4



* Including scope and jig capacitances

Figure 3. Output Load

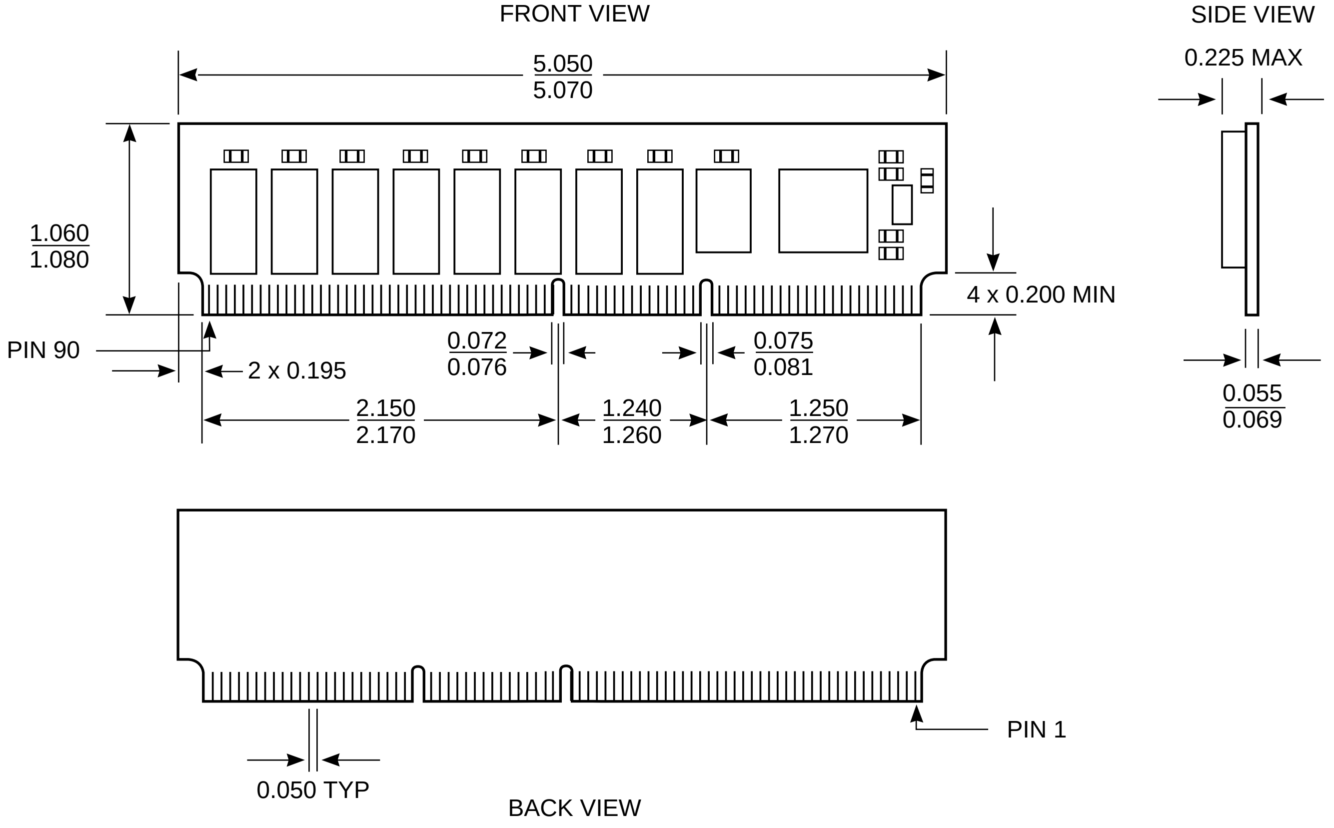


* Including scope and jig capacitances

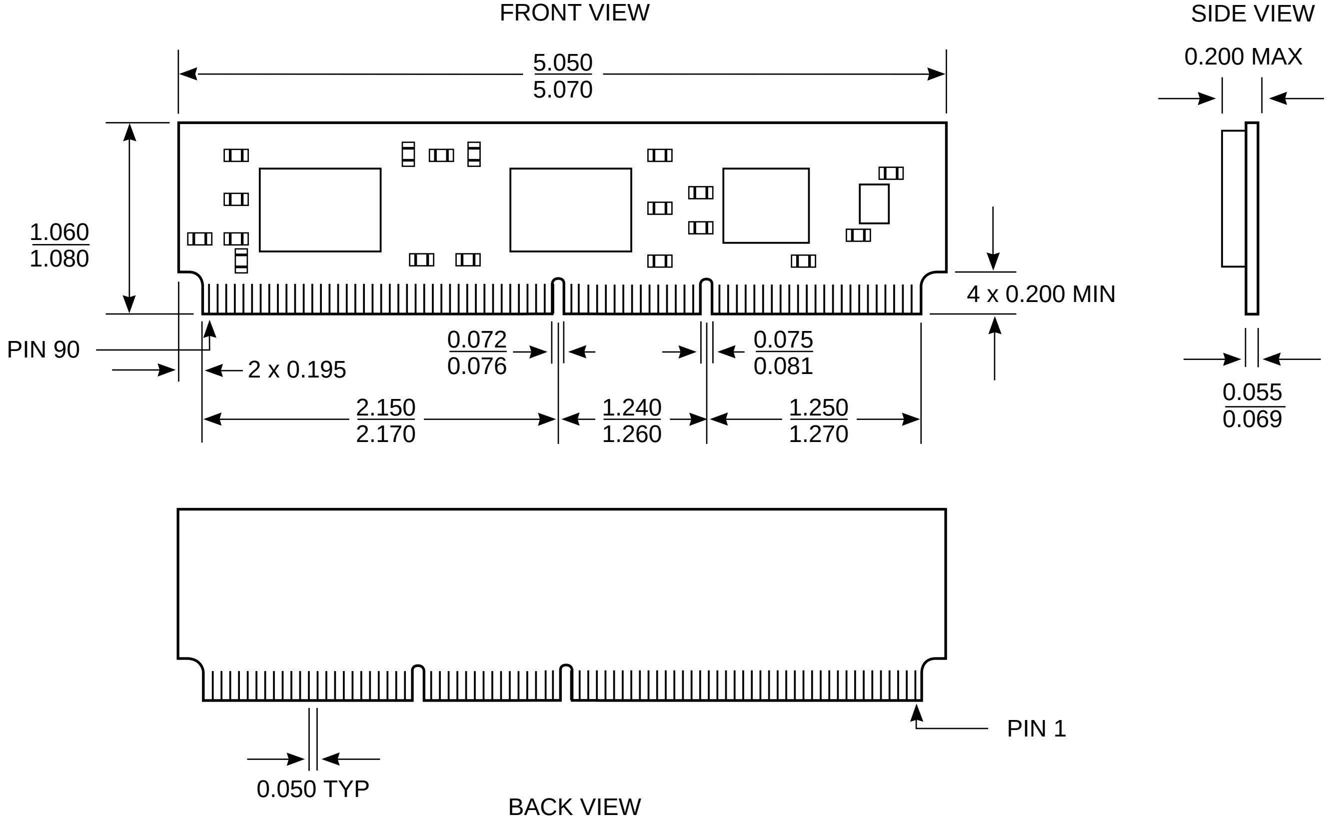
Figure 4. Output Load

(for tOHZ, tCHZ, tOLZ, and tCLZ)

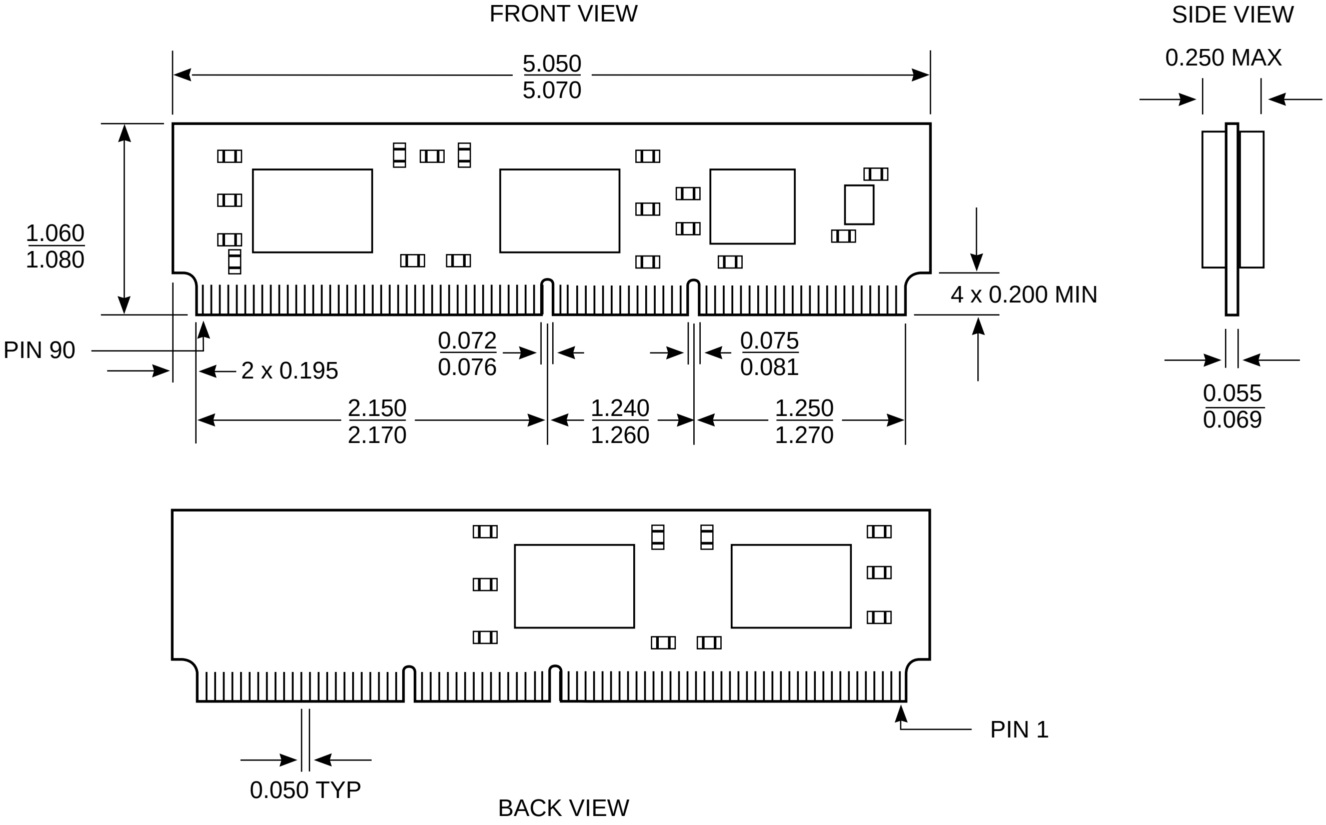
Package Dimensions
PDM4M6110



Package Dimensions
PDM4M6111



Package Dimensions
PDM4M6112



Ordering Information

PDM4M XXXXX X XX X X

Field	Code	Description
Process/ Temperature Range	Blank	Commercial (0°C to +70°C)
Package	M	178 lead Low Profile Module
Speed	15	Speed in nanoseconds
	66	Speed in Megahertz
Power	S	Standard Power
Device Type	6110	256KB Asynchronous Cache Module
	6111	256KB Pipelined Burst Cache Module
	6112	512KB Pipelined Burst Cache Module