



Dual 4 to 1 Multiplexer

**ELECTRICALLY TESTED PER:
5962-8750601**

The 10H574 is a Dual 4-to-1 Multiplexer. This device is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

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- Propagation Delay, 1.5 ns Typical
- 440 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V _{CC1}	1	5	2	GND
Q ₀	2	6	3	51 Ω to V _{TT}
DO ₀	3	7	4	OPEN
DO ₂	4	8	5	OPEN
DO ₁	5	9	7	GND
DO ₃	6	10	8	GND
A	7	11	9	GND
V _{EE}	8	12	10	V _{EE}
B	9	13	12	GND
D ₁₃	10	14	13	GND
D ₁₁	11	15	14	OPEN
D ₁₂	12	16	15	GND
D ₁₀	13	1	17	OPEN
Enable	14	2	18	OPEN
Q ₁	15	3	19	51 Ω to V _{TT}
V _{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

Military 10H574

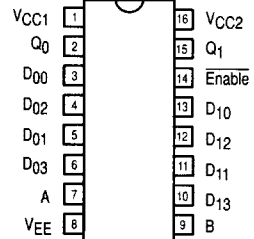


AVAILABLE AS

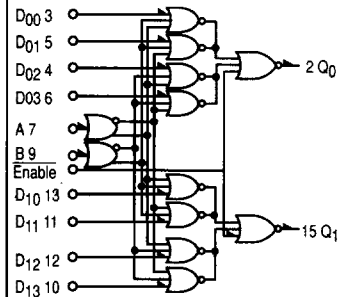
- 1) JAN: N/A
 - 2) SMD: 5962-8750601
 - 3) 883: 10H574/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



POSITIVE LOGIC DIAGRAM

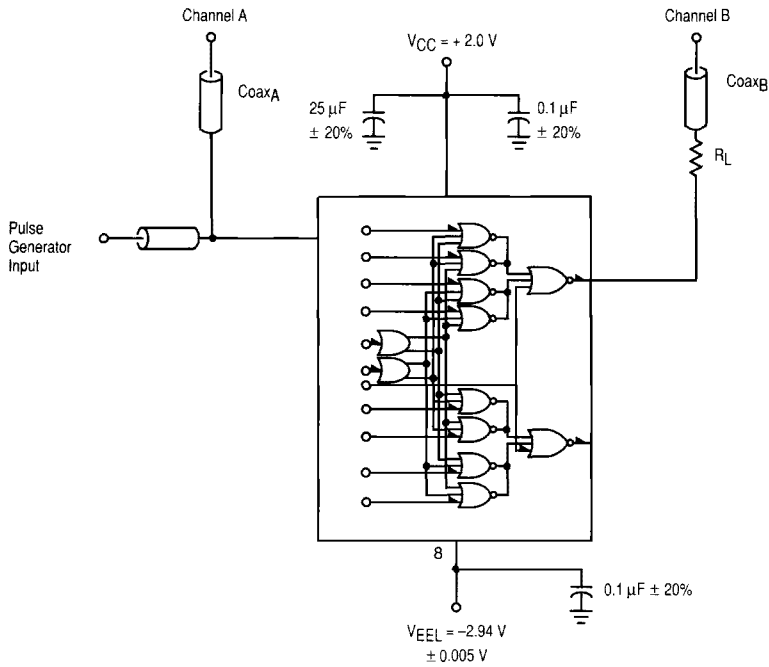


**10H574
TRUTH TABLE**

ENABLE	ADDRESS INPUTS		OUTPUTS	
\bar{E}	B	A	Q ₀	Q ₁
H	∅	∅	L	L
L	L	L	D ₀₀	D ₁₀
L	L	H	D ₀₁	D ₁₁
L	H	L	D ₀₂	D ₁₂
L	H	H	D ₀₃	D ₁₃

∅ = Don't Care

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NOTES

1. Unused outputs loaded 100 Ω to ground.
2. PRR = 1.0 MHz.
3. $t_r = t_f = 1.0 \text{ ns} \pm 0.1 \text{ ns}$ (20% - 80%).
4. $R_L = 50 \Omega$.
5. $P_W = 20 \text{ ns}$.

Figure 1. Switching Test Circuit

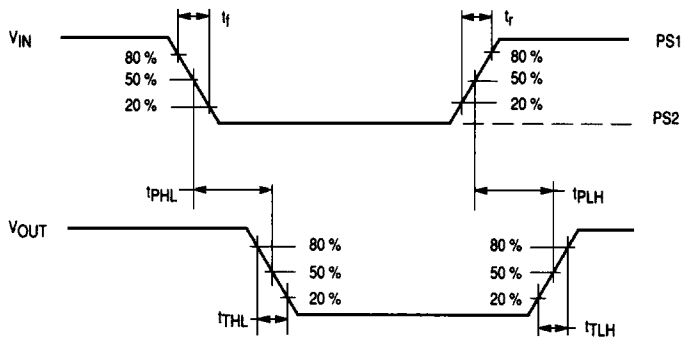


Figure 2. Switching Test Circuit Waveforms

10H574 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	PS1	PS2	VEE1	VEE2	VEE1	VEE2
T _A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-5.46	-2.94
T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-5.46	-2.94
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-5.46	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1 Min	Subgroup 1 Max	Subgroup 2 Min	Subgroup 2 Max	Subgroup 3 Min	Subgroup 3 Max		V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	V _{EE1}	V _{EE2}	V _{CC}	P.U.T.
V _{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3-7 9-14	7-9, 14		8		1, 16	2, 15	
V _{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	3-7, 9, 13, 14	3-7 9-14		8		1, 16	2, 15	
V _{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	7, 9, 14	7, 9, 14	3-7 9-13	8	8	1, 16	2-4 13-15	
V _{OH1}	High Output Voltage	-1.01	-0.78	-1.86	-0.65	-1.06	-0.84	V	3-7 9-13	3-7 9-13	7, 9, 14	8	8	1, 16	2, 15	
I _{IH}	Power Supply Current		300		475		475	μA	3-7 9-13			8		1, 16	3-7, 9-13	
I _{IH1}	Input Current High		420		670		670	μA	14			8		1, 16	14	
I _{IL}	Input Current Low	0.5		0.3		0.5		μA	3-7 9-14			8		1, 16	3-7, 9-14	
I _{EE}	Power Supply Drain Current	-73		-80		-80		mA				8		1, 16	8	

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Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	PS1	PS2	VEEL	VEE1	VEE2	
TA = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	
TA = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	
TA = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
		+25 °C		+125 °C		-55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9	Subgroup 10	Subgroup 11	Subgroup 9	Subgroup 10	Subgroup 11		V _{IN}	V _{OUT}	V _{CC}	VEEL	PS1	P.U.T.		
t _{TLH}	Rise Time	0.5	1.7	0.5	2.0	0.4	1.65	ns	3 - 7, 9 - 14	2, 15	1, 16	8	3 - 5, 9, 11 - 13	2, 15		
t _{FHL}	Fall Time	0.5	1.7	0.5	2.0	0.4	1.65	ns	3 - 7, 9 - 14	2, 15	1, 16	8	3 - 5, 9, 11 - 13	2, 15		
t _{PLH} t _{PHL}	Propagation Delay (A & B) note 1	1.2	2.9	1.5	3.6	1.1	2.75	ns	3 - 7, 9 - 14	2, 15	1, 16	8	3 - 5, 9, 11 - 13	2, 15		
t _{PLH} t _{PHL}	Propagation Delay (Data X & Y) note 2	1.0	2.4	1.0	2.9	0.8	2.25	ns	3 - 7, 9 - 14	2, 15	1, 16	8	3 - 5, 9, 11 - 13	2, 15		
t _{PLH} t _{PHL}	Propagation Delay (Enable) note 3	0.5	1.8	0.5	2.0	0.5	1.7	ns	3 - 7, 9 - 14	2, 15	1, 16	8	3 - 5, 9, 11 - 13	2, 15		

Notes

1. Pins 7, 9.
2. Pins 3 - 6, 10 - 13.
3. Pins 14.