IgT®

Integrated Telecom Technology, Inc.

ATM UPC/OAM Processor

WAC-186-B

User's Manual

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About this User's Manual

- This user's manual version (dated 07/22/97) replaces the last released version (dated 05/29/97).
- Refer to page 13 for a revision history of this document.
- A Non-Conformance Addendum (NCA) may exist for this device. Please consult IgT's home page for a list of available current documentation.

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DESCRIPTION

The ATM UPC/OAM Processor (WAC-186-B) checks incoming connections for violations of negotiated traffic parameters, and performs hardware-intensive processing of Operations, Administration, and Maintenance (OAM) cells. The WAC-186-B is ideally suited for equipment requiring enforcement of traffic parameters and extensive OAM capabilities, such as ATM switches, hubs, bridges, routers, and test equipment. IgT also offers the ATM UPC/OAM Processor Software Driver (WAC-186-DRV) for the WAC-186-B device.

FEATURES

UPC Features

- Processes incoming ATM cells for Usage Parameter Control (UPC) violations.
- Selectively discards cells in violation or tags cells in violation with Cell Loss Priority (CLP) = 1 on a per-connection basis.
- Provides dual Generic Cell Rate Algorithms (GCRAs) to monitor the following variables on a per-connection basis: Peak Cell Rate (PCR), Cell Delay Variation (CDV), Sustainable Cell Rate (SCR), and burst tolerance in compliance with the ATM Forum UNI 3.0. and 3.1 specifications, the ATM Forum Traffic Management 4.0 draft specification, and the ITU-I.371 Recommendation.
- Maintains the following counts per connection: total cells, CLP = 0 cells, OAM cells, and cells in violation.

OAM Features

- Provides OAM Performance Monitoring (PM) for selected connections as per ITU I.610 and Bellcore GR-1248-CORE.
- Generates OAM Alarm Indication Signal (AIS) cells, Remote Defect Indicator (RDI) and Continuity Check (CC) cells on a per-connection basis.
- Performs OAM loopback according to the ATM Forum UNI Specification 3.1.
- Provides a one-cell FIFO for insertion of user-specified OAM cells.
- Provides network delay measurement via OAM Loopback (LB) cells.

General Features

- Supports 1K, 4K, 8K, or 16K active channels from a possible 32K, 128K, 256K, or 512K connections (Virtual Path Identifier (VPI)/Virtual Channel Identifier (VCI) combination).
- Transfers cells through standard UTOPIA FIFO interfaces.
- Processes data at rates up to 250 Mbps.
- Contains a built-in 32-bit processor-to-memory interface.
- Provides built-in loopback capability.
- Provides outputs that can all be tristated.
- Provides boundary scan (JTAG).
- Available in a 208-pin PQFP package.

Figure 1 is a simple block diagram of the WAC-186-B.

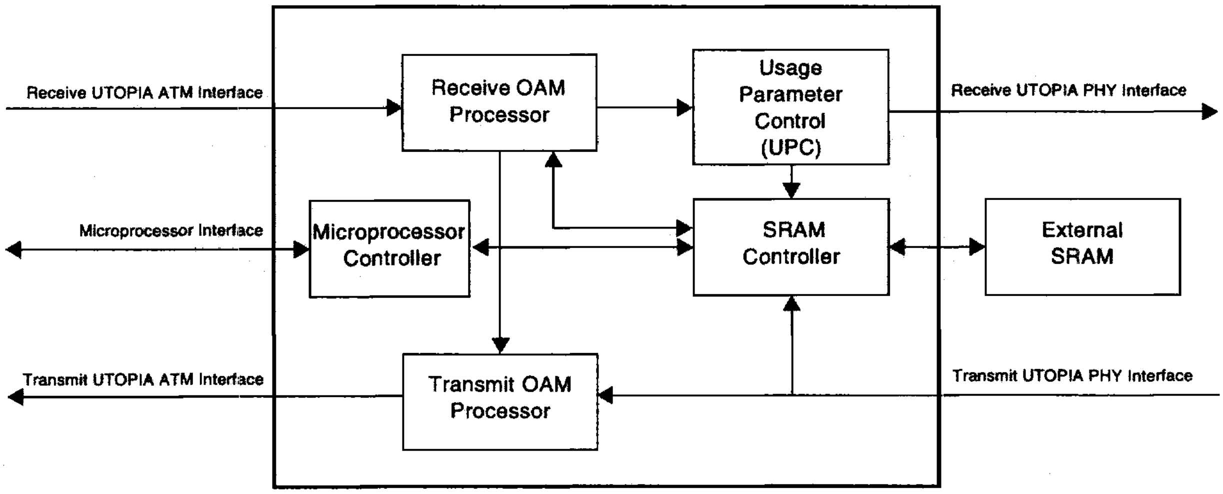


Figure 1. Simple Block Diagram of the WAC-186-B

What's New in this Manual

This revision history documents the ***major*** changes that occur from one manual version to the next version. Note that ***minor*** changes that occur from one version of the user's manual to the next version may ***not*** be listed in this revision history.

From Version	To Version	Major Changes
05/29/97	07/22/97	• In section 9.8.2 "Determining UPC Parameters" on page 87, corrected the equations for calculating the Peak Emission Interval T_{PCR} and the Cell Delay Variation τ_{SCR}.
03/03/97	05/29/97	• In section 8.2.2.1 "UPC_CONFIG" on page 62, changed the field description for the GCRA1_POLICE bit from "Police according to GCRA0 parameters" to "Police according to GCRA1 parameters".

12/17/96	03/03/97	• In Table 12 on page 29, changed the description of the VDD signal from "Supply voltage 5 ± 0.25 V" to "Supply voltage 5 ± 0.5 V".
		• In the description of "VPI_BITS" on page 49, changed the following:
		  • In the section "When the values for SRAM_CONFIG = 10b", for address 111b, removed "VCI(5:0)" and added "(VP-only mode)".
		  • In the section "When the values for SRAM_CONFIG = 11b", for address 111b, removed "VCI(6:0)" and added "(VP-only mode)".
		• In section 8.2.4.6 "BEDC" on page 70, changed the "Not used" bits from "31:15" to "31:16".

05/31/96	12/17/96	• Removed "OAM" from last bulleted item in section 2.2.1 "UPC Functions" on page 17.
		• In section 7.2.2 "GLOBAL_CONFIG" on page 48, expanded EXTENDED_LB description.
		• Added NOTEs to the descriptions of "UPC_VP_TERM" and "UPC_VC_TERM" on page 62.
		• Expanded function descriptions in the following sections:
		  • Section 8.2.5 "LB Control Block Summary" on page 75.
		  • Section 8.2.6.1 "VPI/VCI" on page 75.
		  • Section 8.2.6.2 "TX_TIME/CORR" on page 76.
		• Added a NOTE to section 9.11.5.1 "Source/Termination Point" on page 98.

ATM UPC/OAM Processor User's Manual

1 SYSTEM FEATURES

1.1 Clocks

- Fully static design allows operation at any frequency up to 33 MHz.
- Transmit and receive clocks are independent.

1.2 Test Loopback

- Allows receiver output data to be looped back to transmitter input data, a function commonly referred to as remote loopback.

1.3 Testability

- Provides outputs that are all tristatable.
- Provides JTAG interface.

1.4 Low Latency

- Latency from receiver input to receiver output is less than three cell times.
- Latency from transmitter input to transmitter output is less than three cell times.

1.5 VPI/VCI Mapping and Translation

- Supports 1K, 4K, 8K, or 16K active channels.
- Support for 1K active channels at 25 MHz requires a 32K × 32 20 ns SRAM bank; support for 4K active channels requires a 128K × 32 20 ns SRAM bank; support for 8K active channels requires a 256K × 32 20 ns SRAM bank; support for 16K active channels requires a 512K × 32 20 ns SRAM bank.
- Supports a VPI/VCI connection space 32 times larger than the number of active channels. Maps active connections into the available active channel space using a programmable lookup table. Channels at the beginning of the available active channel space are reserved for Virtual Path (VP) policing. The number of channels reserved equals the number of possible VPs. See Figure 1 for an example. If you assume seven VPI bits, the number of reserved channels for VP policing in the available active channel space would be 2^7, or 128.

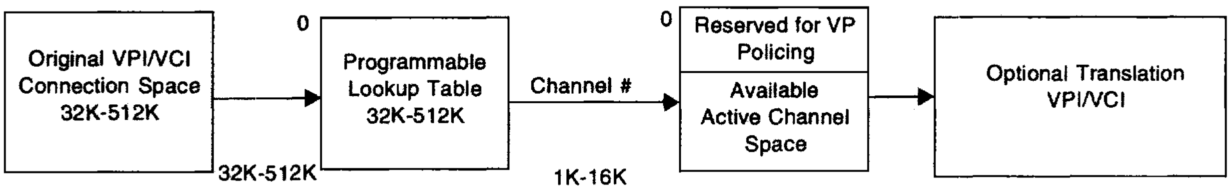


Figure 1. How the WAC-186-B Maps and Translates VPI/VCIs

- Supports five to eight active VPI bits, and 3 to 14 active VCI bits, with a maximum of 19 active bits. Or, supports 12 VPI bits, and zero to seven VC bits for Network Node Interface (NNI) support.
- Optionally translates incoming VPI/VCI to the active channel number, which is split between the VPI and VCI fields.

1.6 Network Configuration

- Supports configuration of network topology (segment point/end point or intermediate point) on a per-channel basis.

1.7 OAM Cell Format

Figure 2 displays the format of OAM cells.

Cell Header	OAM Type	Function Type	Function Specific Fields	Reserved	CRC-10
5 × 8	1 × 4	1 × 4	45 × 8	1 × 6	1 × 10

F4: VCI = 3 (Segment)
VCI = 4 (End-to-End)

F5: PTI = 100 (Segment)
PTI = 101 (End-to-End)

Figure 2. OAM Cell Format

Table 1 indicates the cell and function types of OAM cells. Throughout this manual, OAM cells are referred to by function type.

Table 1. OAM Type/Function Identifiers

OAM Cell Type	Value	OAM Function Type	Value
Fault Management	0001	AIS RDI Continuity Check OAM Cell Loopback	0000 0001 0100 1000
Performance Management	0010	Forward Monitoring Backward Reporting	0000 0001
Activation/Deactivation	1000	Performance Monitoring Continuity Check	0000 0001
User-User System Management	1111	Security System Setup Security System Maintenance	xxxx xxxx

Figure 3 displays the format of the function-specific fields of the AIS and RDI cells.

Defect Type (optional, not supported)	Defect Location (optional, not supported)	Not used
1 × 8	16 × 8	28 × 8

Figure 3. AIS/RDI OAM Cell-Specific Field Format

Figure 4 displays the format of the function-specific fields of the Loopback (LB) cell.

Loopback Indication	Correlation Tag	Loopback Location ID (optional)	Source ID (optional)	Not used
1 × 8	4 × 8	16 × 8	16 × 8	8 × 8

Figure 4. Loopback OAM Cell-Specific Field Format

Figure 5 displays the format of the function-specific fields of the PM cell.

MCSN	TUC_{0+1}	$BEDC_{0+1}$	TUC_0	TSTP (optional, not supported)	Not used	$TRCC_0$	$BLER_{0+1}$	$TRCC_{0+1}$
1 × 8	2 × 8	2 × 8	2 × 8	4 × 8	29 × 8	2 × 8	1 × 8	2 × 8

Figure 5. PM OAM Cell-Specific Field Format

2 THEORY OF OPERATIONS

2.1 Transmitter Features

2.1.1 OAM Functions

- Automatically generates and appends OAM Cyclic Redundancy Check-10 (CRC-10) to each OAM cell generated.
- Allows programmable F4/F5 (VP/VC) for each OAM cell per connection.
- Generates all OAM cells with CLP = 0.
- Schedules transmission of periodic AIS, RDI, and CC cells from a standard 8 kHz signal.
- Provides a one-cell FIFO for insertion of user-specified OAM cells.

2.1.1.1 Performance Monitoring (PM)

- Supports generation of forward monitoring or backward reporting cell types.
- Supports up to 32 simultaneous PM sessions.

2.1.1.1.1 Forward Monitoring

- Generates PM forward monitoring cells with all required fields, including:
  - An incrementing Monitoring Cell Sequence Number (MCSN).
  - Total User Cell (TUC) numbers for both CLP = 0 + 1 and CLP = 0.
  - Bit Interleave Parity-16 (BIP-16) code for CLP = 0 + 1.
- Supports block sizes of 128, 256, 512, and 1024 user cells.
- Waits for an idle cell slot before transmitting a cell, but optionally forces transmission of a cell when the block size is exceeded by 50 percent.

2.1.1.1.2 Backward Reporting

- Generates PM backward reporting cells with all required fields, including:
  - Block Error Result (BLER) as computed by the receiver.
  - TUC counts as received in the forward report (TUC_{0+1}, TUC_0).
  - Total Received Cell Counts (TRCCs) as computed by the receiver ($TRCC_{0+1}$, $TRCC_0$).

2.1.1.2 Fault Management

2.1.1.2.1 Alarm Generation

- Optionally generates end-to-end or segment F4/F5 OAM AIS cells once per second for each connection.

2.1.1.2.2 RDI Generation

- Automatically generates F4/F5 OAM RDI cells once per second for each connection on which the OAM AIS alarm is received.

2.1.1.2.3 Continuity Check (CC) Generation

- Optionally generates end-to-end or segment F4/F5 OAM CC cells once per second for each connection.

2.1.1.2.4 Loopback Generation

- Immediately transmits LB cells (with an LB indication of 01_h) that are provided by the receiver and changes the LB indication field to 00_h.
- Under software control, generates a forward LB cell with a programmable F4/F5 and Payload Type Indicator (PTI), an LB indication of 01_h, an optional LB ID, an optional source ID, and a Time Stamp (TS)-based correlation tag. Provides TS-based correlation tag to the receiver for the detection of the returning cell.
- Supports 32 simultaneous LB flows.
- Network timing may be calculated via the TS field in the OAM LB cell.

2.2 Receiver Features

2.2.1 UPC Functions

- Checks each incoming cell for violations of its negotiated traffic contract.
- Provides for specification of traffic contracts on a per-VCI or a per-VPI basis. Allows for specification of PCR, CDV, SCR, and burst tolerance.
- Provides two GCRAs for each VCI or VPI. These two GCRAs can be used to implement:
  - PCR for CLP = 0 + 1.
  - PCR for CLP = 0 + 1 and PCR for CLP = 0.
  - PCR for CLP = 0 + 1 and SCR for CLP = 0.
  - PCR for CLP = 0 + 1 and SCR for CLP = 0 + 1.
- Optionally checks CLP = 0 + 1 flows using the first GCRA. Violations are counted and are optionally tagged as CLP = 1 or discarded.
- Optionally checks either CLP = 0 + 1 or CLP = 0 flows using the second GCRA. Violations are counted and are optionally tagged as CLP = 1 or discarded.
- Maintains statistics per channel, including:
  - Cells dropped or tagged by GCRA0.
  - Cells dropped or tagged by GCRA1.
  - Total cells received.
  - Total OAM cells passed (OAM cells not terminated).
  - Total cells received with CLP = 0.

2.2.2 OAM Functions

- Detects whether an OAM cell has reached its termination point (the end point of the connection or segment). Processes the supported terminated OAM cells and removes them from the cell stream. Optionally removes the unsupported OAM cells and queues them to an external FIFO.
- Checks and validates the OAM CRC-10 for each OAM cell processed, and drops cells with invalid CRCs.
- Supports diverting OAM cells that are not explicitly supported by the WAC-186-B to an external FIFO.

2.2.2.1 Performance Monitoring (PM)

- Supports reception of forward monitoring or backward reporting cell types.
- Supports termination of either segment or end-to-end PM cells.
- Supports up to 32 PM sessions.
- Optionally supports data collection for each PM session.

2.2.2.1.1 Forward Monitoring

- Checks MCSN.
- Generates TRCC for the transmitter.
- Checks Block Error Detection Code$_{0+1}$ (BEDC$_{0+1}$) and generates a Block Error Result$_{0+1}$ (BLER$_{0+1}$) for the transmitter.
- Supports block sizes of 128, 256, 512, or 1024 user cells.

2.2.2.1.2 Backward Reporting

- Supports block sizes of 128, 256, 512, or 1024 user cells.

2.2.2.1.3 Data Collection

- Optionally performs the following on forward and/or backward reports:
  - Counts BLERs.
  - Counts lost cells.
  - Counts misinserted cells.
  - Counts Severely Errored Cell Blocks (SECBs). Provides programmable thresholds (1 to 16) for block errors, lost cells, and misinserted cells to determine a SECB condition.
  - Counts total transmitted user cells for both CLP = 0 and CLP = 0 or 1 flows.
  - Counts impaired PM blocks.
  - Counts total lost user information cells for both CLP = 0 and CLP = 0 or 1 flows.
  - Counts SECBs caused by errored cells.
  - Counts SECBs caused by misinserted cells.

2.2.2.2 Fault Management

2.2.2.2.1 Alarm Detection

- Detects F4/F5 OAM AIS cells and sets an AIS state indicator for the channel receiving AIS cells. Clears the AIS state indicator when a valid user cell is received, a CC cell is received, or when no AIS cell has been received for 2.5 ± .5 seconds. Optionally interrupts the WAC-186-B upon state transitions.

2.2.2.2.2 RDI Detection

- Detects F4/F5 OAM RDI cells and sets an RDI state indicator for the channel receiving RDI cells. Clears the RDI state indicator when no RDI cell has been received for 2.5 ± .5 seconds. Optionally interrupts the WAC-186-B upon state transitions.

2.2.2.2.3 CC Detection

- Optionally detects F4/F5 OAM CC cells and sets the Loss-Of-Continuity (LOC) state when no user cell or CC cell has been detected for 3.5 ± .5 seconds for each connection. Interrupts the WAC-186-B upon state transitions.

2.2.2.2.4 Loopback Detection

- Detects end-to-end or segment LB cells with LB indication fields equal to 01_h at their termination points (end/segment). Loops back these end-to-end or segment LB cells to the transmitter.
- Optionally terminates cells with matching source IDs or matching LB IDs.
- Supports looping back LB cells for all active connections.

- Detects returning LB cells; checks for match of VPI/VCI, PTI type, and the correlation tag to originating cell; stores current time; terminates the cell; and, optionally interrupts the processor.
- Supports 32 simultaneous returning LB cell detections.

3 PIN DESCRIPTIONS

3.1 Pin Function and Pin Count Summary

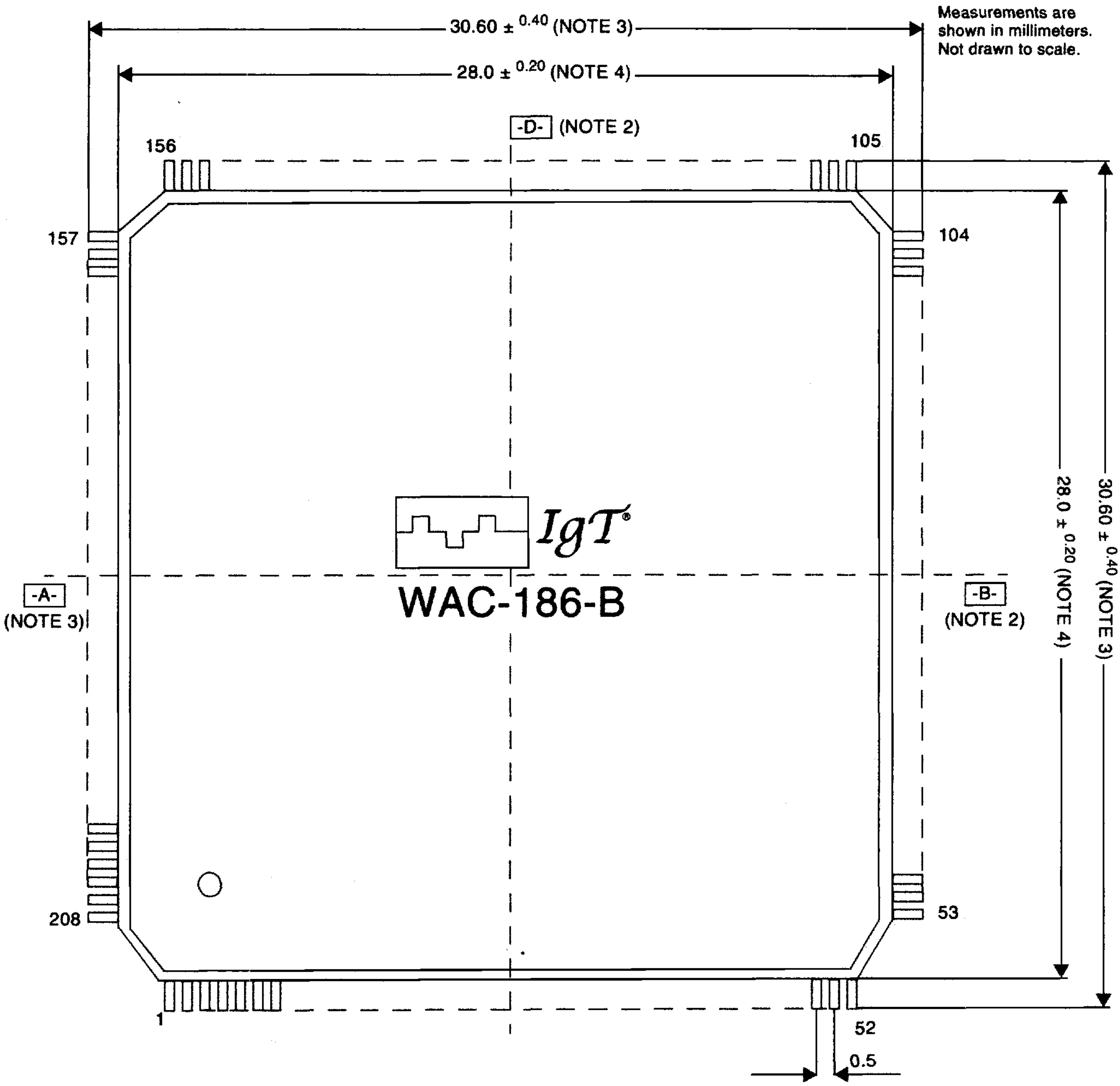
Table 2 summarizes the number of pins required by the WAC-186-B.

Table 2. Pin Function and Pin Count Summary

Pin Function	Pin Count
UTOPIA ATM Layer	24
UTOPIA PHY Layer	29
SRAM Port	54
Microprocessor Port	57
Power	30
Miscellaneous	14

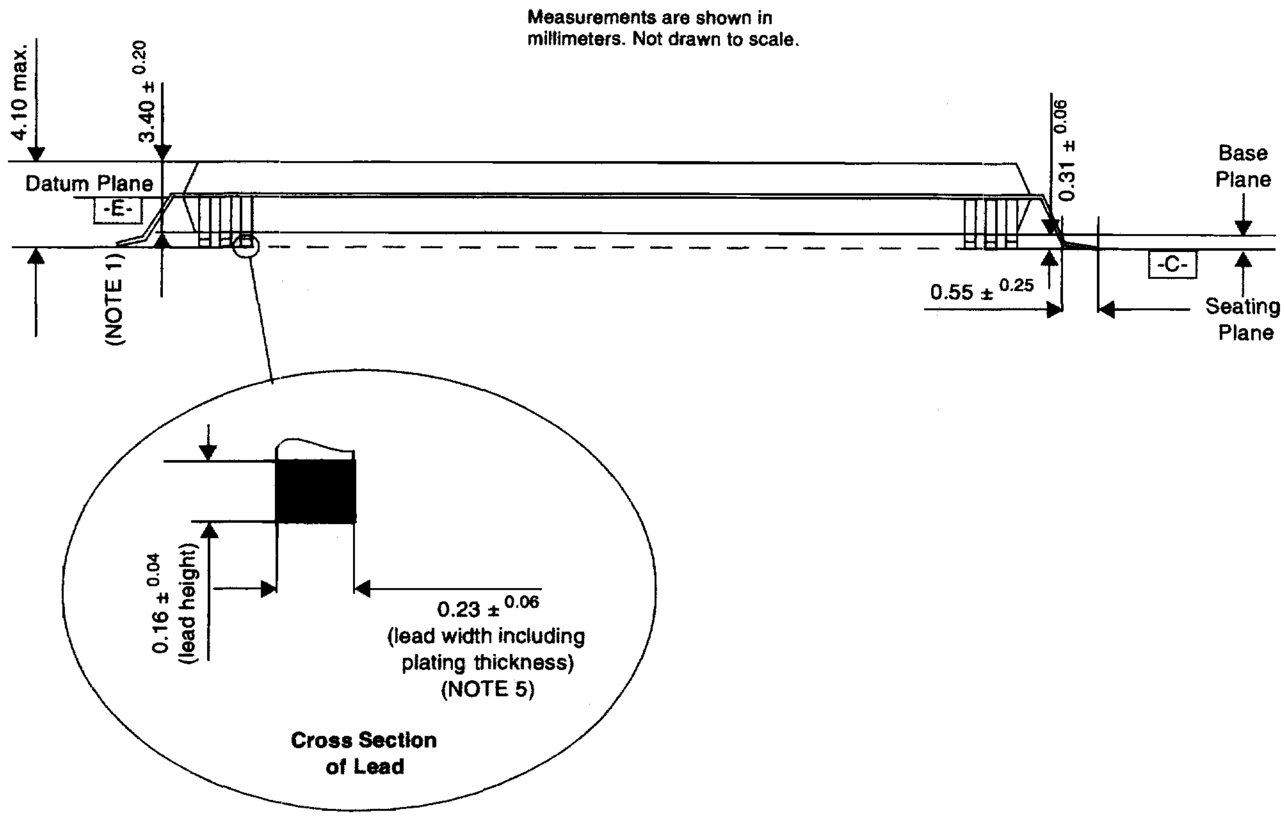
3.2 Package Diagram

Figure 6 (parts 1 and 2) shows the physical dimensions for the 208-pin Plastic Quad Flat Pack (PQFP) used for the WAC-186-B. The package measurements are shown in millimeters.



Refer to NOTES on the following page.

Figure 6. 208-Pin PQFP Physical Dimensions Diagram (Part 1 of 2)



NOTES:

1. Datum plane -E- is located at the mold parting line and is coincident with the bottom of the leads where the leads exit the plastic body.
2. Datums -A-, -B-, and -D- to be determined at datum plane -E-.
3. To be determined at seating plane -C-.
4. These dimensions do not include mold protrusion. Allowable protrusion is .25 mm per side. These dimensions do not include mold mismatch and are determined at datum plane -E-.
5. This dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be .08 mm total in excess of this dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum spacing between adjacent leads to be 0.07 mm.
6. Controlling dimension: millimeter.
7. If you need a measurement that is not shown in this figure, contact IgT.

Figure 6. 208-Pin PQFP Physical Dimensions Diagram (Part 2 of 2)

3.3 Pin Locations

Table 3. Pin Locations

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VDD	53	VDD	105	VDD	157	VDD
2	D(09)	54	/CS	106	RAM_ADD(18)	158	RAM_DATA(7)
3	D(10)	55	/RD	107	RAM_ADD(17)	159	RAM_DATA(6)
4	D(11)	56	/WR	108	RAM_ADD(16)	160	RAM_DATA(5)
5	D(12)	57	/ACK	109	RAM_ADD(15)	161	RAM_DATA(4)
6	D(13)	58	INTR	110	RAM_ADD(14)	162	RAM_DATA(3)
7	D(14)	59	GND	111	RAM_ADD(13)	163	RAM_DATA(2)
8	GND	60	TPHY_ADDR	112	RAM_ADD(12)	164	GND
9	D(15)	61	TPHY_TAG(1)	113	RAM_ADD(11)	165	RAM_DATA(1)
10	D(16)	62	TPHY_TAG(0)	114	RAM_ADD(10)	166	RAM_DATA(0)
11	D(17)	63	/TPHY_WRITE_EN	115	RAM_ADD(9)	167	RATM_SOC
12	D(18)	64	TPHY_SOC	116	RAM_ADD(8)	168	RATM_CLAV (/RATM_EMPTY)
13	D(19)	65	GND	117	GND	169	/RATM_READ_EN
14	D(20)	66	TPHY_CLAV	118	VDD	170	RATM_DATA(0)
15	GND	67	TPHY_DATA(7)	119	RAM_ADD(7)	171	GND
16	D(21)	68	TPHY_DATA(6)	120	RAM_ADD(6)	172	RATM_DATA(1)
17	D(22)	69	TPHY_DATA(5)	121	RAM_ADD(5)	173	RATM_DATA(2)
18	D(23)	70	TPHY_DATA(4)	122	RAM_ADD(4)	174	RATM_DATA(3)
19	D(24)	71	TPHY_DATA(3)	123	RAM_ADD(3)	175	RATM_DATA(4)
20	D(25)	72	TPHY_DATA(2)	124	RAM_ADD(2)	176	RATM_DATA(5)
21	GND	73	TPHY_DATA(1)	125	RAM_ADD(1)	177	RATM_DATA(6)
22	D(26)	74	TPHY_DATA(0)	126	RAM_ADD(0)	178	RATM_DATA(7)
23	D(27)	75	GND	127	RAM_DATA(31)	179	GND
24	D(28)	76	TPHY_CLK	128	RAM_DATA(30)	180	/RESET
25	D(29)	77	VDD	129	GND	181	VDD
26	VDD	78	RPHY_CLK	130	VDD	182	8_KHZ
27	GND	79	GND	131	RAM_DATA(29)	183	GND
28	D(30)	80	RPHY_DATA(7)	132	RAM_DATA(28)	184	TATM_DATA(0)
29	D(31)	81	RPHY_DATA(6)	133	RAM_DATA(27)	185	TATM_DATA(1)
30	A(0)	82	RPHY_DATA(5)	134	RAM_DATA(26)	186	TATM_DATA(2)
31	A(1)	83	RPHY_DATA(4)	135	RAM_DATA(25)	187	TATM_DATA(3)
32	A(2)	84	RPHY_DATA(3)	136	RAM_DATA(24)	188	TATM_DATA(4)
33	A(3)	85	RPHY_DATA(2)	137	GND	189	TATM_DATA(5)
34	A(4)	86	RPHY_DATA(1)	138	RAM_DATA(23)	190	TATM_DATA(6)
35	A(5)	87	GND	139	RAM_DATA(22)	191	TATM_DATA(7)
36	A(6)	88	RPHY_DATA(0)	140	RAM_DATA(21)	192	TATM_CLAV (/TATM_FULL)
37	GND	89	/RPHY_READ_EN	141	RAM_DATA(20)	193	GND
38	A(7)	90	RPHY_CLAV	142	RAM_DATA(19)	194	TATM_SOC
39	A(8)	91	RPHY_SOC	143	RAM_DATA(18)	195	/TATM_WRITE_EN
40	A(9)	92	RPHY_ADDR	144	VDD	196	TATM_TAG(0)
41	A(10)	93	RPHY_CLAV_OAM	145	RAM_DATA(17)	197	TATM_TAG(1)
42	A(11)	94	SCAN_TDI	146	RAM_DATA(16)	198	D(0)
43	A(12)	95	SCAN_TDO	147	GND	199	D(1)
44	A(13)	96	/SCAN_TRST	148	RAM_DATA(15)	200	GND
45	SCAN_EN	97	SCAN_TCLK	149	RAM_DATA(14)	201	D(2)
46	A(14)	98	SCAN_TMS	150	RAM_DATA(13)	202	D(3)
47	A(15)	99	GND	151	RAM_DATA(12)	203	D(4)
48	A(16)	100	OUTPUT_EN	152	RAM_DATA(11)	204	D(5)
49	A(17)	101	/RAM_CE	153	RAM_DATA(10)	205	D(6)
50	A(18)	102	/RAM_OE	154	RAM_DATA(9)	206	D(7)
51	A(19)	103	/RAM_WE	155	RAM_DATA(8)	207	D(8)
52	GND	104	GND	156	GND	208	GND

3.4 Pin Descriptions

3.4.1 UTOPIA PHY Layer Interface Signals

3.4.1.1 Transmit UTOPIA PHY Layer Interface Signals

Table 4. Transmit UTOPIA PHY Layer Interface Signals

Signal Name	Pin #	Type	Reset Value*	Description
TPHY_CLK	76	In	NA	*Transmit UTOPIA PHY Layer Clock* clocks the transmit portion of the device.
TPHY_DATA(7:0)	67-74	In	NA	*Transmit UTOPIA PHY Layer Data Bits 7 to 0* form the 8-bit ATM data byte that is written into the WAC-186-B.
TPHY_SOC	64	In	NA	*Transmit UTOPIA PHY Layer Start-Of-Cell* indicates that the data being written into the WAC-186-B is the first byte of the 53-byte ATM cell.
/TPHY_WRITE_EN	63	In	NA	*Transmit UTOPIA PHY Layer Write Enable* is an active low signal used to enable the writing of data into the WAC-186-B.
TPHY_CLAV	66	Out	Tristate	*Transmit UTOPIA PHY Layer Cell Available* is used to indicate that the WAC-186-B can accept a cell. In MPHY mode, this signal is tristate when TPHY_ADDR = 1.
TPHY_ADDR	60	In	NA	*Transmit UTOPIA PHY Layer Address* is used for selecting and polling when connecting to an ATM UTOPIA level 2 device (MPHY). The address of the WAC-186-B is fixed: 0 selected 1 not selected.
*Present only while /RESET is asserted.				

3.4.1.2 Receive UTOPIA PHY Layer Interface Signals

Table 5. Receive UTOPIA PHY Layer Interface Signals

Signal Name	Pin #	Type	Reset Value*	Description
RPHY_CLK	78	In	NA	*Receive UTOPIA PHY Layer Clock* clocks the receive portion of the WAC-186-B.
RPHY_DATA(7:1) RPHY_DATA(0)	80-86 88	Out	Tristate	*Receive UTOPIA PHY Layer Data Bits 7 to 0* form the 8-bit ATM data byte that is read from the WAC-186-B. In MPHY mode, this signal is tristate when RPHY_ADDR = 1. In SPHY mode, this signal is tristate when RPHY_DATA is not valid.

Table 5. Receive UTOPIA PHY Layer Interface Signals (Continued)

Signal Name	Pin #	Type	Reset Value*	Description
RPHY_CLAV	90	Out	Tristate	*Receive UTOPIA PHY Layer Cell Available* is used to indicate that the WAC-186-B has user cells to transfer. In MPHY mode, this signal is tristate when RPHY_ADDR = 1.
RPHY_CLAV_OAM	93	Out	0	*Receive UTOPIA PHY Layer Cell Available OAM* is used to indicate that the WAC-186-B has OAM cells to transfer. In MPHY mode, this signal is tristate when RPHY_ADDR = 1. Refer to section 9.3 "Using an External OAM FIFO with the WAC-186-B" on page 81.
RPHY_SOC	91	Out	Tristate	*Receive UTOPIA PHY Layer Start-Of-Cell* indicates that the data being read from the WAC-186-B is the first byte of the 53-byte ATM cell. In MPHY mode, this signal is tristate when RPHY_ADDR = 1. In SPHY mode, this signal is tristate when RPHY_DATA is not valid.
/RPHY_READ_EN	89	In	NA	*Receive UTOPIA PHY Layer Read Enable* is an active low signal used to indicate that the ATM layer is reading data from the WAC-186-B.
RPHY_ADDR	92	In	NA	*Receive UTOPIA PHY Layer Address* is used for selecting and polling when connecting to a ATM UTOPIA Level 2 device (MPHY). The address of the WAC-186-B is fixed: 0 Selected 1 Not selected.
*Present only while /RESET is asserted.				

3.4.1.3 Multipriority Extension to UTOPIA Interface PHY Layer Signal

Table 6. Multipriority Extension to UTOPIA Interface PHY Layer Signal

Signal Name	Pin #	Type	Reset Value*	Description
TPHY_TAG(1:0)	61-62	In	NA	*Transmit UTOPIA PHY Layer Tags 1 and 0* form a 2-bit tag that is written into the WAC-186-B. This tag is transported with the cell, but is not used by the WAC-186-B. These pins may be pulled up if the WAC-185 is not being used.
*Present only while /RESET is asserted.				

3.4.2 UTOPIA ATM Layer Interface Signals

3.4.2.1 Transmit UTOPIA ATM Layer Interface Signals

Table 7. Transmit UTOPIA ATM Layer Interface Signals

Signal Name	Pin #	Type	Reset Value*	Description
TATM_DATA(7:0)	191-184	Out	00	*Transmit UTOPIA ATM Layer Data Bits 7 to 0* form the 8-bit ATM data byte that is written into the physical (PHY) layer device.
TATM_SOC	194	Out	0	*Transmit UTOPIA ATM Layer Start-Of-Cell* indicates that the data being written into the PHY layer device is the first byte of the 53-byte ATM cell.
TATM_CLAV (/TATM_FULL)	192	In	NA	*Transmit UTOPIA ATM Layer Cell Available* is an active high signal used to indicate that the PHY device has space available for a cell transfer. *Transmit UTOPIA ATM Layer Full* is an active low signal indicating that at most four more bytes can be received. The WAC-186-B reacts to this signal in Single-PHY (SPHY) mode, allowing direct connection to UTOPIA octet devices.
/TATM_WRITE_EN	195	Out	1	*Transmit UTOPIA ATM Layer Write Enable* is an active low signal that enables writing data into the PHY layer device.
*Present only while /RESET is asserted.				

3.4.2.2 Receive UTOPIA ATM Layer Interface Signals

Table 8. Receive UTOPIA ATM Layer Interface Signals

Signal Name	Pin #	Type	Reset Value*	Description
RATM_DATA(7:1) RATM_DATA(0)	178-172 170	In	NA	*Receive UTOPIA ATM Layer Data Bits 7 to 0* form the 8-bit ATM data byte to be written into the receiver.
RATM_SOC	167	In	NA	*Receive UTOPIA ATM Layer Start-Of-Cell* indicates that the data to be written into the receiver is the first byte of the 53-byte ATM cell.
RATM_CLAV (/RATM_EMPTY)	168	In	NA	*Receive UTOPIA ATM Layer Cell Available* is an active high signal used to indicate that the PHY layer device has a cell available for transfer. *Receive UTOPIA ATM Layer Empty* is an active low signal indicating that no more data is available. The WAC-186-B reacts to this signal, allowing direct connection to UTOPIA octet devices.
/RATM_READ_EN	169	Out	0	*Receive UTOPIA ATM Layer Read Enable* is an active low signal used to enable the writing of data from the PHY layer device into the WAC-186-B. In MPHY mode, this signal is tristatable when RPHY_ADDR = 1.
*Present only while /RESET is asserted.				

3.4.2.3 Multipriority Extension to UTOPIA Interface ATM Layer Signal

Table 9. Multipriority Extension to UTOPIA Interface ATM Layer Signal

Signal Name	Pin #	Type	Reset Value*	Description
TATM_TAG(1:0)	197-196	Out	0	*Transmit UTOPIA ATM Layer Tags 1 to 0*-form the 2-bit tag being written into the PHY layer device. These pins may be unconnected if the WAC-185 is not used.
*Present only while /RESET is asserted.				

3.4.3 Microprocessor Interface Signals

Table 10. Microprocessor Interface Signals

Signal Name	Pin #	Type	Reset Value*	Description
/CS	54	In	NA	*Chip Select* is an active low signal used to select the device.
/RD	55	In	NA	*Read* is an active low read signal from the external microprocessor.
/WR	56	In	NA	*Write* is an active low write signal from the external microprocessor.

Table 10. Microprocessor Interface Signals (Continued)

Signal Name	Pin #	Type	Reset Value*	Description
/ACK	57	Out	1	*Acknowledge* is an active low signal to indicate that the WAC-186-B has completed a write operation or that data is available on a read operation.
D(31:30) D(29:26) D(25:21) D(20:15) D(14:9) D(8:2) D(1:0)	29-28 25-22 20-16 14-9 7-2 207-201 199-198	Bi	Tristate	*Data Bits 31 to 0* form the 32-bit microprocessor data bus.
A(19:14) A(13:7) A(6:0)	51-46 44-38 36-30	In	NA	*Address Bits 19 to 0* form the 20-bit microprocessor address bus.
INTR	58	Out	0	*Interrupt* goes high when an alarm condition is detected. Each alarm condition is independently maskable. *Interrupt* goes low after the INTR port is read.
*Present only while /RESET is asserted.				

3.4.4 RAM Interface Signals

Table 11. RAM Interface Signals

Signal Name	Pin #	Type	Reset Value*	Description
RAM_ADD(18:8) RAM_ADD(7:0)	106-116 119-126	Out	0	*RAM Address Bits 18 to 0* form the 19-bit SRAM address bus. Refer to section 9.2 "SRAM Memory Interface" on page 80 for the bits to use for different memory configurations.
RAM_DATA(31:30) RAM_DATA(29:24) RAM_DATA(23:18) RAM_DATA(17:16) RAM_DATA(15:8) RAM_DATA(7:2) RAM_DATA(1:0)	127-128 131-136 138-143 145-146 148-155 158-163 165-166	Bi	Tristate	*RAM Data Bits 31 to 0* form the 16-bit SRAM data bus.
/RAM_OE	102	Out	1	*RAM Output Enable* is an active low signal used to enable the drivers on the RAM.
/RAM_WE	103	Out	1	*RAM Write Enable* is an active low signal used to perform a write to the RAM.
/RAM_CE	101	Out	1	*RAM Chip Enable* is an active low signal used to enable the RAM for a read or write operation.
*Present only while /RESET is asserted.				

3.4.5 Miscellaneous Signals

Table 12. Miscellaneous Signals

Signal Name	Pin #	Type	Reset Value*	Description
/RESET	180	In	NA	*Reset* re-initializes the device.
SCAN_TCLK	97	In	NA	*Scan Test Clock* is an independent clock used to drive the internal boundary scan test logic. When not using boundary scan, this signal should be connected to +5 V through a pull-up resistor.
SCAN_TMS	98	In	NA	*Scan Test Mode Select* controls the operation of the internal boundary scan test logic. When not using boundary scan, this signal should be connected to +5 V through a pull-up resistor.
SCAN_TDI	94	In	NA	*Scan Test Data Input* is the serial input for boundary scan test data and instruction bits. When not using boundary scan, this signal should be connected to +5 V through a pull-up resistor.
SCAN_TDO	95	Out	Tristate	*Scan Test Data Output* is the serial output for boundary scan test data.
/SCAN_TRST	96	In	NA	*Scan Test Reset* is an active low signal used to reset the internal boundary scan test logic. When not using boundary scan, this signal should be connected to 0 V to place all boundary scan logic in reset.
OUTPUT_EN	100	In	NA	*Output Enable* is an active high signal used to enable all output signals. A low on this signal forces all output pins into a high impedance state.
8_KHZ	182	In	NA	*8_KHZ* is an active high clock signal used for real-time based operations. This signal may be connected to an 8 KHz frame pulse that is sourced by many PHY layer devices.
SCAN_EN	45	In	NA	*Scan Enable* is used for manufacturing testing purposes only. Connect this signal to 0 volts.
VDD	1, 26, 53, 77, 105, 118, 130, 144, 157, 181	In	NA	Supply voltage 5 ± 0.5 V.
GND	8, 15, 21, 27, 37, 52, 59, 65, 75, 79, 87, 99, 104, 117, 129, 137, 147, 156, 164, 171, 179, 183, 193, 200, 208	In	NA	Ground.

*Present only while /RESET is asserted.

4 PHYSICAL CHARACTERISTICS

Table 13. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND.	-0.3	7.0	V
I_{OUT}	DC output current, per pin		-4	4	mA
T_{STG}	Storage temperature		-65	150	°C

Table 14. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.50	5.50	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature		-40	85	°C
t_R	Input rise time			10	ns
t_F	Input fall time			10	ns

Table 15. DC Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ITH}	High-level TTL input voltage	All TTL clocks and scan signals	2.0			V
V_{ITL}	Low-level TTL input voltage	All TTL clocks and scan signals			0.8	V
V_{ISH}	High-level Schmitt-triggered TTL input voltage	All TTL inputs except clocks and scan signals	2.25			V
V_{ISL}	Low-level Schmitt-triggered TTL input voltage	All TTL inputs except clocks and scan signals			0.8	V
V_{IHys}	Hysteresis Schmitt-triggered TTL input voltage	All TTL inputs except clocks and scan signals	0.4	0.8		V
V_{OH}	TTL high-level output voltage	I_{OH} = -4 mA DC	2.4			V
V_{OL}	TTL low-level output voltage	I_{OL} = 4 mA DC			0.4	V
I_{TYP}	Typical operating current	RPHY_CLK and TPHY_CLK = 25 MHz		200		mA
NOTES: • V_{CC}= 5 V ± 10%, T_A = -40°C to 85°C for industrial use. • Typical values are T_A = 25°C and V_{CC} = 5 V.						

Table 16. Capacitance

Symbol	Parameter	Conditions	Min	Max	Uni
C_{IN}	Input capacitance			10	pF
C_{OUT}	Output capacitance			6	pF
C_{LOAD}	Load capacitance	To meet timing on all signals except RAM_ADD.		30	pF
C_{LOAD}	Load capacitance	To meet timing on RAM_ADD.		50	pF
NOTES: • Capacitance measured at 25°C. • Sample tested only.					

5 TIMING DIAGRAMS

All pin names are described in section 3 "Pin Descriptions" on page 20. Unless otherwise indicated, all output timing delays assume a capacitive loading of 30 pF.

5.1 ATM UTOPIA Timing

The ATM UTOPIA interface works in the octet-level handshaking mode (refer to Appendix B, "References", on page 108 for information on the UTOPIA specifications). Because it responds to the cell available signal supplied by the PHY layer device in an octet-by-octet manner, the WAC-186-B is also compatible with cell-level handshaking UTOPIA devices. Since the WAC-186-B has two UTOPIA interfaces, the clock from the PHY UTOPIA interface is used by the ATM UTOPIA interface. The WAC-186-B asserts /TATM_WRITE_EN only when a full cell is available for transmission, and asserts /RATM_READ_EN only when space for a full cell is available.

Table 17. Transmit Signal Names and Their Corresponding UTOPIA Designations

Signal Name	UTOPIA Name
TATM_DATA	TxData
TATM_SOC	TxSOC
/TATM_WRITE_EN	TxEnb*
TATM_CLAV (/TATM_FULL)	TxFull*/TxClav
TPHY_CLK	TxClk
Not available	TxRef*
Not available	TxPrty
RATM_DATA	RxData
RATM_SOC	RxSOC
/RATM_READ_EN	RxEnb*
RATM_CLAV (/RATM_EMPTY)	RxEmpty*/RxClav
RPHY_CLK	RxClk
Not available	RxRef*
Not available	RxPrty

5.1.1 Transmit ATM UTOPIA Timing

Figure 7 shows the transmit ATM UTOPIA timing.

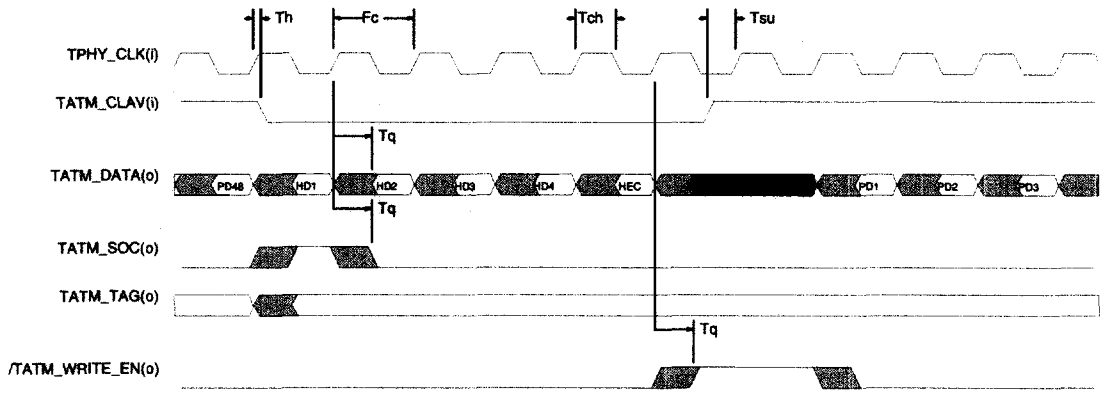


Figure 7. Transmit ATM UTOPIA Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	TPHY_CLK frequency			33	
Tch	TPHY_CLK duty cycle		45	55	%
Tsu	TPHY_CLK setup time	TATM_CLAV	8		ns
Th	TPHY_CLK hold time	TATM_CLAV	1		n
Tq	TPHY_CLK to output delay	TATM_DATA, TATM_SOC, /TATM_WRITE_EN, TATM_TAG	1	18	ns

Symbol	Definition
HD1 to HD4	1st to 4th header bytes
HEC	Header error check filler byte
PD1 to PD3	1st to 3rd payload bytes
PD48	48th payload byte

5.1.2 Receive ATM UTOPIA Timing

Figure 8 shows the receive ATM UTOPIA timing.

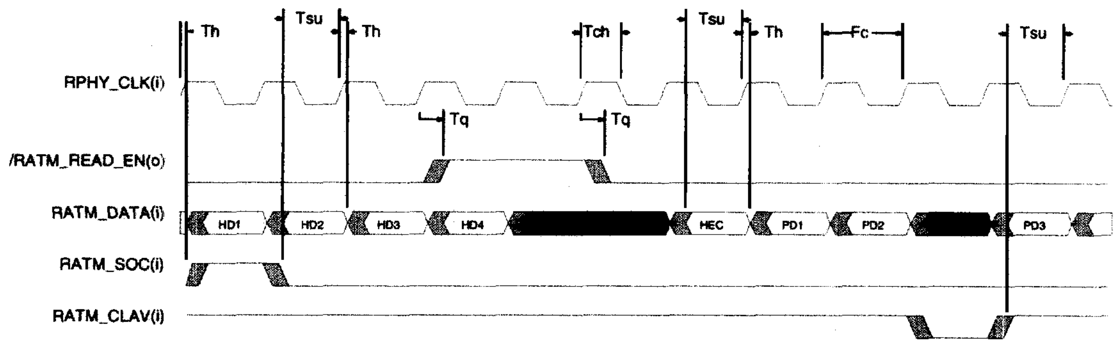


Figure 8. Receive ATM Interface Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	RPHY_CLK frequency			33	MHz
Tch	RPHY_CLK duty cycle		45	55	%
Tsu	RPHY_CLK setup time	RATM_DATA, RATM_SOC, RATM_CLAV	8		ns
Th	RPHY_CLK hold time	RATM_DATA, RATM_SOC, RATM_CLAV	1		ns
Tq	RPHY_CLK to output delay	/RATM_READ_EN		18	ns

Symbol	Definition
HD1 to HD4	1st to 4th header bytes
HEC	Header error check filler byte
PD1 to PD3	1st to 3rd payload bytes

5.2 PHY Timing

The PHY UTOPIA interface has two modes of operation: UTOPIA Level 1-compatible or UTOPIA Level 2-compatible (refer to Appendix B, "References", on page 108). For UTOPIA Level 1 compatibility, the device supports cell-level handshaking. In this mode, the WAC-186-B asserts TPHY_CLAV only when space for a full cell is available and asserts RPHY_CLAV only when a full cell is available. These signals remain asserted until the end of the cell (four bytes before the last byte for TPHY_CLAV, the last byte for RPHY_CLAV) providing capability to octet-level handshaking ATM devices. For UTOPIA Level 2 compatibility, the device responds to polling cycles and device selection.

Table 18. Transmit Signal Names and Their Corresponding UTOPIA Designations

Signal Name	UTOPIA Name
TPHY_DATA	TxData
TPHY_SOC	TxSOC
/TPHY_WRITE_EN	TxEnb*
TPHY_CLAV (/TPHY_FULL)	TxFull*/TxClav
TPHY_CLK	TxClk
Not available	TxRef*
Not available	TxPrty
RPHY_DATA	RxData
RPHY_SOC	RxSOC
/RPHY_READ_EN	RxEnb*
RPHY_CLAV (/RPHY_EMPTY)	RxEmpty*/RxClav
RPHY_CLK	RxClk
Not available	RxRef*
Not available	RxPrty

5.2.1 Transmit PHY UTOPIA Timing

Figure 9 shows the transmit SPHY interface timing.

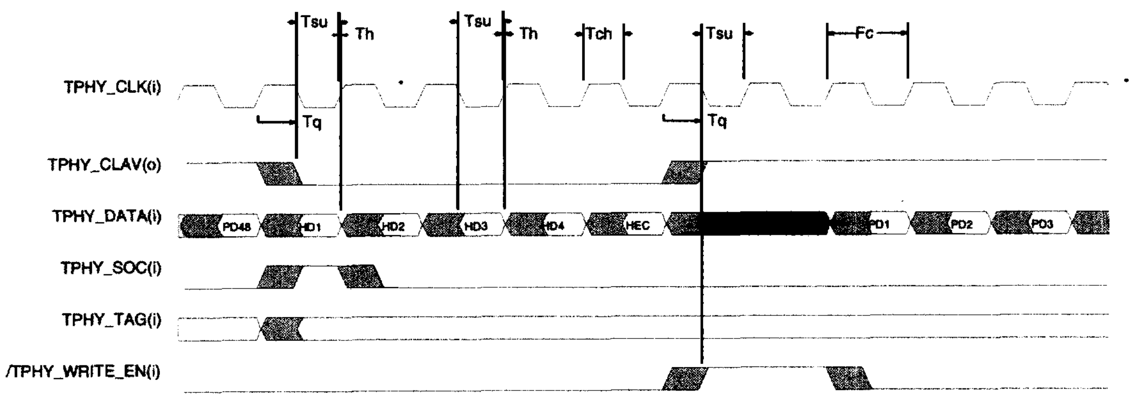


Figure 9. Transmit SPHY Interface Timing

Figure 10 shows the transmit MPHY interface timing.

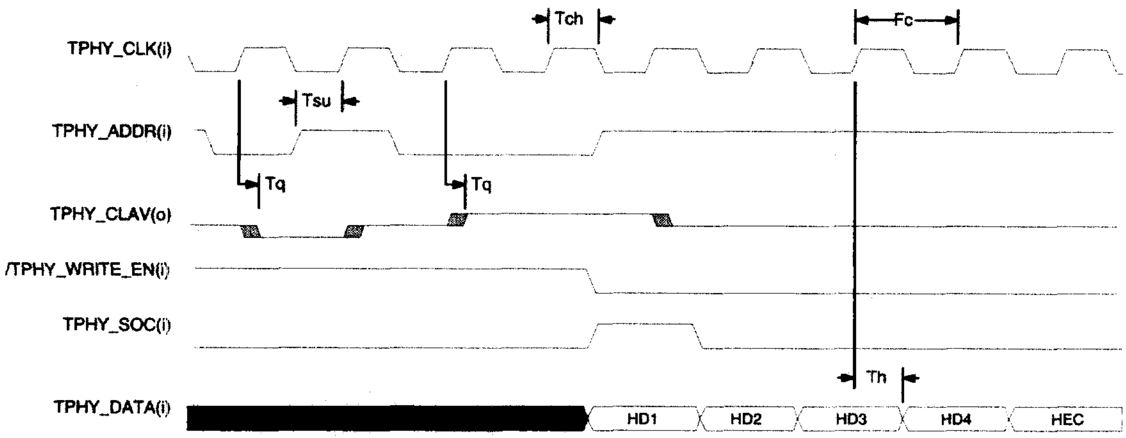


Figure 10. Transmit MPHY UTOPIA Interface Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	TPHY_CLK frequency			33	MHz
Tch	TPHY_CLK duty cycle		45	55	%
Tsu	TPHY_CLK setup time	/TPHY_WRITE_EN, TPHY_DATA, TPHY_SOC, TPHY_TAG, TPHY_ADDR	8		ns
Th	TPHY_CLK hold time	/TPHY_WRITE_EN, TPHY_DATA, TPHY_SOC, TPHY_TAG	1		ns
Tq	TPHY_CLK to output delay	TPHY_CLAV	1	18	ns

Symbol	Definition
HD1 to HD4	1st to 4th header bytes
HEC	Header error check filler byte
PD1 to PD3	1st to 3rd payload bytes
PD48	48th payload byte

5.2.2 Receive PHY UTOPIA Timing

Figure 11 shows the receive SPHY interface timing.

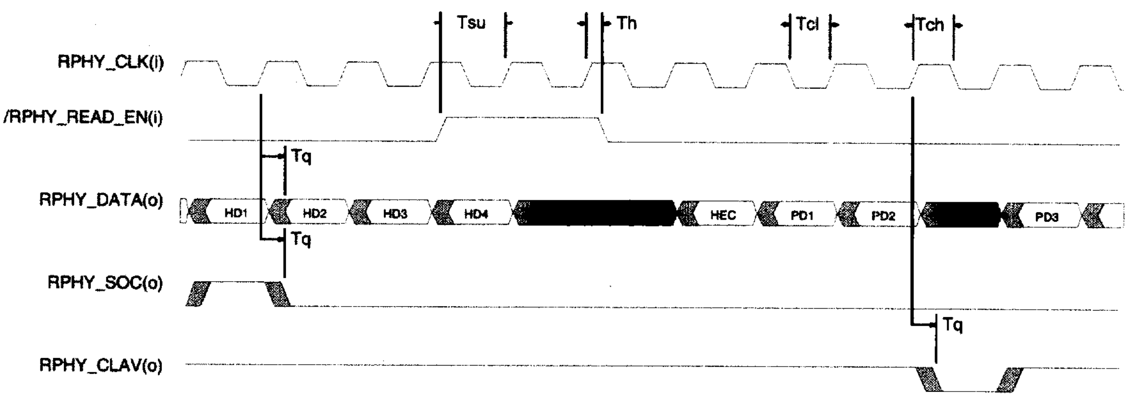


Figure 11. Receive SPHY UTOPIA Interface Timing

Figure 12 shows the receive MPHY interface timing.

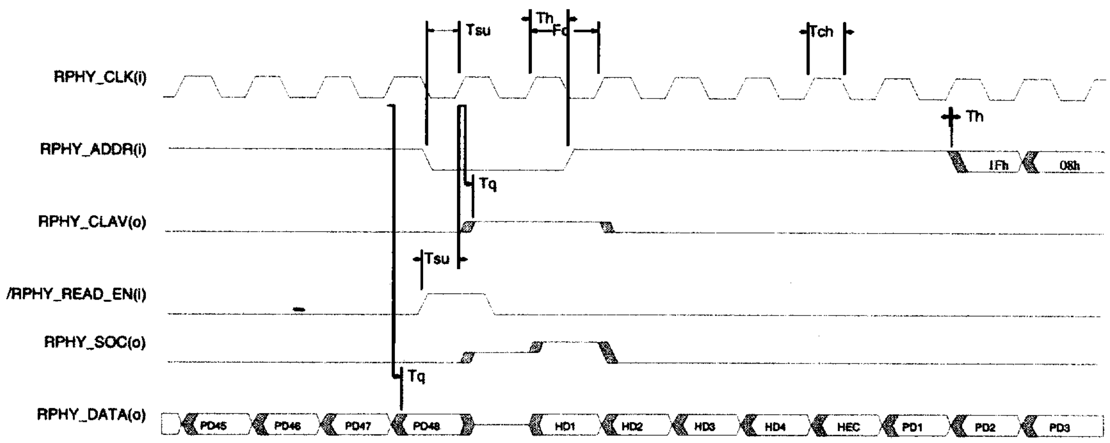


Figure 12. Receive MPHY UTOPIA Interface Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	RPHY_CLK frequency			33	MHz
Tch	RPHY_CLK duty cycle		45	55	%
Tsu	RPHY_CLK setup time	/RPHY_READ_EN, RPHY_ADDR	8		ns
Th	RPHY_CLK hold time	/RPHY_READ_EN	1		ns
Tq	RPHY_CLK to output delay	RPHY_DATA, RPHY_SOC, RPHY_CLAV		18	ns

Symbol	Definition
HD1 to HD4	1st to 4th header bytes
HEC	Header error check filler byte
PD1 to PD3	1st to 3rd payload bytes
PD45 to PD48	45th to 48th payload bytes

5.3 Microprocessor Timing

Figure 13 displays the timing for typical microprocessor read/write cycles. In Figure 13, the read cycle precedes the write cycle. The setup, hold, and delay times are given with respect to /CS, /RD, and /WR. Parameter times are determined by the relationships of the various signals as shown in the table that accompanies Figure 13. For example, the Tav parameter definition is "address valid time after /CS, /RD, or /WR; whichever comes last". This definition indicates that the address, A, must be valid *Tav* nanoseconds after /CS, /RD, or /WR; whichever comes last. In the read cycle example below, since /RD is asserted after /CS, the address must be valid *Tav* nanoseconds after the /RD signal, and has no minimum setup time with respect to the /CS signal. /CS, /RD, and /WR may be asynchronous to the WAC-186-B clock.

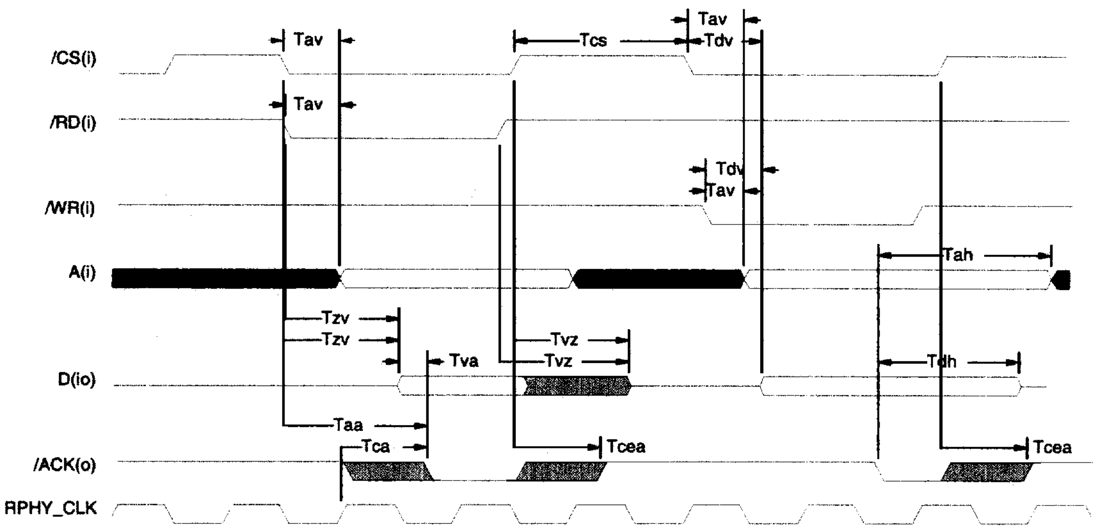


Figure 13. Microprocessor Read and Write Cycle Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tah	Address hold time from /ACK assertion.	A	0		ns
Tav	Address valid time after /CS, /RD, or /WR; whichever comes last.	A	0	40	ns
Tca	RPHY_CLK rising edge to /ACK assertion.	/ACK		25	ns
Tcea	/CS deassertion to /ACK deassertion.	/ACK		25	ns
Tcs	Minimum /CS deassertion time.		15		ns
Tdh	Data hold time from /ACK assertion.	D	0		ns
Taa	Acknowledge assertion after /CS, /WR, or /RD; whichever comes last.	/ACK	3	7	RPHY_CLK periods
Tdv	Data valid time after /CS or /WR; whichever comes last.	D		40	ns
Tva	Data valid prior to /ACK assertion.	D	20		ns
Tvz	Data tristate after /CS or /RD deassertion; whichever comes first.	D		25	ns
Tzv	Data active after /CS or /RD; whichever comes last.	D		25	ns

Figure 14 displays the interrupt timing constraints. The interrupt is asserted asynchronously with respect to the /RD and /CS signals when a non-masked interrupt occurs. The interrupt is cleared when the interrupt register (4_h) containing the active interrupt is read, assuming that no additional interrupts are generated during the read cycle.

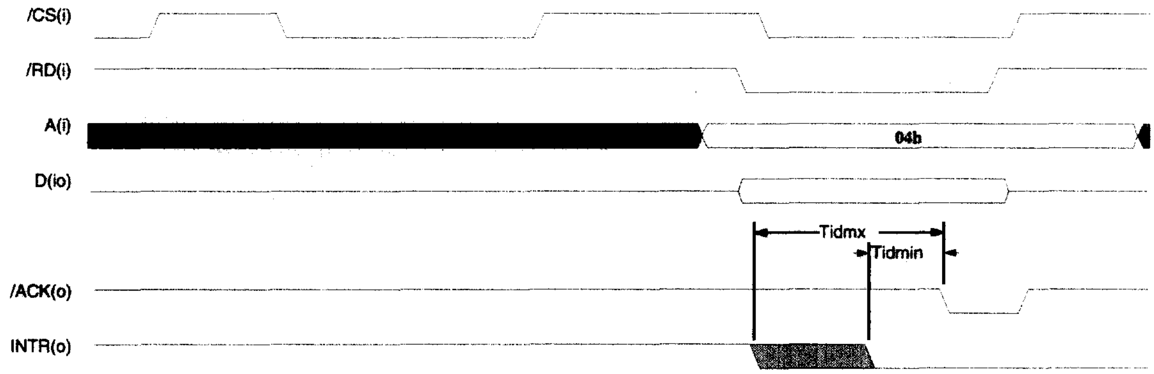


Figure 14. Interrupt Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tidmin	Interrupt deassertion prior to /ACK assertion	INTR	20		ns
Tidmx	Interrupt deassertion prior to /ACK assertion			1	RPHY_CLK period

5.4 RAM Interface Timing

5.4.1 Read Cycle Timing

Figure 15 shows the RAM interface timing for the read cycle.

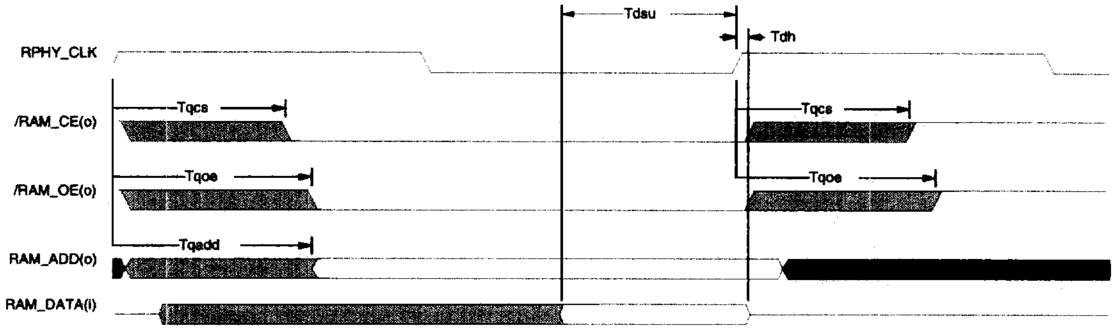


Figure 15. RAM Interface Timing for the Read Cycle

Symbol	Parameter	Signals	Min	Max	Unit
Tqcs	RPHY_CLK to output delay on /RAM_CE	/RAM_CE		16	ns
Tqoe	RPHY_CLK to output delay on /RAM_OE	/RAM_OE		18	ns
Tqadd	RPHY_CLK to output delay on RAM_ADD	RAM_ADD		16	ns
Tdsu	RAM data valid prior to RPHY_CLK	RAM_DATA	1		n
Tdh	RAM data valid after RPHY_CLK	RAM_DATA	1		ns

5.4.2 Write Cycle Timing

Figure 16 shows the RAM interface timing for the write cycle.

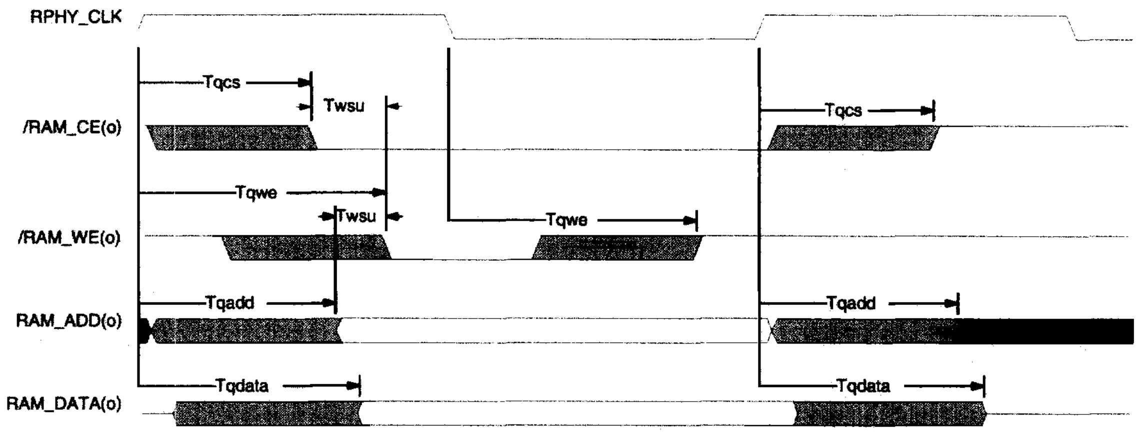


Figure 16. RAM Interface Timing for the Write Cycle

Symbol	Parameter	Signals	Min	Max	Unit
Tqcs	RPHY_CLK to output delay on /RAM_CE	/RAM_CE		16	ns
Tqadd	RPHY_CLK to output delay on RAM_ADD	RAM_ADD		16	ns
Tqdata	RPHY_CLK to output delay on RAM_DATA	RAM_DATA		19	ns
Tqwe	RPHY_CLK to output delay on /RAM_WE	/RAM_WE		22	n
Twsu	/RAM_CE and RAM_ADD valid prior to fall of /RAM_WE	/RAM_CE, RAM_ADD	0		ns

5.5 Miscellaneous Timing

5.5.1 Reset Timing

Figure 17 shows the reset signal timing. The /RESET signal must be asserted for a minimum time (Tres). The WAC-186-B remains in reset while /RESET is asserted.

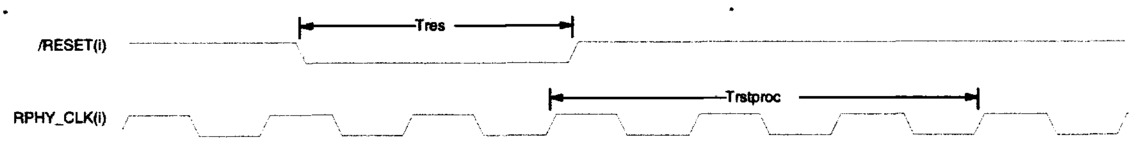


Figure 17. Reset Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tres	Reset assertion time	/RESET	40		ns
Trstproc	Reset processing time	/RESET	3		RPHY_CLK periods

5.5.2 Output Enable Timing

All outputs of the chip are tristated when OUTPUT_EN is deasserted. Figure 18 shows the output enable timing.

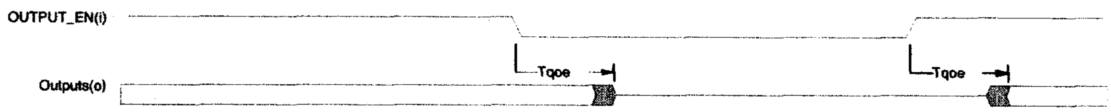


Figure 18. Output Enable Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tqoe	Output enable	All outputs		25	ns

5.5.3 8 KHz Signal Timing

Figure 19 shows the timing required for the 8_KHz signal.

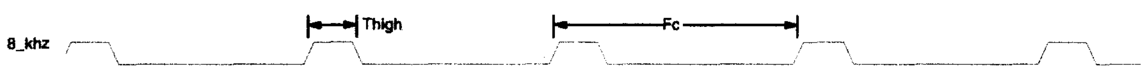


Figure 19. Timing for the 8_KHz Signal

Symbol	Parameter	Signals	Min	Typical	Max	Unit
Fc	Frequency	8_KHz		8		KHz
Thigh	8_KHz pulse width high	8_KHz	15			ns
NOTE: 8 kHz is required for 1 second periodic OAM cells. This signal may be connected to a UNI 8 kHz framing pulse or an 8 kHz oscillator.						

6 BOUNDARY SCAN

Table 19 lists the boundary scan instructions and instruction codes.

Table 19. Boundary Scan Instruction Codes

Instruction Name	Instruction Code, IR(1:0)
EXTEST	00
BYPASS	11
BYPASS	10
SAMPLE	01

Table 20 shows the boundary scan registers. In these registers, bit 0 will be shifted out first on SCAN_TDO.

The entries in the Type column are defined as follows: "In" are input scan registers, "Out" are output scan registers, and "En" are internal scan registers that control the tristate enable pins on the outputs.

Table 20. Boundary Scan Registers

Pin/Enable Name	Bit #	Type
/RAM_CE	237	Out
/RAM_OE	236	Out
/RAM_WE	235	Out
RAM_ADD(18:0)	234-216	Out
/RAM_OE_EN(3)	215	En
RAM_DATA(31)	214	In
RAM_DATA(31)	213	Out
RAM_DATA(30)	212	In
RAM_DATA(30)	211	Out
RAM_DATA(29)	210	In
RAM_DATA(29)	209	Out
RAM_DATA(28)	208	In
RAM_DATA(28)	207	Out
RAM_DATA(27)	206	In
RAM_DATA(27)	205	Out
RAM_DATA(26)	204	In
RAM_DATA(26)	203	Out
RAM_DATA(25)	202	In
RAM_DATA(25)	201	Out
RAM_DATA(24)	200	In
RAM_DATA(24)	199	Out
/RAM_OE_EN(2)	198	En
RAM_DATA(23)	197	In
RAM_DATA(23)	196	Out
RAM_DATA(22)	195	In
RAM_DATA(22)	194	Out
RAM_DATA(21)	193	In
RAM_DATA(21)	192	Out
RAM_DATA(20)	191	In
RAM_DATA(20)	190	Out
RAM_DATA(19)	189	In
RAM_DATA(19)	188	Out
RAM_DATA(18)	187	In
RAM_DATA(18)	186	Out
RAM_DATA(17)	185	In
RAM_DATA(17)	184	Out
RAM_DATA(16)	183	In
RAM_DATA(16)	182	Out
/RAM_OE_EN(1)	181	En
RAM_DATA(15)	180	In
RAM_DATA(15)	179	Out
RAM_DATA(14)	178	In
RAM_DATA(14)	177	Out
RAM_DATA(13)	176	In
RAM_DATA(13)	175	Out
RAM_DATA(12)	174	In
RAM_DATA(12)	173	Out
RAM_DATA(11)	172	In
RAM_DATA(11)	171	Out
RAM_DATA(10)	170	In
RAM_DATA(10)	169	Out
RAM_DATA(9)	168	In
RAM_DATA(9)	167	Out
RAM_DATA(8)	166	In
RAM_DATA(8)	165	Out
/RAM_OE_EN(0)	164	En
RAM_DATA(7)	163	In
RAM_DATA(7)	162	Out
RAM_DATA(6)	161	In
RAM_DATA(6)	160	Out
RAM_DATA(5)	159	In
RAM_DATA(5)	158	Out
RAM_DATA(4)	157	In
RAM_DATA(4)	156	Out
RAM_DATA(3)	155	In
RAM_DATA(3)	154	Out
RAM_DATA(2)	153	In
RAM_DATA(2)	152	Out
RAM_DATA(1)	151	In
RAM_DATA(1)	150	Out
RAM_DATA(0)	149	In
RAM_DATA(0)	148	Out
RATM_SOC	147	In
RATM_CLAV (/RATM_EMPTY)	146	In
/RATM_READ_EN	145	Out
RATM_DATA(0:7)	144-137	In
/RESET	136	In
8_KHZ	135	In
TATM_DATA(0:7)	134-127	Out
/TI_CLAV_TRI_OE	126	En
TATM_CLAV (/TATM_FULL)	125	In
TATM_SOC	124	Out

Table 20. Boundary Scan Registers (Continued)

Pin/Enable Name	Bit #	Type
/TATM_WRITE_EN	123	Out
TATM_TAG(0:1)	122-121	Out
MICRO_DATA(0)	120	In
MICRO_DATA(0)	119	Out
MICRO_DATA(1)	118	In
MICRO_DATA(1)	117	Out
MICRO_DATA(2)	116	In
MICRO_DATA(2)	115	Out
MICRO_DATA(3)	114	In
MICRO_DATA(3)	113	Out
MICRO_DATA(4)	112	In
MICRO_DATA(4)	111	Out
MICRO_DATA(5)	110	In
MICRO_DATA(5)	109	Out
MICRO_DATA(6)	108	In
MICRO_DATA(6)	107	Out
MICRO_DATA(7)	106	In
MICRO_DATA(7)	105	Out
MICRO_DATA(8)	104	In
MICRO_DATA(8)	103	Out
MICRO_DATA(9)	102	In
MICRO_DATA(9)	101	Out
MICRO_DATA(10)	100	In
MICRO_DATA(10)	99	Out
MICRO_DATA(11)	98	In
MICRO_DATA(11)	97	Out
MICRO_DATA(12)	96	In
MICRO_DATA(12)	95	Out
MICRO_DATA(13)	94	In
MICRO_DATA(13)	93	Out
MICRO_DATA(14)	92	In
MICRO_DATA(14)	91	Out
MICRO_DATA(15)	90	In
MICRO_DATA(15)	89	Out
MICRO_DATA(16)	88	In
MICRO_DATA(16)	87	Out
MICRO_DATA(17)	86	In
MICRO_DATA(17)	85	Out
MICRO_DATA(18)	84	In
MICRO_DATA(18)	83	Out
MICRO_DATA(19)	82	In
MICRO_DATA(19)	81	Out
MICRO_DATA(20)	80	In
MICRO_DATA(20)	79	Out
MICRO_DATA(21)	78	In

Pin/Enable Name	Bit #	Type
MICRO_DATA(21)	77	Out
MICRO_DATA(22)	76	In
MICRO_DATA(22)	75	Out
MICRO_DATA(23)	74	In
MICRO_DATA(23)	73	Out
MICRO_DATA(24)	72	In
MICRO_DATA(24)	71	Out
MICRO_DATA(25)	70	In
MICRO_DATA(25)	69	Out
MICRO_DATA(26)	68	In
MICRO_DATA(26)	67	Out
MICRO_DATA(27)	66	In
MICRO_DATA(27)	65	Out
MICRO_DATA(28)	64	In
MICRO_DATA(28)	63	Out
MICRO_DATA(29)	62	In
MICRO_DATA(29)	61	Out
MICRO_DATA(30)	60	In
MICRO_DATA(30)	59	Out
MICRO_DATA(31)	58	In
MICRO_DATA(31)	57	Out
/MICRO_OE	56	En
MICRO_ADDR(0:19)	55-36	In
/CS	35	In
/RD	34	In
/WR	33	In
/ACK	32	Out
INTR	31	Out
TPHY_ADDR	30	In
TPHY_TAG(1:0)	29-28	In
/TPHY_WRITE_EN	27	In
TPHY_SOC	26	In
TPHY_CLAV	25	Out
TPHY_DATA(7:0)	24-17	In
TPHY_CLK	16	In
RPHY_CLK	15	In
RPHY_DATA(7:0)	14-7	Out
/RPHY_DATA_OE	6	En
/RPHY_READ_EN	5	In
/RPHY_CLAV_OE	4	En
RPHY_CLAV	3	Out
RPHY_SOC	2	Out
RPHY_ADDR	1	In
RPHY_CLAV_OAM	0	Out

7 MICROPROCESSOR PORTS

7.1 Microprocessor Ports Summary

Table 21. Microprocessor Ports Summary

Address	Name	Read or Write	Description
0_h	SOFTWARE_RESET	R/W	Places the WAC-186-B in a soft reset state.
1_h	GLOBAL_CONFIG	R/W	Sets the globally programmable WAC-186-B options.
2_h	REV	R	Indicates the device revision.
3_h	PM_THRES	R/W	Indicates thresholds for declaring a PM block severely errored.
4_h	INT	R	Indicates which interrupt conditions have occurred since the register was cleared.
5_h	INT_MASK	R/W	Contains masks to disable the associated interrupts.
6_h	AIS/RDI/LOC LOCATOR	R	Marks the ranges in which a change in AIS state, RDI state, or LOC was detected.
7_h	INVALID_VPI/VCI	R	Contains the last invalid VPI/VCI detected.
8_h	Reserved		Initialize to 0 at initial setup. Software modifications to this location after setup will cause incorrect operation.
9_h	LOCAL_TIME	R/W	Indicates the local time.
A_h	FM_OAM_CMD	R/W	Initiates or terminates the generation/expectation of periodic fault management cells (AIS/RDI/CC) or the generation of single LB cells.
B_h	FM_OAM_CMD2	R/W	Second part of the FM_OAM_CMD register. Contains the VPI/VCI for the associated command.
C_h	SEND_TX_FIFO	R/W	Controls the transmission of the TX_FIFO contents.
D_h	TEST_MODE	R/W	Controls the test modes.
E_h	LOOPBACK_ SOURCE_ID (Optional)	R/W	Write with the value 0 to maintain software compatibility with future versions.
F_h	Not used		Write with the value 0 to maintain software compatibility with future versions.
10_h	TX_OAM_FIFO	W	A one-cell FIFO that holds the OAM cell to be transmitted.

7.2 Microprocessor Port Bit Definitions

NOTES:

- The external /RESET signal resets all microprocessor write ports to their specified values when asserted.
- All ports marked as "Reserved" must not be modified from their reset values. Software modifications to these locations will cause incorrect operation.
- All read/write port bits marked "Not used" must be written with the value 0 to maintain software compatibility with future versions.
- All read-only port bits marked "Not used" are driven with a 0 and should be masked off by the software to maintain compatibility with future versions.
- After a software reset, values in the microprocessor ports and external RAM memory remain unchanged.

7.2.1 SOFTWARE_RESET

Address: 0_h
Type: Read/Write
Function: Places the WAC-186-B in a soft reset state. During the soft reset state, only the microprocessor register interface is active; the rest of the device is in reset. While in reset, the WAC-186-B will not accept or transmit cells, or perform any updates to the SRAM. All outputs will be held in their inactive states.
Hardware Reset Value: 00000000_h
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:1)	Write with a 0 to maintain software compatibility with future versions.
SW_RESET (0)	1 Places the WAC-186-B cell functions in the reset state. 0 Allows the device to resume normal operation.

7.2.2 GLOBAL_CONFIG

Address: 1_h
Type: Read/Write
Function: Sets the globally programmable WAC-186-B options.
Hardware Reset Value: 00000000_h
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:16)	Write with a 0 to maintain software compatibility with future versions.
EXTENDED_LB (15)	1 Enable support of the SOURCE_ID and LOOPBACK_LOCATION_ID fields in the OAM LB cell. The SOURCE_ID and LOOPBACK_LOCATION_ID fields are generated for all LB cells. For VCs or VPs that are not end-to-end or segment termination points, the SOURCE_ID fields and LOOPBACK_LOCATION_ID fields are checked before the LB cell is processed. 0 Ignore SOURCE_ID and LOOPBACK_LOCATION_ID fields in the OAM LB Cell.
MPHY_SEL (14)	1_b Enable SPHY/octet-level handshaking UTOPIA mode. 0_b Enable MPHY/cell-level handshaking UTOPIA mode.
VPI_BITS_OUTGOING (13:12)	Controls the translation of the channel number into the VP and VC fields. All bits not set by the translation are set to 0.This field represents the number of bits placed in the VP field. Remaining bits are placed in the VC field. For more information on the VCI/VPI translation option, refer to section 9.10 "Mapping Channels on the WAC-186-B for Use with the ATM Routing Table (WAC-187)" on page 91. 00_b Do not place any bits of the channel number in the VP field when translating is enabled. 01_b Place bits 5:0 of the channel number in the VP field when translating is enabled. 10_b Place bits 6:0 of the channel number in the VP field when translating is enabled. 11_b Place bits 7:0 of the channel number in the VP field when translating is enabled.
OAM_CRC_GEN (11)	0_b Do not generate CRC-10 on cells sourced from the OAM_TX_FIFO. 1_b Generate CRC-10 on cells sourced from the OAM_TX_FIFO.
OAM_RX (10)	0_b Place unhandled OAM cells in the external receive FIFO. Handled cells include AIS, RDI, LB, continuity, and PM cells when PM is enabled on the channel. Refer to section 9.11.8 "OAM Summary Tables" on page 99. 1_b Pass unhandled OAM cells in the normal cell flow.
VP/VC_PASS (9)	0_b Translate VPI/VCI to the channel number on received cells. 1_b Pass VPI/VCI as received when translating.
DROP_OUT_OF_RANGE (8)	Drop cells with "out-of-range" VPI/VCI. Out-of-range VPI/VCI have bits set that are greater than the allowable number of VPI or VCI bits. The GFC field is ignored unless VPI_BITS = 111. 0_b Do not check for cells with out-of-range VPI/VCI values. 1_b Check/drop cells with out-of-range VPI/VCI values. NOTE: If not dropped, cells with out-of-range VPI/VCI values may cause improper operation due to address aliasing.
UPC/OAM_EN (7)	0_b Disable UPC/OAM processing. All cells pass, no OAM cells processed. 1_b Enable UPC/OAM function.

(Continued)

Field (Bits)	Description
DROP_INACTIVE (6)	Drop cells with inactive VPI/VCI. Inactive VPI/VCIs are valid VPI/VCI combinations that are not marked as "active" in the VPI/VCI Connection Lookup Table (refer to section 8.2.7 "VPI/VCI Connection Lookup Table Summary" on page 77). 0_b Do not drop cells with inactive VPI/VCI values. 1_b Drop cells with inactive VPI/VCI values.
SRAM_CONFIG (5:4)	SRAM configuration. Initialize to the proper setting. 00_b 32K × 32 SRAM, 15 valid VP/VC bits, 1024 active channels. 01_b 128K × 32 SRAM, 17 valid VP/VC bits, 4096 active channels. 10_b 256K × 32 SRAM, 18 valid VP/VC bits, 8192 active channels. 11_b 512K × 32 SRAM, 19 valid VP/VC bits, 16384 active channels.
Not used (3)	Write with a 0 to maintain software compatibility with future versions.
VPI_BITS (2:0)	In the received cell, the number of VPI bits to be used in the channel lookup table address calculation (refer to section 8.2.8.1 "CHAN" on page 77). When values for SRAM_CONFIG = 00b: 000_b Use VCI(9:0),VPI(4:0) as the connection. 001_b Use VCI(8:0),VPI(5:0) as the connection. 010_b Use VCI(7:0), VPI(6:0) as the connection. 011_b Use VCI(6:0), VPI(7:0) as the connection. 111_b Use VPI(9:0) as the channel number. (VP-only mode.)* When values for SRAM_CONFIG = 01b: 000_b Use VCI(11:0), VPI(4:0) as the connection. 001_b Use VCI(10:0), VPI(5:0) as the connection. 010_b Use VCI(9:0), VPI(6:0) as the connection. 011_b Use VCI(8:0), VPI(7:0) as the connection. 111_b Use VPI(11:0) as the channel number. (VP-only mode.)* When values for SRAM_CONFIG = 10b: 000_b Use VCI(12:0), VPI(4:0) as the connection. 001_b Use VCI(11:0), VPI(5:0) as the connection. 010_b Use VCI(10:0), VPI(6:0) as the connection. 011_b Use VCI(9:0), VPI(7:0) as the connection. 111_b Use VPI(11:0) as the connection. (VP-only mode.)* When values for SRAM_CONFIG = 11b: 000_b Use VCI(13:0), VPI(4:0) as the connection. 001_b Use VCI(12:0), VPI(5:0) as the connection. 010_b Use VCI(11:0), VPI(6:0) as the connection. 011_b Use VCI(10:0), VPI(7:0) as the connection. 111_b Use VPI(11:0) as the connection. (VP-only mode.)*

*NOTE: In an NNI, the bits of the header that are often referred to as the GFC(3:0) become VPI bits (11:8).

7.2.3 REV

Address: 2_h
Type: Read Only
Function: Indicates the revision number of the WAC-186-B.
Hardware Reset Value: 00001861_h
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:16)	Write with a 0 to maintain software compatibility with future versions.
REVISION (15:0)	1861_h Revision B.

7.2.4 PM_THRES

Address: 3_h
Type: Read /Write
Function: Indicates thresholds for declaring a PM block severely errored.
Hardware Reset Value: 00000000_h
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:12)	Write with a 0 to maintain software compatibility with future versions.
BLER_THRESHOLD (11:8)	Indicates the value of the Block Error Result (BLER) beyond which a PM report is considered severely errored.
LOST_THRESHOLD (7:4)	Indicates the number of cells detected as lost beyond which a PM report is considered severely errored.
MISINSERT_THRES (3:0)	Indicates the number of cells detected as misinserted beyond which a PM report is considered severely errored.

7.2.5 INT

Address: 4_h
Type: Read Only (Clear on Read)
Function: Indicates which interrupt conditions have occurred since the register was cleared. This register, in conjunction with the INT_MASK register, generates the microprocessor interrupt.
Hardware Reset Value: 00000000_h
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:6)	Write with a 0 to maintain future software compatibility.
OAM_CRC_ERR (5)	1_b An OAM cell was received with an invalid CRC field. 0_b No OAM cells were received with an invalid CRC field.
INVAL_VP (4)	1_b An invalid VPI/VCI was detected. 0_b No invalid VPI/VCIs were detected.
LB_INT (3)	1_b An OAM loopback was completed. 0_b No OAM loopbacks were completed.
LOC_INT (2)	1_b A channel either entered or exited the LOC state. The channel is not receiving expected CC cells. 0_b No change in any channel's LOC state.
RDI_INT (1)	1_b A channel either entered or exited the RDI state (receiving RDIs). 0_b No change in any channel's RDI state.
AIS_INT (0)	1_b A channel either entered or exited the AIS state (receiving AISs). 0_b No change in any channel's AIS state.

As shown in Figure 20, some of the bits in the interrupt register point to other registers in which more information on the error condition may be found.

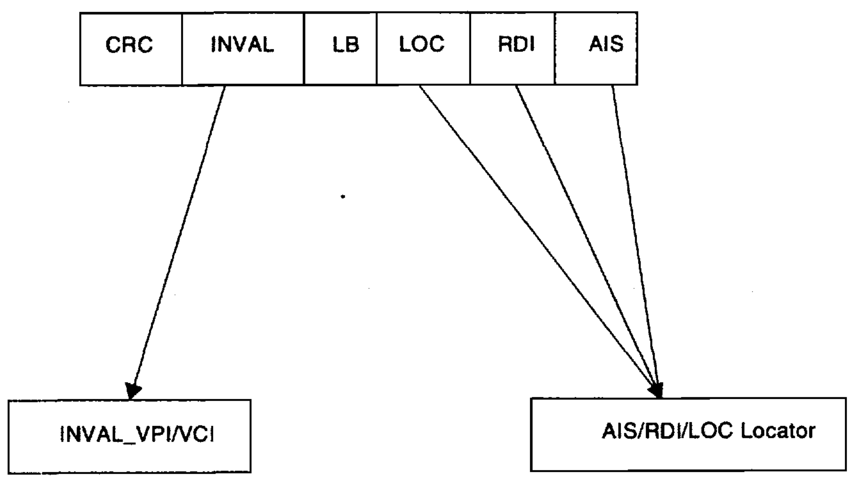


Figure 20. Interrupt Information Tree

7.2.6 INT_MASK

Address: 5_h
Type: Read/Write
Function: Contains masks to disable the associated interrupts. If a mask bit is set, the associated interrupt will not generate a microprocessor interrupt.

NOTE: The _MASK bits in this register disable the generation of an interrupt through the INTR pin. However, they do not affect the operation of the associated interrupt or status bits.

Hardware Reset Value: 0000 $003F_h$
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:6)	Write with a 0 to maintain software compatibility with future versions.
OAM_CRC_ERR_MASK (5)	1 Disables OAM_CRC_ERR. 0 Enables OAM_CRC_ERR.
INVAL_VP_MASK (4)	1 Disables INVAL_VP_INTR. 0 Enables INVAL_VP_INTR.
LB_INT_MASK (3)	1 Disables LB_INT. 0 Enables LB_INT.
LOC_INT_MASK (2)	1 Disables LOC_INT. 0 Enables LOC_INT.
RDI_INT_MASK (1)	1 Disables RDI_INT. 0 Enables RDI_INT.
AIS_INT_MASK (0)	1 Disables AIS_INT. 0 Enables AIS_INT.

7.2.7 AIS/RDI/LOC Locator

Address: 6_h

Type: Read Only (Clear on Read)

Function: Marks the range of channels in which a change in AIS state, RDI state, or LOC was detected. A change of AIS state, RDI state, or LOC state in a channel will cause the appropriate interrupt to be generated and will set a bit in this register corresponding to the range in which the channel is located. This register helps identify which channel was the cause of the AIS, RDI, or LOC interrupt.

Organization: The channel space is divided into 32 consecutive ranges. The size of the range depends on the SRAM configuration:

For SRAM_CONFIG = 00, each range is 32 channels.
For SRAM_CONFIG = 01, each range is 128 channels.
For SRAM_CONFIG = 10, each range is 256 channels.
For SRAM_CONFIG = 11, each range is 512 channels.

Hardware Reset Value: 00000000_h

Locator Word Format: Refer to the following table.

Field (Bits)	Description
LOCATOR (31:0)	1_b One or more AIS/RDI/LOC states in the range has changed since the last read. 0_b No AIS/RDI/LOC states in range changed.

Figure 23 shows an example of how address ranges are mapped in the LOCATOR word.

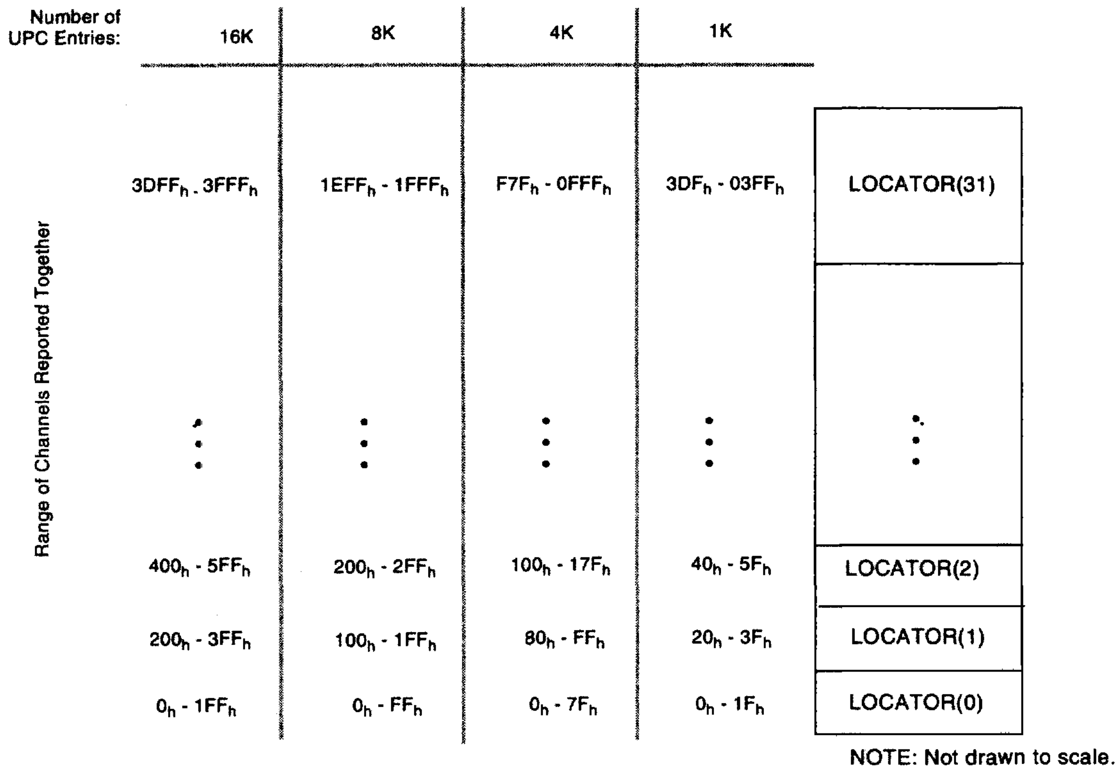


Figure 21. Locator Range Mapping

7.2.8 INVALID_VPI/VCI

Address: 7_h
Type: Read Only (Clear on Read)
Function: Indicates the last VPI/VCI that was discarded because it was an out-of-range VPI/VCI or an inactive VPI/VCI.
Hardware Reset Value: 00000000_h
Format: Refer to the following table.

Field (Bits)	Description
GFC (31:28)	Indicates the GFC of the last cell discarded due to invalid VPI/VCI.
VPI (27:20)	Indicates the VPI of the last cell discarded due to invalid VPI/VCI.
VCI (19:4)	Indicates the VCI of the last cell discarded due to invalid VPI/VCI.
PTI (3:1)	Indicates the PTI of the last cell discarded due to invalid VPI/VCI.
CLP (0)	Indicates the CLP of the last cell discarded due to invalid VPI/VCI.

7.2.9 LOCAL_TIME

Address: 9_h
Type: Read/Write
Function: Indicates the local time. Local time is represented in number of RPHY_CLK cycles and has no relation to real time.
Hardware Reset Value: 00000000_h
Format: Refer to the following table.

Field (Bits)	Description
LOCAL_TIME (31:0)	Indicates the local time. Resolution is in clock cycles.

7.2.10 FM_OAM_CMD

Address: A_h
Type: Read/Write
Function: Initiates or terminates the generation or expectation of periodic FM cells (AIS/RDI/CC), or the generation of single LB cells. The FM_OAM_CMD2 port contains the VPI/VCI for the generated cell. The NDONE field should be written with a 1. When the command has been executed, the NDONE field will be set to 0, and another command may be initiated.

NOTE: The OAM_FM_CMD2 register **must** be written before FM_OAM_CMD is written (refer to section 7.2.11 "FM_OAM_CMD2" on page 56).

Hardware Reset Value: FFFF 0000_h
Format: Refer to the following table.

Field (Bits)	Description
LOOPBACK_LOCATION_ID (Optional) (31:16)	When EXTENDED_LB support is enabled, this code is placed in the least significant 16-bits of the LOOPBACK_LOCATION_ID field of OAM LB cells generated by the WAC-186-B. When EXTENDED_LB support is not enabled, the least significant 16 bits of OAM LB cells generated by the WAC-186-B are set to "FFFF". The 14 most significant bytes of the LOOPBACK_LOCATION_ID field are set to "FF".
Not used (15:13)	Write with a 0 to maintain future software compatibility.
LOOPBACK_SESSION (12:8)	Indicates the LB session number.
OAM_CMD_ERR (7)	1_b Command completed in error due to the current UPC control block state of the VP/VC designated in FM_OAM_CMD2 (refer to section 7.2.11 "FM_OAM_CMD2" on page 56.) 0_b Command completed successfully.
OAM_FUNCTION_TYPE (6:4)	000_b Generate AIS OAM cells at an average rate of one cell per second. 001_b Generate RDI OAM cells at an average rate of one cell per second. 010_b Generate CC OAM cells in the A-to-B direction at an average rate of one cell per second.. 011_b Expect CC OAM cells in the B-to-A direction and detect LOC state. $1XX_b$ Generate one LB OAM cell.
F4/F5 (3)	0_b Use F4 OAM flow (VP OAM flow). 1_b Use F5 OAM flow (VC OAM flow).
END/SEG (2)	0_b Use segment OAM flow. 1_b Use end-to-end OAM flow.
STOP/START (1)	0_b Stop action defined in OAM_FUNCTION_TYPE. Not valid for function type "$1XX_b$" (generate LB OAM cell). 1_b Start action defined in OAM_FUNCTION_TYPE.
NDONE (0)	1_b Command in progress. 0_b Command completed.

7.2.11 FM_OAM_CMD2

Address: B_h
Type: Read/Write
Function: Part two of the FM_OAM_CMD register. This register contains the VPI/VCI for the associated command.

NOTE: This register must be written before the FM_OAM_CMD register is written (refer to section 7.2.10 "FM_OAM_CMD" on page 55).

Hardware Reset Value: 00000000_h
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:30)	Write with a 0 to maintain software compatibility with future versions.
LB_TAG (29:28)	Indicates the value of the priority tag to be sent with generated LB OAM cells.
GFC (27:24)	Indicates the GFC for the OAM command.
VPI (23:16)	Indicates the VPI for the OAM command.
VCI (15:0)	Indicates the VCI for the OAM command.

7.2.12 SEND_TX_FIFO

Address: C_h
Type: Read/Write
Function: Controls the transmission of the TX_FIFO contents.
Hardware Reset Value: 00000000_h
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:3)	Write with a 0 to maintain future software compatibility.
TX_FIFO_PRI_TAG (2:1)	Indicates the value of the priority tag to be sent with the cell in the TX_FIFO.
SEND_TX (0)	1_b Transmit cell from TX_FIFO. The cell is transmitted on the TATM UTOPIA interface. 0_b Transmit operation has completed. No operation pending.

NOTES:

- If the TX_FIFO is used to send a non-OAM cell and PM is enabled for that VP/VC, the cell will cause an error (misinserted cell) in the PM session downstream.
- To have the WAC-186-B generate a CRC-10 when an OAM cell is sent, set the OAM_CRC_GEN bit in the UPC_CONFIG register (refer to section 7.2.2 "GLOBAL_CONFIG" on page 48).

7.2.13 TEST_MODE

Address: D_h
Type: Read/Write
Hardware Reset Value: $0000\ 0000_h$
Format: Refer to the following table..

Field (Bits)	Description
Not used (31:4)	Write with a 0 to maintain future software compatibility.
Reserved (3:1)	
TEST_LOOP (0)	Places chip in test loopback mode. 0_b Enables normal device operation. 1_b Enables the test mode that loops the UTOPIA receive output to the UTOPIA transmit input.

7.2.14 LOOPBACK_SOURCE_ID (Optional)

Address: E_h
Type: Read/Write
Hardware Reset Value: $0000\ 0000_h$
Format: Refer to the following table.

Field (Bits)	Descriptions
Not used (31:16)	Write with a 0 to maintain future software compatibility.
SOURCE_ID (15:0)	When EXTENDED_LB support is enabled, this code is placed in the least significant 16-bits of the SOURCE_ID field in the OAM LB cell generated by the WAC-186-B. The 14 most significant bytes are set to "FF". If EXTENDED_LB support is not enabled, all 16 bytes of the SOURCE_ID field in the OAM LB cell generated by the WAC-186-B are set to "FF".

7.2.15 TX_OAM_FIFO

Address: 10_h

Type: Write Only

Function: A one-cell FIFO that holds the OAM cell to be transmitted. The cell data must be packed into 4-byte words as shown in Table 22. The MSB is sent on the UTOPIA interface first. After the FIFO is full, further writes to this location are ignored. The FIFO is reset to empty after the cell is transmitted.

NOTE: To have the WAC-186-B generate a CRC-10 when an OAM cell is sent, set the OAM_CRC_GEN bit in the UPC_CONFIG register (refer to section 8.2.2.1 "UPC_CONFIG" on page 62).

Format: Refer to the following table.

Field (Bits)	Description
OAM_TX_CELL_DATA (31:0)	Contains the OAM data to be transmitted via the transmit UTOPIA interface.

Cell data must be transferred to the FIFO in the order listed in Table 22.

Table 22. TX OAM FIFO Descriptions

Word Number	Cell			
	31:24	23:16	15:8	7:0
0	header byte 1	header byte 2	header byte 3	header byte 4
1				header byte 5
2	payload byte 1	payload byte 2	payload byte 3	payload byte 4
3	payload byte 5	payload byte 6	payload byte 7	payload byte 8
4	payload byte 9	payload byte 10	payload byte 11	payload byte 12
5	payload byte 13	payload byte 14	payload byte 15	payload byte 16
6	payload byte 17	payload byte 18	payload byte 19	payload byte 20
7	payload byte 21	payload byte 22	payload byte 23	payload byte 24
8	payload byte 25	payload byte 26	payload byte 27	payload byte 28
9	payload byte 29	payload byte 30	payload byte 31	payload byte 32
10	payload byte 33	payload byte 34	payload byte 35	payload byte 36
11	payload byte 37	payload byte 38	payload byte 39	payload byte 40
12	payload byte 41	payload byte 42	payload byte 43	payload byte 44
13	payload byte 45	payload byte 46	payload byte 47	payload byte 48

8 EXTERNAL RAM MEMORY MAP

8.1 External RAM Summary

The external RAM contains:

- UPC Control Blocks
- PM Control Block
- Loopback (LB) Control Blocks
- VPI/VCI Connection Lookup Table

The memory-mapped ports information is stored in the external memory. All of the external memory is available to the host processor for read/write access. Figure 22 shows the external RAM memory map.

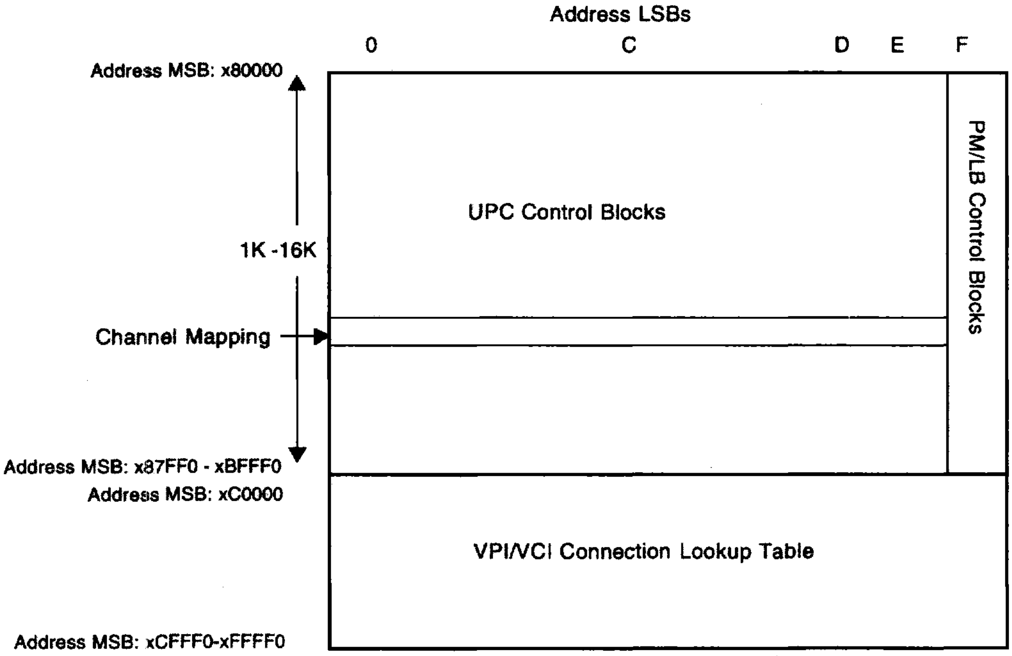


Figure 22. External RAM Memory Map

Figure 23 shows a memory map of the external RAM, including address values for possible numbers of UPC entries.

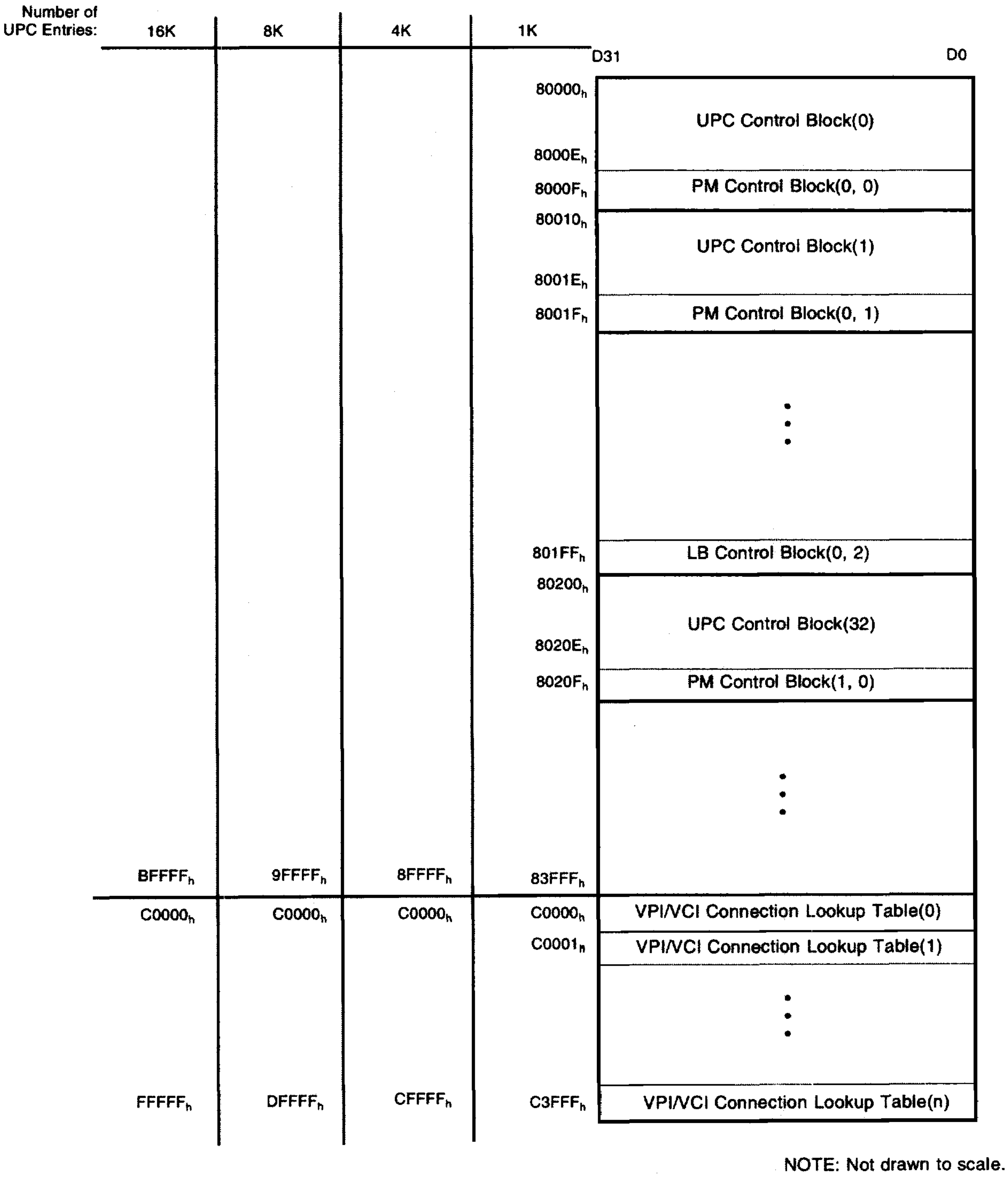


Figure 23. External RAM Memory Map

8.2 External RAM Block Definitions

NOTES:

- All ports marked as "Reserved" must be initialized to 0 at initial setup. Software modifications to these locations after setup will cause incorrect operation.
- All read/write port bits marked "Not used" must be written with the value 0 to maintain software compatibility with future versions.
- All read-only port bits marked "Not used" are driven with a 0 and should be masked off by the software to maintain compatibility with future versions.
- The entire external memory space is accessible by the host to facilitate memory testing. However, write operations to ports marked "Read" are not recommended during operation because the WAC-186-B will be constantly updating them. These ports provide the host with statistical information.

8.2.1 UPC Control Block Summary

Function: The UPC Control Block contains the information necessary for performing UPC policing. UPC_CONFIG, the configuration, T0, τ0, GCRA coefficients, T1, τ1, GCRA1 coefficients, and VPI/VCI fields must be set on channel activation/setup. All other fields may be initialized to "000" at this time to provide known starting values.

Organization: 1K-16K entries

Base address: 80000_h

Index: 10_h

Address = *base* + (*channel* × *index*) + *offset*

Table 23. UPC Control Block Summary

Offset	Name	Read or Write	Description
0_h	UPC_CONFIG	R/W	Contains configuration information for the GCRA operation, pointers to PM sessions enabled for this channel, and channel configuration for VP or VC segment points or end points.
1_h	Reserved	R	Initialize to 0 at initial setup. Software modifications to this location after setup will cause incorrect operation.
2_h	T0	R/W	Provides the T parameter for the first GCRA algorithm.
3_h	τ0	R/W	Provides the τ parameter for the first GCRA algorithm.
4_h	Reserved	R	Initialize to 0 at initial setup. Software modifications to this location after setup will cause incorrect operation.
5_h	T1	R/W	Provides the T parameter for the second GCRA algorithm.
6_h	τ1	R/W	Provides the τ parameter for the second GCRA algorithm.
7_h	GRCA0_DROP/TAG_CNT	R	Counts the non-compliant cells tagged or dropped by the GCRA0 algorithm.
8_h	GCRA1_DROP/TAG_CNT	R	Counts the non-compliant cells tagged or dropped by the GCRA1 algorithm.
9_h	CLP0	R	Counts the CLP = 0 cells received by this VPC/VCC.
A_h	TOT_CELLS	R	Counts the total cells received by this VPC/VCC.
B_h	TOT_OAM_PASSED	R	Counts the OAM cells passed through by this channel.
C_h	STATUS	R	Indicates the current state of the UPC channel.
D_h	VPI/VCI	R/W	Indicates the VPI/VCI for generated OAM cells.

8.2.2 UPC Control Block Bit Descriptions

NOTE: When counters reach the maximum value, they will "roll over" to 0. If statistics are required, the software should periodically sample the counters.

8.2.2.1 UPC_CONFIG

Offset: 0_h
Type: Read/Write
Function: Contains configuration information for the GCRA operation, pointers to PM sessions enabled for this channel, and channel configurations for VP or VC segment points or end points. This location must be initialized by the host during channel activation.
Format: Refer to the following table.

Field (Bits)	Description
VP_MON (31)	This bit is valid only for VP UPC channels. 1 Perform UPC function on VP. 0 Perform UPC function on VC. NOTE: This field is valid only for VP control blocks.
GCRA0_EN (30)	1 Enable the GCRA0 filter. 0 Disable the GCRA0 filter.
GCRA0_POLICE (29)	1 Police according to GCRA0 parameters. 0 Monitor only; no policing actions taken.
GCRA0_DISC (28)	1 Discard cells not in compliance with GCRA0 if policing. 0 Tag cells not in compliance with GCRA0 if policing.
GCRA1_EN (27)	1 Enable the GCRA1 filter. 0 Disable the GCRA1 filter.
GCRA1_POLICE (26)	1 Police according to GCRA1 parameters. 0 Monitor only; no policing actions taken.
GCRA1_DISC (25)	1 Discard cells not in compliance with GCRA1 if policing. 0 Tag cells not in compliance with GCRA1 if policing.
GCRA1_CLP (24)	1 Use CLP = 0 + 1 for GCRA1. 0 Use CLP = 0 only for GCRA1.
Not used (23:20)	Write with a 0 to maintain future software compatibility.
UPC_VP_TERM (19:18)	00 VP intermediate link. 01 VP end point. 10 VP segment end point. NOTE: This field is valid only for VP control blocks.
UPC_VC_TERM (17:16)	00 VC intermediate link. 01 VC end point. 10 VC segment end point. NOTE: This field must be "00_b" for VP control blocks.
Not used (15:12)	Write with a 0 to maintain future software compatibility.
PM_BA_EN (11)	1 PM is active in the B-to-A direction. Backward PM cells are generated. 0 PM is inactive in the B-to-A direction. Backward PM cells are not generated.

(Continued)

Field (Bits)	Description
PM_BA_CHANNEL (10:6)	If PM is active in the B-to-A direction for this channel, this is the assigned PM session number.
PM_AB_EN (5)	1 PM is active in the A-to-B direction. Forward cells are generated. 0 PM is inactive in the A-to-B direction. Forward cells are not generated.
PM_AB_CHANNEL (4:0)	If PM is active in the A-to-B direction for this channel, this field is the assigned PM session number.

8.2.2.2 T0

Offset: 2_h
Type: Read/Write
Format: Refer to the following table.

Field (Bits)	Description
GCRA0_T (31:0)	Provides the T parameter for the GCRA algorithm. Resolution is the number of clock cycles. For programming information, refer to section 9.8.2 "Determining UPC Parameters" on page 87.

8.2.2.3 τ0

Offset: 3_h
Type: Read/Write
Format: Refer to the following table.

Field (Bits)	Description
GCRA0_τ (31:0)	Provides the τ parameter for the GCRA algorithm. Resolution is the number of clock cycles. For programming information, refer to section 9.8.2 "Determining UPC Parameters" on page 87.

8.2.2.4 T1

Offset: 5_h
Type: Read/Write
Format: Refer to the following table.

Field (Bits)	Description
GCRA0_T (31:0)	Provides the T parameter for the GCRA algorithm. Resolution is the number of clock cycles. For programming information, refer to section 9.8.2 "Determining UPC Parameters" on page 87.

8.2.2.5 τ1

Offset: 6_h
Type: Read/Write
Format: Refer to the following table.

Field (Bits)	Description
GCRA1_τ (31:0)	Provides the τ parameter for the GCRA algorithm. Resolution is the number of clock cycles. For programming information, refer to section 9.8.2 "Determining UPC Parameters" on page 87.

8.2.2.6 GRCA0_DROP/TAG_CNT

Offset: 7_h
Type: Read Only
Function: Provides a count of non-compliant cells as identified by GCRA0. If GRCA0 is programmed to drop cells, this is a count of cells dropped by GCRA0. If GCRA0 is programmed to tag cells, this is a count of cells tagged by GCRA0. If GCRA0 is monitoring the cell flow, this is a count of cells detected to be in violation by the GCRA0.
Format: Refer to the following table.

Field (Bits)	Description
GCRA0_DROP/TAG_CNT (31:0)	Indicates the count of non-compliant cells tagged or dropped by the GCRA0 algorithm.

8.2.2.7 GCRA1_DROP/TAG_CNT

Offset: 8_h
Type: Read Only
Function: Provides a count of non-compliant cells as identified by GCRA1. If GRCA1 is programmed to drop cells, this is a count of cells dropped by GCRA1. If GCRA1 is programmed to tag cells, this is a count of cells tagged by GCRA1. If GCRA1 is monitoring the cell flow, this is a count of cells detected to be in violation by GCRA1.
Format: Refer to the following table.

Field (Bits)	Description
GCRA1_DROP/TAG_CNT (31:0)	Indicates the count of non-compliant cells tagged or dropped by the GCRA1 algorithm.

8.2.2.8 CLP0

Offset: 9_h
Type: Read Only
Function: Counts the cells that arrived at the WAC-186-B with CLP = 0. This count does not take into account any tagging done by the GCRA.
Format: Refer to the following table.

Field (Bits)	Description
CLP0_CELLS (31:0)	Indicates the count of CLP = 0 cells received by this channel.

8.2.2.9 TOT_CELLS

Offset: A_h
Type: Read Only
Format: Refer to the following table.

Field (Bits)	Description
TOTAL_CELLS (31:0)	Indicates the count of total cells received by the channel.

8.2.2.10 TOT_OAM_PASSED

Offset: B_h
Type: Read Only
Format: Refer to the following table.

Field (Bits)	Description
TOTAL_OAM_CELLS (31:0)	Indicates the count of OAM cells passed through by this channel. OAM cells that are identified to be at their termination point are not included in this count (refer to section 9.11.1 "Network Configuration" on page 96.)

8.2.2.11 STATUS

Offset: C_h
Type: Read Only
Function: Contains the status of the channel. Indicates the OAM states of the channel and whether a channel is active.

NOTE: For correct operation, do **NOT** write to this register after initialization.

Format: Refer to the following table.

Field (Bits)	Description
UPC_ACTIVE0 (31)	1 GCRA0 receiving cells faster than the minimum rate. 0 No cell has been received in the last x seconds, where x = $2^{29} \times$ RPHY_CLK period.
UPC_ACTIVE1 (30)	1 GCRA1 receiving cells faster than the minimum rate. 0 No cell has been received in the last x seconds, where x = $2^{29} \times$ RPHY_CLK period.
Reserved (29:27)	Write with a 0 to maintain software compatibility with future versions.
LOC_STATE (26)	1 LOC has been detected (no CC cell or user cell has been received in the last 3.5 ± .5 seconds). 0 No LOC detected.
RDI_STATE (25)	1 Receiving RDI cells. 0 No RDI cells have been received in the last 2.5 ± .5 seconds.
AIS_STATE (24)	1 Receiving AIS cells, generating RDI cells. 0 No AIS cells have been received in the last 2.5 ± .5 seconds, or a user cell or CC cell has been received since the last AIS.

(Continued)

Field (Bits)	Description
CC_GEN (23)	1 Generating CC cells under software command. 0 Not generating CC cells under software command.
CC_RCV (22)	1 Expecting CC cells under software command. 0 Not expecting CC cells under software command.
FAULT_STATE (21)	1 Generating AIS cells under software command. 0 Not generating AIS cells under software command.
FAULT_STATE2 (20)	1 Generating RDI cells under software command. 0 Not generating RDI cells under software command.
AIS/RDI END/SEG (19)	0_b Segment OAM flow for AIS/RDI cells. 1_b End-to-end OAM flow.
CC END/SEG (18)	0_b Use segment OAM flow for CC cells. 1_b Use end-to-end OAM flow for CC cells
F4/F5 (17)	Indicates the type of OAM flow to be used. 0_b For VP service, use F4 OAM flow. 1_b For VC service, use F5 OAM flow.
Reserved (16:0)	Initialize to 0. Software modifications to these locations after setup will cause incorrect operation.

8.2.2.12 VPI/VCI

Offset: D_h
Type: Read/Write
Function: Contains the header to be used with the AIS, RDI, and CC cells generated by this channel. This must be set by the host during channel activation for correct operation.
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:30)	Write with a 0 to maintain future software compatibility.
TAG (29:28)	Indicates the value of the priority tag to be sent with generated OAM cells.
GFC (27:24)	Indicates the GFC for generated OAM cells for this channel.
VPI (23:16)	Indicates the VPI for generated OAM cells for this channel.
VCI (15:0)	Indicates the VCI for generated OAM cells for this channel.

8.2.3 PM Control Block Summary

Function: The PM Control Block contains the configuration and status of the PM sessions. On start-up of a PM session, the PM_CONFIG and VPI/VCI fields must be initialized. All other fields may be initialized to "0" to provide known initialization of counts.
Organization: 32 entries
Base address: $8000F_h$
Index: 200_h

Address = *base* + (*PM channel* × *index*) + *offset*

Table 24. PM Control Block Summary

Offset	Name	Read or Write	Description
00_h	PM_CONFIG	R/W	Indicates the configuration and MCSN.
10_h	TUC	R	Indicates the number of Transmitted User Cells (CLP = 0 + 1 and CLP = 0) from the last PM report.
20_h	TRCC	R	Provides Total Received Cell Counts (CLP = 0 + 1 and CLP = 0) as of the last PM report.
30_h	BLER	R	Provides the Block Error Result from the last PM report.
40_h	CCC	R	Provides the Current Cell Count, which is the number of transmitted or received cells (CLP = 0 + 1 and CLP = 0) in the correct block.
50_h	BEDC	R	Provides the Block Error Detection Code in the current block.
60_h	VPI/VCI	R/W	Specifies the VPI/VCI for generated PM cells.
70_h	SECB	R	Indicates the Severely Errored Cell Blocks.
80_h	ERRORED_CELLS	R	Indicates the number of Errored Cells as estimated by the BLER.
90_h	$LOST\_CELLS_{0+1}$	R	Indicates the number of lost user information cells with CLP = 0 + 1.
$A0_h$	$LOST\_CELLS_0$	R	Indicates the number of lost user information cells with CLP = 0.
$B0_h$	MISINSERTED_CELLS	R	Indicates the number of misinserted user information cells.
$C0_h$	IMPAIRED_BLOCKS	R	Indicates the number of PM cell blocks containing at least one error.
$D0_h$	$TOT\_LOST\_CELLS_{0+1}$	R	Indicates the total number of lost user information cells with CLP = 0 + 1.
$E0_h$	$TOT\_LOST\_CELLS_0$	R	Indicates the total number of lost user information cells with CLP = 0.
$F0_h$	$SECB_{ERRORED}$	R	Indicates the SECB due to bit errors.
100_h	$SECB_{MISINSERTED}$	R	Indicates the SECB due to misinserted cells.
110_h	TC_{0+1}	R	Indicates the total cell count with CLP = 0 + 1.
120_h	TC_0	R	Indicates the total cell count with CLP = 0.

8.2.4 PM Control Block Bit Descriptions

8.2.4.1 PM_CONFIG

Offset: 0_h
Type: Read/Write
Function: Contains configuration information for the PM session, including the desired block size and OAM flow type.
Format: Refer to the following table.

Field (Bits)	Description
Reserved (31:24)	Initialize to 0 at setup.
MCSN (23:16)	Indicates the MCSN.
Not used (15:9)	Write with a 0 to maintain software compatibility with future versions.
PM_CELL_RECVD (8)	1 A PM cell has been received on this session. 0 No PM cells have been received on this session.
BACK_REP_GEN_EN (7)	1 If B-to-A PM, generate backward report cells. 0 If B-to-A PM, do not generate backward report cells.
FORCE_BS (6)	1_b Force transmission of PM forward OAM cells when block size is exceeded by 50 percent. 0_b Do not force transmission of PM forward OAM cells.
END/SEG (5)	0_b Use segment OAM flow. 1_b Use end-to-end OAM flow.
F4/F5 (4)	Indicates the type of OAM flow to be used. 0_b For VP service, use F4 OAM flow. 1_b For VC service, use F5 OAM flow.
BLOCK_SIZE (3:2)	00_b Block size for PM is 128 cells. 01_b Block size for PM is 256 cells. 10_b Block size for PM is 512 cells. 11_b Block size for PM is 1024 cells.
Not used (1)	Write with a 0 to maintain software compatibility with future versions.
PM_DATA_COLLECT (0)	1 Collect PM data. 0 Do not collect PM data.

8.2.4.2 TUC

Offset: 10_h
Type: Read Only
Function: Counts TUC. If B-to-A monitoring, TUC is the number of cells transmitted by B as given in the last PM forward report. If A-to-B monitoring, TUC is the information from the last backward report.
Format: Refer to the following table.

Field (Bits)	Description
TUC_{0+1} (31:16)	Counts cells with CLP = 0 + 1.
TUC_0 (15:0)	Counts cells with CLP = 0.

8.2.4.3 TRCC

Offset: 20_h
Type: Read Only
Function: Indicates the TRCC. If B-to-A monitoring, TRCC is the count of cells received as of the last PM forward report. If A-to-B monitoring, TRCC is the information from the last backward report.
Format: Refer to the following table.

Field (Bits)	Description
$TRCC_{0+1}$ (31:16)	Counts cells with CLP = 0 + 1.
$TRCC_0$ (15:0)	Counts cells with CLP = 0.

8.2.4.4 BLER

Offset: 30_h
Type: Read Only
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:8)	Write with a 0 to maintain software compatibility with future versions.
BLER (7:0)	Block Error Result (BLER) indicates the number of BIP violations detected in the last PM block. This number is calculated from forward reports or stored from the backward reports.

8.2.4.5 CCC

Offset: 40_h
Type: Read Only
Function: If B-to-A monitoring, counts current cells received. If A-to-B monitoring, counts current cells transmitted.
Format: Refer to the following table.

Field (Bits)	Description
T/RCC$_{0+1}$ (31:16)	Counts cells with CLP = 0 + 1.
T/RCC$_0$ (15:0)	Counts cells with CLP = 0.

8.2.4.6 BEDC

Offset: 50_h
Type: Read Only
Function: If B-to-A monitoring, indicates the Block Error Detection Code (BEDC) of the current block of cells received. If A-to-B monitoring, indicates the BEDC of the current block of cells transmitted.
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:16)	Write with a 0 to maintain software compatibility with future versions.
BEDC (15:0)	Indicates the BIP to date on all cells transmitted or received in the current block.

8.2.4.7 VPI/VCI

Offset: 60_h
Type: Read/Write
Function: Provides the VPI/VCI of the channel on which PM is performed. This field is used to generate the header of all PM cells generated for the PM session. This field must be properly initialized for correct operation.
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:30)	Write with a 0 to maintain future software compatibility.
TAG (29:28)	Indicates the value of the priority tag to be sent with PM OAM cells.
GFC (27:24)	Indicates the GFC for PM OAM cells for this channel.
VPI (23:16)	Indicates the VPI for PM OAM cells for this channel.
VCI (15:0)	Indicates the VCI for PM OAM cells for this channel.

8.2.4.8 SECB

Offset: 70_h
Type: Read Only
Function: Counts PM cell blocks that had more impairments than the threshold value for that type of impairment. A block is declared severely errored if:

- BLER > BLER_THRESHOLD, or
- the number of lost cells > LOSTTHRESHOLD, or
- the number of misinserted cells > MISINSERT_THRES.

Format: Refer to the following table.

Field (Bits)	Description
SECB (31:0)	Counts Severely Errored Cell Blocks (SECB) received.

8.2.4.9 ERRORED_CELLS

Offset: 80_h
Type: Read Only
Function: Estimates the number of errored cells by the number of errors in the BLER (when defined) and when BLER < BLER_THRESHOLD. BLER is defined when the number of lost or misinserted cells is 0.
Format: Refer to the following table.

Field (Bits)	Description
ERRORED_ CELLS (31:0)	Counts cells in error as calculated by BLER when valid.

8.2.4.10 $LOST\_CELLS_{0+1}$

Offset: 90_h
Type: Read Only
Function: Counts the background cell loss for CLP = 0 + 1. It is not incremented when the $TUCD_{0+1}$ > LOST_THRESHOLD.
Format: Refer to the following table.

Field (Bits)	Description
LOST_CELLS (31:0)	Counts cells detected as lost, which includes only cells from blocks not determined to be severely errored.

8.2.4.11 $LOST\_CELLS_0$

Offset: $A0_h$
Type: Read Only
Function: Counts the background cell loss for CLP = 0. It is not incremented if the number of lost cells with CLP = 0 > LOST_THRESHOLD. The number of lost cells with CLP = 0 is the smaller of $TUCD_0$ or $TUCD_{0+1}$ because some cells may have been tagged (that is, CLP = 0 switched to CLP = 1).
Format: Refer to the following table.

Field (Bits)	Description
LOST_CELLS (31:0)	Counts cells with CLP = 0 detected as lost, which includes only cells from blocks not determined to be severely errored.

8.2.4.12 MISINSERTED_CELLS

Offset: $B0_h$
Type: Read Only
Function: Counts the cells that have been misrouted or inserted into the monitored channel. It is not incremented if the number of misinserted cells > MISINSERT_THRES.
Format: Refer to the following table.

Field (Bits)	Description
MISINSERTED_CELLS (31:0)	Counts cells detected as misinserted, which includes only cells from blocks not determined to be severely errored.

8.2.4.13 IMPAIRED_BLOCKS

Offset: $C0_h$
Type: Read Only
Function: Counts the total blocks containing at least one errored cell, lost cell, or misinserted cell.
Format: Refer to the following table.

Field (Bits)	Description
IMPAIRED_BLOCKS (31:0)	Counts the impaired blocks.

8.2.4.14 $TOT\_LOST\_CELLS_{0+1}$

Offset: $D0_h$
Type: Read Only
Function: Counts the total lost cells for CLP = 0 + 1. This includes cell loss from blocks with $TUCD_{0+1}$ > LOST_THRESHOLD.
Format: Refer to the following table.

Field (Bits)	Description
LOST_CELLS (31:0)	Counts the number of lost cells detected.

8.2.4.15 $TOT\_LOST\_CELLS_0$

Offset: $E0_h$
Type: Read Only
Function: Counts the total cell loss for CLP = 0. This includes cell loss from blocks with $TUCD_0$ > LOST_THRESHOLD. The number of lost cells with CLP = 0 is the smaller of $TUCD_0$ or $TUCD_{0+1}$ since some cells may have been tagged (that is, CLP = 0 switched to CLP = 1).
Format: Refer to the following table.

Field (Bits)	Description
TC_LOST_CELLS (31:0)	Counts the total number of lost cells with CLP = 0 detected.

8.2.4.16 $SECB_{ERRORED}$

Offset: $F0_h$
Type: Read Only
Function: Counts blocks in which BLER > BLER_THRESHOLD.
Format: Refer to the following table.

Field (Bits)	Description
$SECB_{ERRORED}$ (31:0)	Counts SECBs caused by excessive BLERs.

8.2.4.17 $SECB_{MISINSERTED}$

Offset: 100_h
Type: Read Only
Function: Counts blocks in which TUCD > MISINSERT_THRES.
Format: Refer to the following table.

Field (Bits)	Description
$SECB_{MISINSERTED}$ (31:0)	Counts SECBs caused by excessive misinserted cells detection.

8.2.4.18 TC_{0+1}

Offset: 110_h
Type: Read Only
Function: Counts cells for CLP = 0 + 1 that are originated by the transmitting end point. This count is determined by examining the TUC_{0+1} in the PM reports.
Format: Refer to the following table.

Field (Bits)	Description
TC (31:0)	Counts the total of transmitted cells.

8.2.4.19 TC_0

Offset: 120_h
Type: Read Only
Function: Counts cells for CLP = 0 that are originated by the transmitting end point. This count is determined by examining the TUC_0 in the PM reports.
Format: Refer to the following table.

Field (Bits)	Description
TC (31:0)	Counts the total of transmitted cells with CLP = 0.

8.2.5 LB Control Block Summary

Function: The LB Control Block stores the information necessary to determine if an LB cell is successful. Before initiating an LB session through the FM_OAM_CMD registers, the host needs to clear the VALID bit of the RETURN_TIME register. After an LB session has ended, the host should clear all three LB control block registers to avoid capturing more LB cells.
Organization: 32 entries
Base address: $801DF_h$
Index: 200_h

Address = *base* + (LB *session* × *index*) + *offset*

Table 25. LB Control Block Summary

Offset	Name	Read or Write	Description
00_h	VPI/VCI	R	Indicates the VPI/VCI.
10_h	TX_TIME/CORR	R	Indicates the local time when a cell was scheduled for transmission.
20_h	RETURN_TIME	R/W	Indicates the local time when a returning LB cell was detected.

8.2.6 LB Control Block Bit Descriptions

8.2.6.1 VPI/VCI

Offset: 00_h
Type: Read/Write
Function: This field stores the header of the LB cell sent on this connection. The GFC/VPI, VPI, and VCI fields are used to determine if the LB cell has returned.
Format: Refer to the following table.

Field (Bits)	Description
Not used (31:30)	Write with a 0 to maintain future software compatibility.
TAG (29:28)	Indicates the value of the priority tag to be sent with generated LB OAM cells.
GFC/VPI(11:8) (27:24)	Indicates the GFC for generated LB OAM cells for this channel.
VPI(7:0) (23:16)	Indicates the VPI for generated LB OAM cells for this channel.
VCI (15:0)	Indicates the VCI for generated LB OAM cells for this channel.

8.2.6.2 TX_TIME/CORR

Offset: 10_h
Type: Read/Write
Function: When the LB cell is sent, this location holds a copy of the correlation tag sent in the LB cell. The correlation tag represents the local time that the cell was scheduled to be sent. The TX_TIME/CORR field is also used to determine if the LB cell has returned.
Format: Refer to the following table.

Field (Bits)	Description
Reserved (31)	Initialize to 0 at initial setup.
TX_TIME/CORR (30:0)	Indicates the local time when the cell was scheduled for transmission.

8.2.6.3 RETURN_TIME

Offset: 20_h
Type: Read/Write
Function: When the LB cell is received, the local time is placed in this register. By determining the difference between the return time and the transmit time, the round trip time can be calculated.
Format: Refer to the following table.

Field (Bits)	Description
VALID (31)	0 Loopback has not yet completed. 1 Loopback has completed, and the return time is valid.
RETURN_TIME (30:0)	Indicates the local time when a returning LB cell was detected.

8.2.7 VPI/VCI Connection Lookup Table Summary

Organization: 16K-256K entries
Base address: $C0000_h$
Index: 1_h

Address = *base* + (*connection* ÷ 2)

NOTES:

- Two values per entry, with the MSB the odd value and the LSB the even value.
- Connection number format is given in the description of the VPI_BITS field in section 7.2.2 "GLOBAL_CONFIG" on page 48.

Table 26. VPI/VCI Connection Lookup Table Summary

Address	Name	Read or Write	Description
0_h	CHAN	R/W	Contains the UPC channel number.

8.2.8 VPI/VCI Connection Lookup Table Bit Descriptions

8.2.8.1 CHAN

Address: 00_h
Type: Read/Write
Format: Refer to the following table.

Field (Bits)	Description
ACTIVE1 (31)	1 Enables the odd numbered connection as valid/active. 0 Disables the odd numbered connection as invalid/inactive.
Not used (30)	Write with a 0 to maintain software compatibility with future versions.
CHAN1_# (29:16)	Indicates the channel number for odd numbered connections (VPI/VCI).
ACTIVE0 (15)	1 Enables the even numbered connection as valid/active. 0 Disables the even numbered connection as invalid/inactive.
Not used (14)	Write with a 0 to maintain software compatibility with future versions.
CHAN0_# (13:0)	Indicates the channel number for even numbered connections (VPI/VCI).

9 APPLICATION NOTES

9.1 UTOPIA Interface Connections

Figure 24 on page 79 shows the UTOPIA connections of several IgT products.

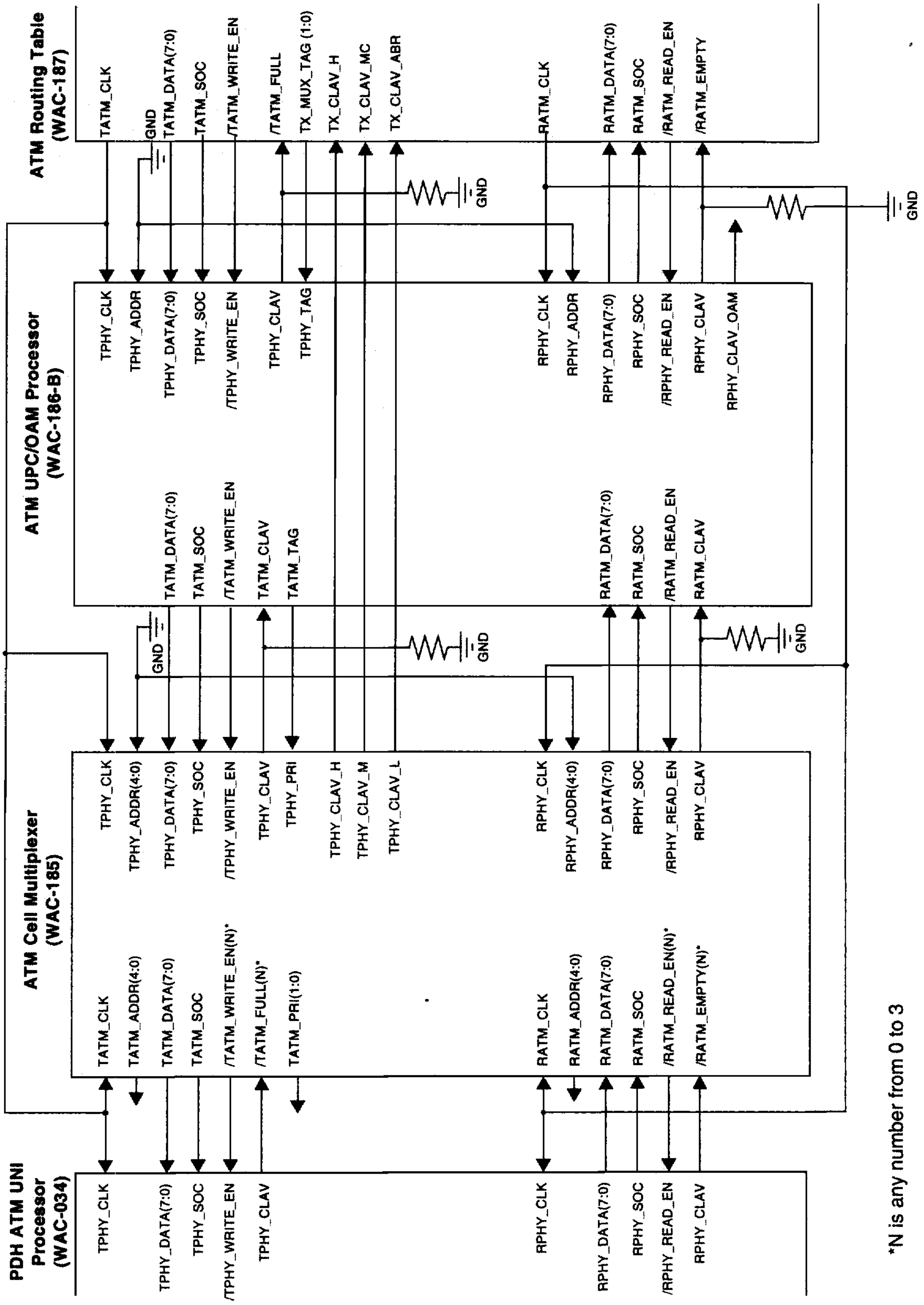


Figure 24. UTOPIA Interface Single-PHY Connections

9.2 SRAM Memory Interface

The SRAM interface is a glueless interface to a single bank of SRAMs. Not all the address bits are required for the smaller configurations. Table 27 indicates the valid SRAM bits for each possible SRAM configuration.

Table 27. Valid SRAM_ADDR Bits

SRAM Configuration	Valid SRAM_ADDR Bits
512K x 32	RAM_ADD(18:0)
256K x 32	RAM_ADD(18), RAM_ADD(16:0)
128K x 32	RAM_ADD(18), RAM_ADD(15:0)
32K x 32	RAM_ADD(18), RAM_ADD(13:0)

9.3 Using an External OAM FIFO with the WAC-186-B

The WAC-186-B processes FM and PM OAM cells. It does not process activation/deactivation and system administration OAM cells. If no device in the system (such as a WAC-187) can queue these unhandled OAM cells to a host processor, the optional WAC-186-B external FIFO interface can perform this queueing function.

To turn on the optional WAC-186-B external FIFO interface, set the OAM_RX bit in the GLOBAL_CONFIG register to 0_b (refer to section 7.2.2 "GLOBAL_CONFIG" on page 48). This optional interface easily attaches to an external FIFO, such as the Integrated Device Technology, Inc. (IDT) SyncFIFO™, as shown in Figure 25. The FIFO may then be interfaced to a microprocessor. When the WAC-186-B encounters cells that it cannot process and the optional WAC-186-B external FIFO interface is turned on, the WAC-186-B writes the unprocessed OAM cells into the external FIFO, not into the ATM layer device. Since the WAC-186-B PHY interface disregards the full flag of the FIFO, the cells destined for the FIFO are dropped if the FIFO becomes full. If a 4K FIFO is used, 77 cells may be queued to the microprocessor before cells are dropped.

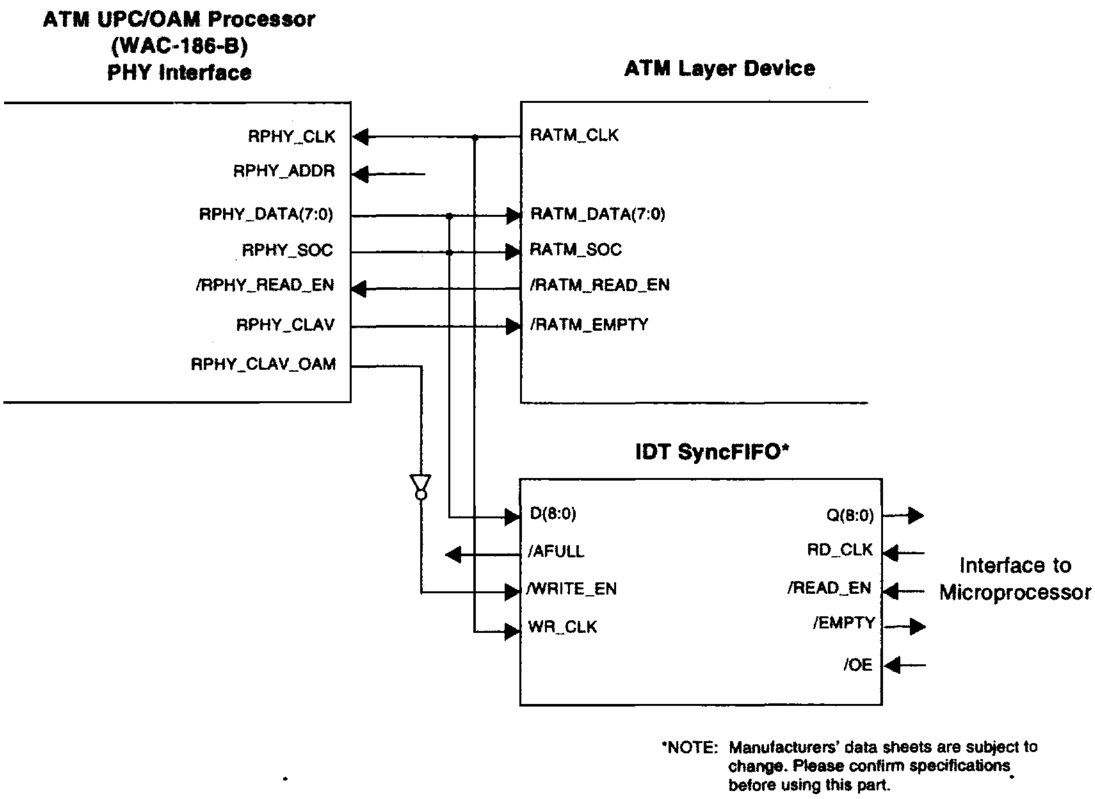


Figure 25. Using an External OAM FIFO with the WAC-186-B

9.4 Connecting the WAC-186-B and Other MPHY Layer Devices to an ATM Layer MPHY Device

As Figure 26 shows, the WAC-186-B can be easily used as an MPHY layer device, in accordance with the UTOPIA Level 2 specification (refer to Appendix B, "References", on page 108), and connected with other MPHY layer devices (for example, another WAC-186-B) to an ATM layer MPHY device. An external address decode is required. The address decode and its connections are shown in bold in Figure 27.

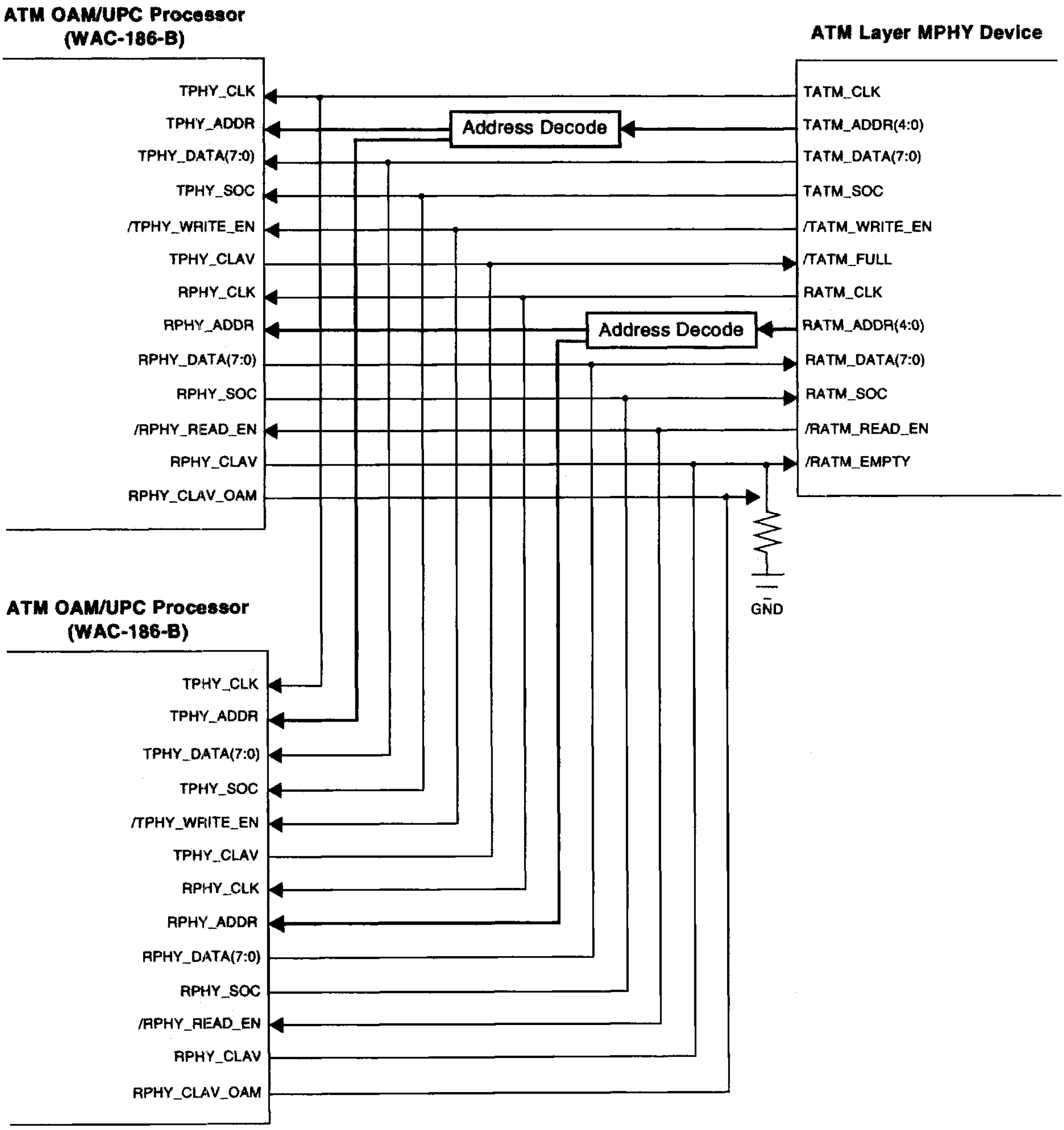
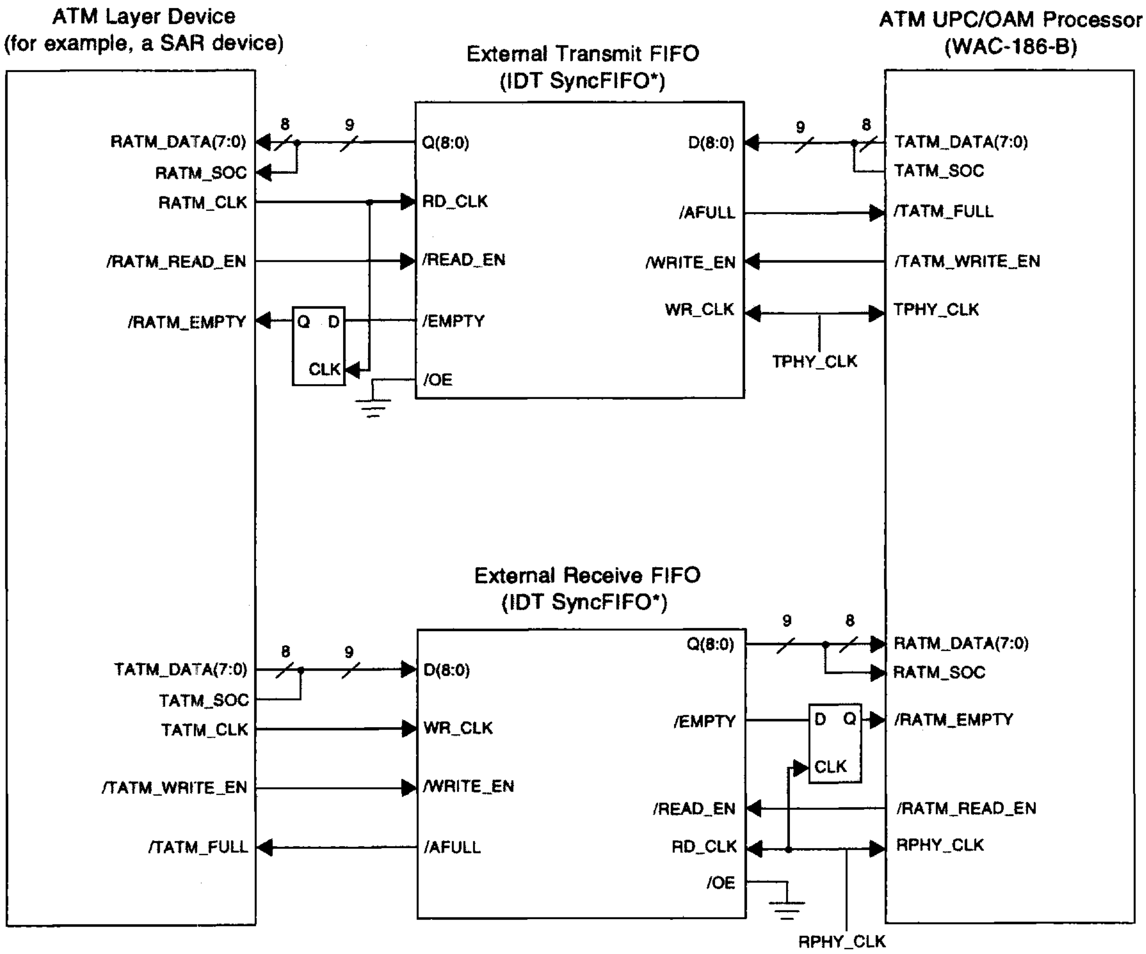


Figure 26. Connecting the WAC-186-B and other MPHY Layer Devices to an ATM MPHY Layer Device

9.5 Connecting the WAC-186-B ATM UTOPIA Interface to an ATM Layer Device

As shown in Figure 27, the WAC-186-B ATM interface can be connected to an ATM layer device by using a pair of 9-bit wide, 64-byte deep IDT SyncFIFOs. Figure 27 shows the connection of a UTOPIA-compliant ATM layer device to the WAC-186-B. When the external transmit FIFO asserts /AFULL for the WAC-186-B, the FIFO must be able to accept at least four extra writes.



*NOTE: Manufacturers' data sheets are subject to change. Please confirm specifications before using this part.

Figure 27. Connecting the WAC-186-B ATM UTOPIA Interface to an ATM Layer Device

9.6 Connecting the WAC-186-B PHY UTOPIA Interface to a PHY Layer Device

The WAC-186-B PHY interface can be connected to a PHY layer device. Figure 28 shows the connection of a UTOPIA-compliant PHY layer device to the WAC-186-B.

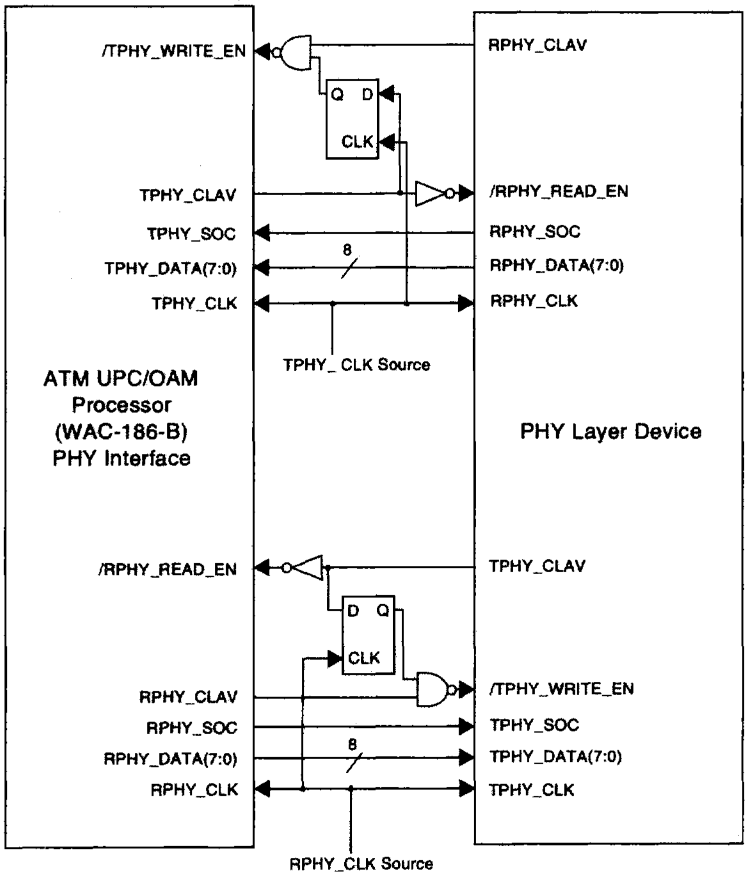
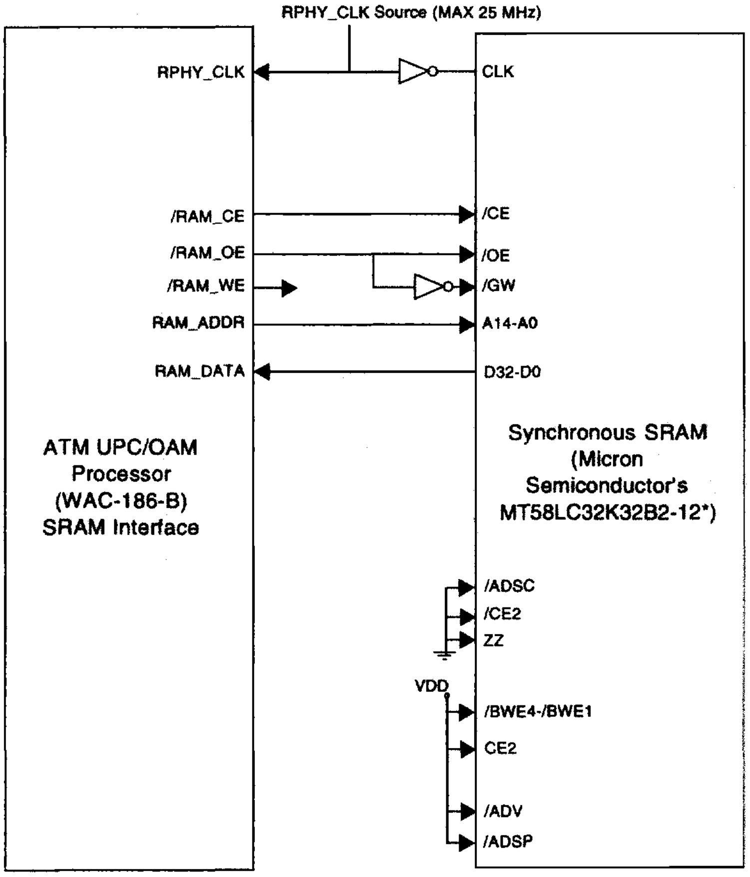


Figure 28. Connecting the WAC-186-B PHY UTOPIA Interface to a PHY Interface

9.7 Connecting the WAC-186-B to a Synchronous SRAM (SSRAM)

Although the WAC-186-B is designed to be used with asynchronous SRAMs, in some cases you can use Synchronous SRAMs (SSRAMs). The SSRAMs must have "flow-through" architecture, and care must be taken to meet all the timing requirements of the SSRAMs. Figure 29 shows the connection of the WAC-186-B to a 32K × 32 flow-through SSRAM (in this example, Micron Semiconductor's SYNCBURST™, part number MT58LC32K32B2-12). The connection shown in Figure 29 can operate at a maximum rate of 25 MHz.



*NOTE: Manufacturers' data sheets are subject to change. Please confirm specifications before using this part.

Figure 29. Connecting the WAC-186-B to a Synchronous SRAM

9.8 UPC Processing

The ATM UNI Specification version 3.1 (refer to Appendix B, "References", on page 108) defines UPC as the actions taken to monitor and control traffic. The WAC-186-B monitors and controls traffic by detecting violations of negotiated parameters and acting appropriately. The device also determines whether traffic complies with the traffic contract. The Connection Admission Control (CAC) software procedure allocates resources and derives the parameter values for the operation of the WAC-186-B.

The WAC-186-B supplies two GCRA engines. The GCRA is a continuous leaky bucket algorithm in which cells leak from the bucket at a continuous rate. The bucket state reflects the amount of time required for the bucket to empty. The bucket size is the maximum amount of time allowed for the bucket to empty.

If cells arrive faster than they leak out, the level of the bucket rises. Once the bucket becomes full, arriving cells are determined to be in violation. If cells arrive slower than they leak out, the level of the bucket sinks toward empty.

9.8.1 GCRA Required Parameters and Operation

Two parameters are necessary to specify the behavior of the GCRA algorithm:

- The first parameter, T, is the peak emission rate, which represents the leak rate of the bucket, or the amount of time one cell takes to leak out of the bucket. This parameter is usually set to represent the PCR or the SCR.
- The second parameter, τ, is the bucket limit, or the maximum amount of cells that may be in the bucket when the bucket will still accept another cell. The bucket limit determines the amount of clumping, which is defined by the maximum burst size allowed.

The GCRA uses these parameters and the current state of the bucket. The current state of the bucket is the Theoretical Arrival Time (TAT), or the time at which the bucket would be empty.

TAT = current time + time for one cell to leak out of the bucket

When a cell arrives, the state of the bucket is checked. The bucket can have one of three states:

- Empty = Current time > TAT. If the bucket is empty, the cell is accepted and T is added to the empty bucket .
- Partially Full = The bucket is not empty and TAT < current time + τ (bucket limit). If the bucket is partially full, the cell is accepted and T is added to the bucket, increasing the time until the bucket will be empty.
- Full = TAT > current time + τ. If the bucket is full, the cell is determined to be non-conforming and the bucket state is not updated.

Figure 30 shows the GCRA flowchart.

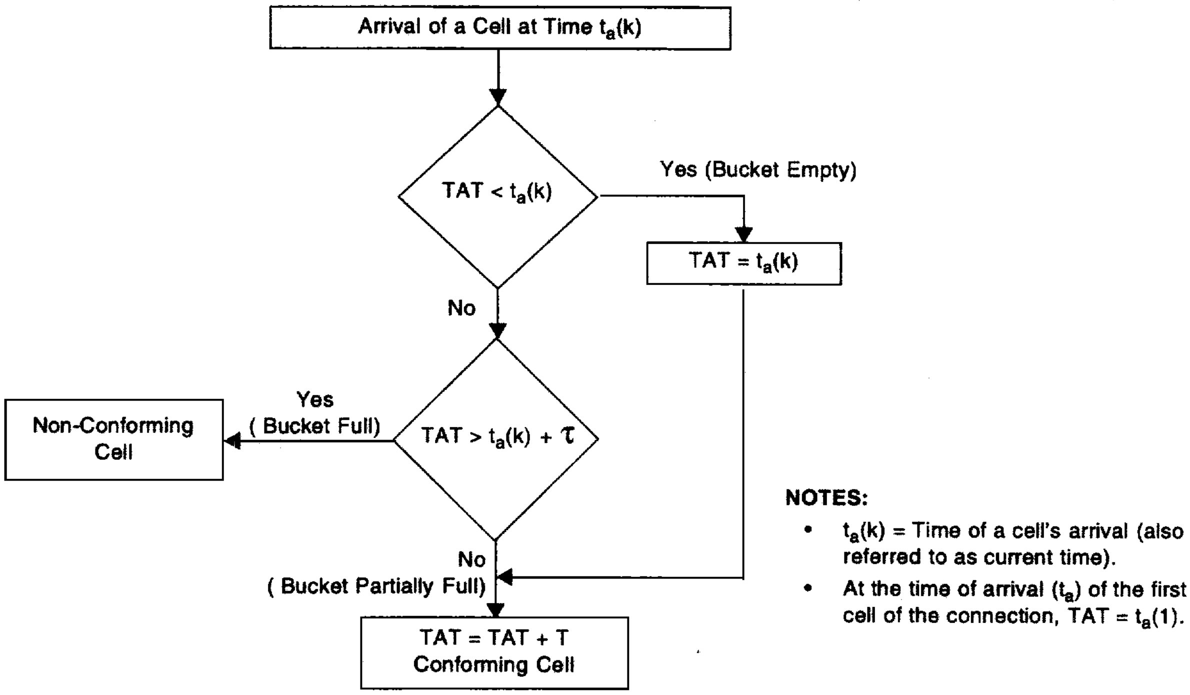


Figure 30. GCRA Flowchart

9.8.2 Determining UPC Parameters

The units for the WAC-186-B parameters are based on the RPHY_CLK clock periods. For example, for a value of 1 second when the RPHY_CLK clock rate of the WAC-186-B is 25 MHz, the programmed value should be: 1 second ÷ 40 ns = 25,000,000 = $17D7840_h$.

The parameters T and τ can range from a value of 1 (40 ns) to a maximum of 1FFFFFFF, allowing the PCR and SCR to range from less than 1 cell per second to the maximum link rate of 365,566 cells per second. The maximum window over which the SCR is calculated is 20 seconds at 25 MHz.

If traffic monitoring is required on PCR, the parameters may be assigned so that:

$$\text{Peak Emission Interval } (T_{PCR}) = \frac{\left(\frac{1}{PCR}\right)}{\text{RPHY Clock Period}}$$

$$\tau_{PCR} = \frac{\text{CDVT}}{\text{RPHY Clock Period}}$$

If traffic monitoring is required on SCR, the parameters may be assigned so that:

$$\text{Peak Emission Interval } (T_{SCR}) = \frac{\left(\frac{1}{SCR}\right)}{\text{RPHY Clock Period}}$$

$$\text{Cell Delay Variation } (\tau_{SCR}) = \frac{\text{CDVT}}{\text{RPHY Clock Period}} + \text{Burst Tolerance}$$

$$\text{Where Burst Tolerance} = (\text{Maximum Burst Size} - 1) \times (T_{SCR} - T_{PCR})$$

9.8.3 Interaction of GCRAs

The WAC-186-B supports up to two GCRA algorithms. Each algorithm is configured independently on a per-channel basis. For each channel, one or two GCRAs may be chosen. The GCRAs may be configured for policing or monitoring. When configured for policing, the GCRA logs violations and performs corrective actions. The corrective action to be taken (tag cells or drop cells) may be chosen. When configured for monitoring, the GCRA logs violations but does not take any corrective action. The second GCRA may be used for policing cells with CLP = 0 or for all cells. As explained below, the options chosen determine how the GCRAs interact with each other.

If either of the GCRAs determines that the cell is non-compliant and will be dropped, neither of the GCRAs is updated, as shown in Figure 31.

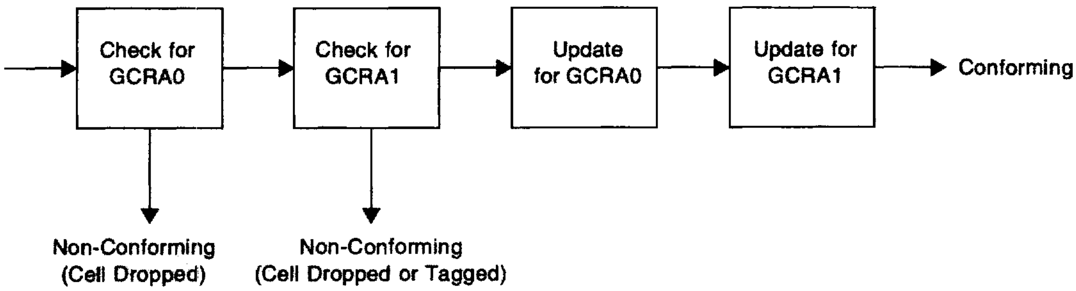


Figure 31. GCRA0 Dropping Cells, GCRA1 Dropping or Tagging Cells

However, if the first GCRA is configured to tag cells in violation, and the second GCRA is set to process cells with CLP = 0 + 1, the second GCRA processes the tagged cell, as shown in Figure 32.

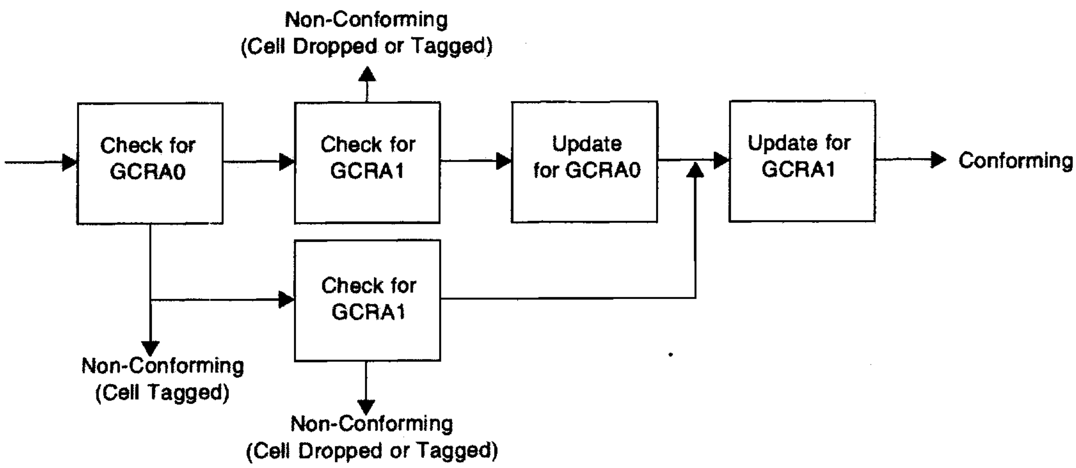


Figure 32. GCRA0 Tagging Cells, GCRA1 Dropping or Tagging Cells

If the second GCRA is configured to operate on cells with CLP = 0, it processes only the CLP = 0 cells that conform to GCRA0, as shown in Figure 33. If the CLP = 0 and either of the GCRAs determine that the cell is non-compliant and will be dropped, neither of the GCRAs is updated. If the CLP = 1, only the first GCRA examines the cell.

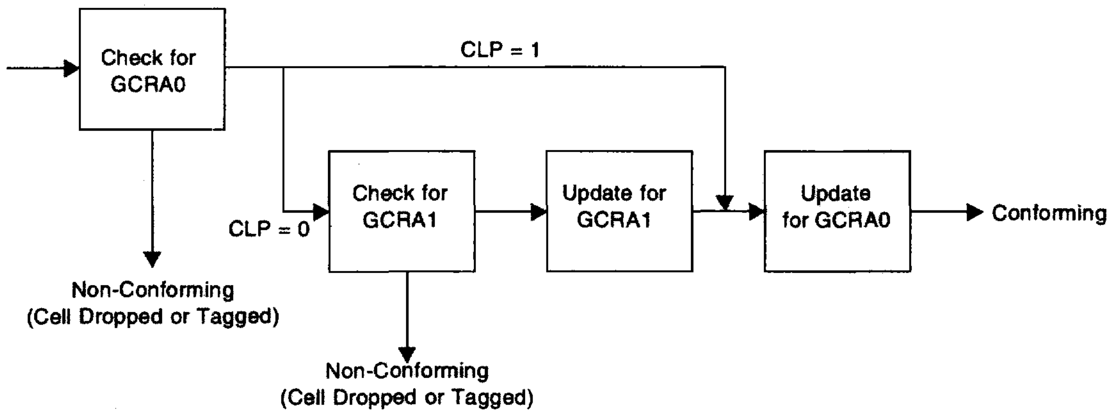


Figure 33. GCRA0 Dropping or Tagging Cells in Violation, GCRA1 Policing CLP = 0 Cells Only

9.9 Mapping Connections to Channels

9.9.1 Connections vs. Channels

A connection (or the connection range) is defined as the combination of valid VP bits and valid VC bits. The number of valid VP bits is programmable to between 5 and 12 (refer to section 7.2.2 "GLOBAL_CONFIG" on page 48). The number of valid VC bits is the difference between the number of valid VP bits and the total number of valid bits as given by the SRAM_CONFIG field of the UPC_CONFIG register (refer to "SRAM_CONFIG" on page 49).

Active channels are connections that are enabled. To enable a VC-level connection, the channel number must be placed in the lookup table and marked as active. The UPC control block for that channel number must also be initialized and configured. The number of channels available for VC-level functions is determined by the maximum channels supported minus the reserved channels (refer to section "Reserved Channels (VP-Level Connections)").

The connection range is 32 times larger than the maximum number of active channels.

9.9.2 Reserved Channels (VP-Level Connections)

One channel is reserved for each possible VP. The number of possible VPs is determined from the number of valid VP bits. The reserved channels are located at channel number = VP number. The reserved channels are used for VP-level policing and/or OAM functions. To activate VP-level monitoring, set the VP_MON bit in the UPC Control Block configuration register (refer to "VP_MON" on page 62). All possible VPs are active for OAM-level functions. In the SRAM configurations that support 1K and 4K active channels, the chip may be configured as a VP-only chip by selecting support of 12 VP bits. With the support of 12 VP bits, all available channels are reserved for VP processing.

9.9.3 Lookup Table (VC-Level Connections)

The VPI/VCI Connection Lookup Table (refer to section 8.2.7 "VPI/VCI Connection Lookup Table Summary" on page 77) provides the ability to select the desired VCs (VP/VC combinations) to be supported. The lookup table is addressed by the connection index. The connection index is the valid VC bits concatenated with the valid VP bits. Each entry in the lookup table contains a channel number that points to a UPC control block and an active/inactive indication. The active/inactive bit indicates whether the connection index is an active connection or an inactive connection. Active connections map to a channel number and to the corresponding UPC control block. Inactive connections are not activated and are optionally dropped. If they are not dropped, cells with that VPI/VCI are passed through without policing or OAM support.

Figure 34 shows the mapping from a VC channel, uniquely identified by the VPI/VCI combination, to a channel number and associated control block using the lookup table. This example assumes eight valid VP bits.

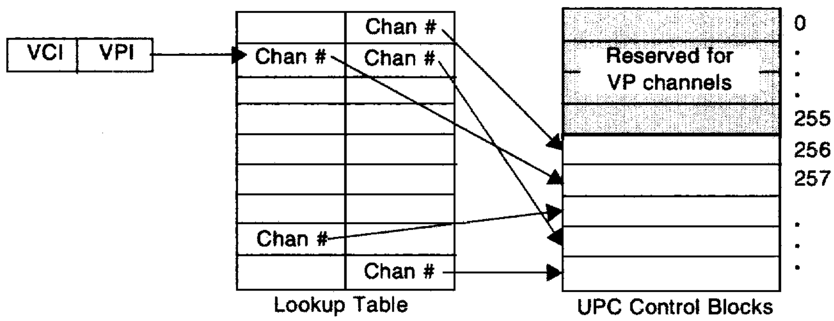


Figure 34. VC Connection Mapping

9.9.4 VP-Level Policing Versus VC-Level Policing

VP-level policing is activated by the VP_MON bit in the UPC Control Block configuration register (refer to section 8.2.2.1 "UPC_CONFIG" on page 62) in the channel reserved for VP-level operations. When a user cell arrives at the WAC-186-B, the reserved VP's UPC control block is checked to determine if VP_MON is enabled. If VP-level policing is enabled, the VC field is ignored and policing is performed using the supplied parameters. The results are stored in the reserved control block. If VP-level policing is not enabled, the WAC-186-B accesses the VPI/VCI Connection Lookup Table to find the VP/VC mapping. Thus, if VP-level policing is activated, all VCs within the VP are policed together. VP-level policing overrides any VC-level settings. While policing on the VP level, OAM functions on the VC level are supported if the applicable VCs are mapped to an active channel.

9.10 Mapping Channels on the WAC-186-B for Use with the ATM Routing Table (WAC-187)

To maximize the use of the available channels within the ATM Routing Table (WAC-187), the WAC-186-B provides a VPI/VCI translation option that compresses the VPI/VCI fields.

9.10.1 Global Setup

Set the global configuration register (refer to section 7.2.2 "GLOBAL_CONFIG" on page 48) to the following:

- VP/VC_PASS = 0 to enable VPI/VCI field translation if any VC-level switching is desired.
- DROP_OUT_OF_RANGE = 0 to disable the valid range checking if any VP-level switching is desired. This enables all possible VCs on any VP.

9.10.2 VC-Level Switching

For VC-level switching, the channel number of the VC is set via the lookup table, and VP-level monitoring is turned off for that VP. In this mode, the incoming VPI/VCI field is translated to the selected channel number.

If translating is enabled and the channel is set up for VC service, the WAC-186-B always translates the entire VPI and VCI fields. In translation, the channel number replaces the VPI and VCI bits (as defined by VPI_BITS_OUTGOING), and the remaining bits of the VPI and VCI are replaced with the value 0. If VIP_BITS_OUTGOING is "00", none of the channel number bits replace VPI bits, therefore the entire outgoing VPI field (eight bits) will be written with 0.

The channel number is divided into two parts. One part, consisting of the LSBs, is used as the outgoing VP, and the other part is used as the outgoing VC. The size of the part to be placed in the VPI field is programmable to be either 0, 6, 7, or 8, and the remaining bits are placed in the VCI field. For the WAC-187, the number of bits for the outgoing VPI field should be set to 6, and the number of valid VPI bits should also be set to 6.

The following examples show VC-level translation during three different configurations of the WAC-186-B.

The example shown in Figure 35 assumes the following parameters (refer to section 7.2.2 "GLOBAL_CONFIG" on page 48):

- SRAM_CONFIG = 01 (128K × 32K SRAM)
- VPI_BITS = 010 (use VCI(9:0), VPI(6:0) as the channel lookup table index)
- VPI_BITS_OUTGOING = 01 (place channel number bits (5:0) in VPI and bits (11:6) in VCI)
- VP/VC_PASS = 0
- UPC/OAM_EN = 1

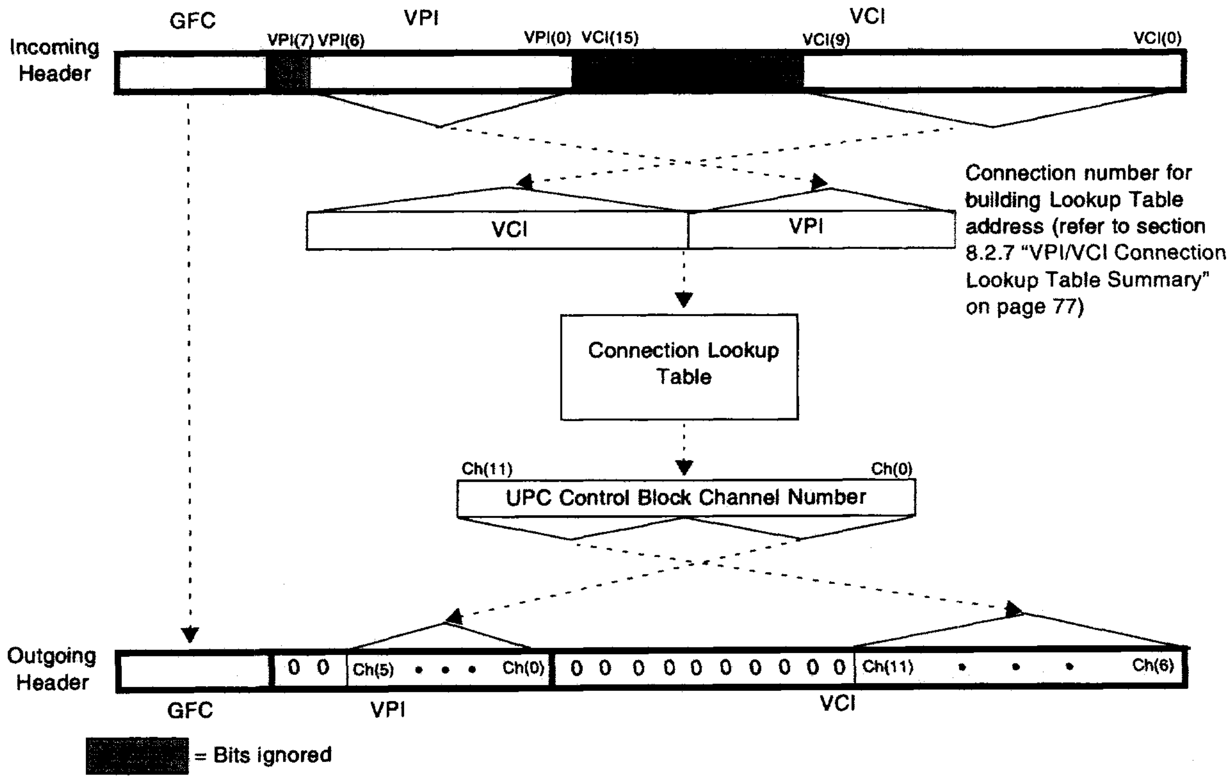


Figure 35. VC Switching Translation Example 1

The example shown in Figure 36 assumes the following parameters (refer to section 7.2.2 "GLOBAL_CONFIG" on page 48):

- SRAM_CONFIG = 01 (128K × 32K SRAM)
- VPI_BITS = 010 (use VCI(9:0), VPI(6:0) as the channel lookup table index)
- VPI_BITS_OUTGOING = 00 (place no channel number bits in VPI and channel number bits (11:0) in VCI)
- VP/VC_PASS = 0
- UPC/OAM_EN = 1

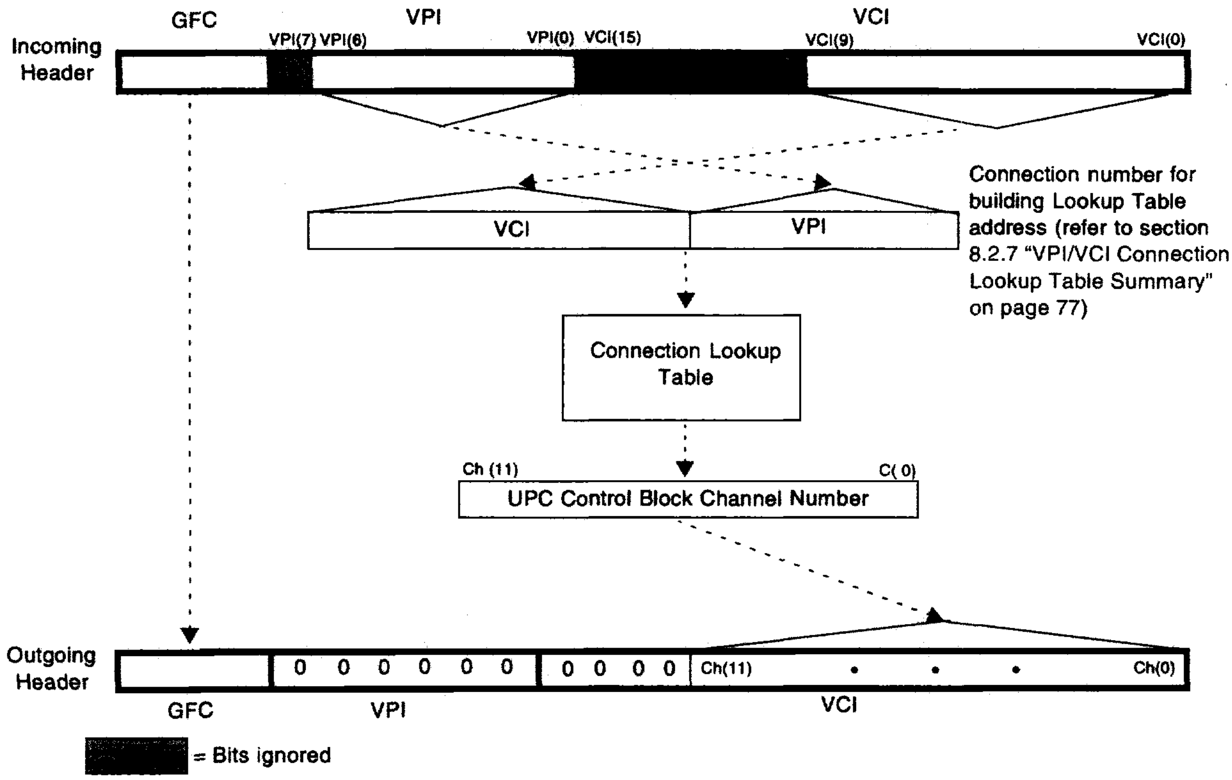


Figure 36. VC Switching Translation Example 2

The example shown in Figure 37 assumes the following parameters (refer to section 7.2.2 "GLOBAL_CONFIG" on page 48):

- SRAM_CONFIG = 10 (256K × 32K SRAM)
- VPI_BITS = 111 (use VCI(6:0), GFC(3:0), VPI(7:0) as the channel lookup table index)
- VPI_BITS_OUTGOING = 11 (place channel number bits (7:0) in VPI and bits (12:8) in VCI)
- VP/VC_PASS = 0
- UPC/OAM_EN = 1

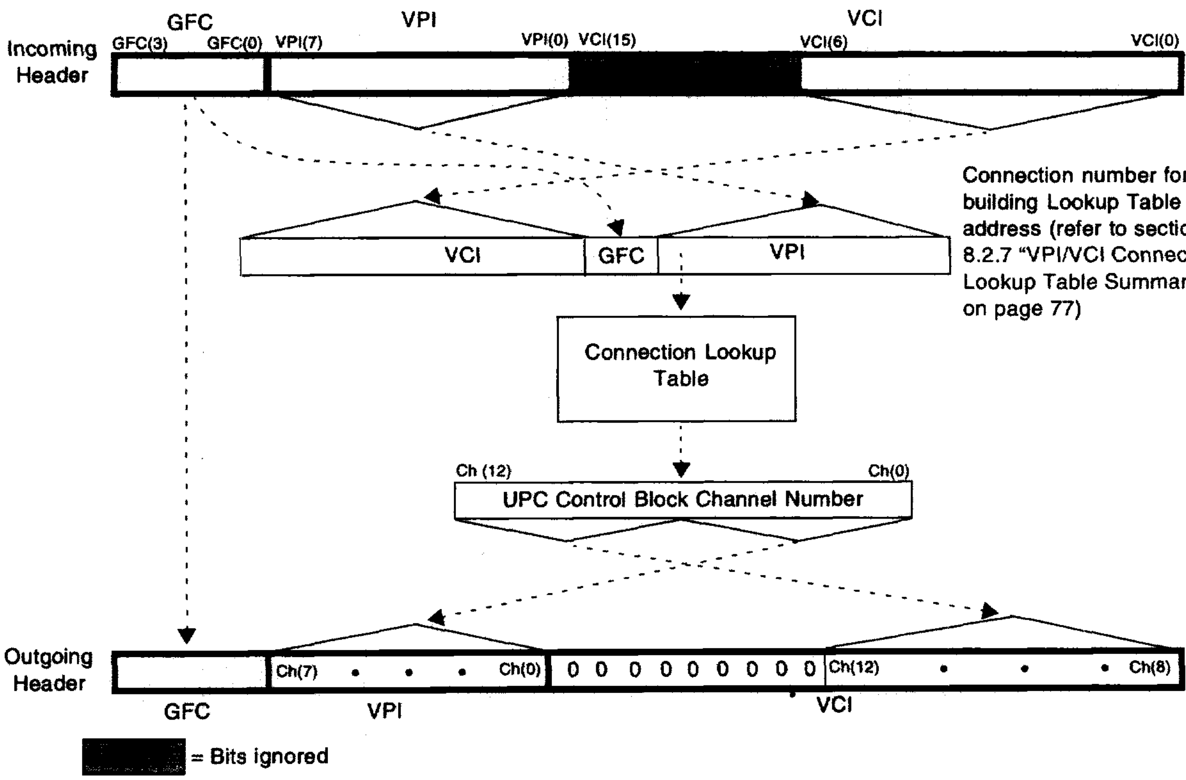


Figure 37. VC Switching Translation Example 3

9.10.3 VP Switching Connections

When VP-level switching is desired, the control block at the reserved channel for VP processing (channel number = VP) should be set to police that VP on a VP level. This will disable the translation of the VPI/VCI field for that VP.

When connections that are switched on the VP level and the VC level are present within the same part, channel numbers must be allocated carefully. When a VP is designated for VP switching, software must ensure that the channel numbers that would translate to that particular VP are not currently allocated.

Figure 38 shows the mapping function and the reserved mapping locations when a VP is configured for VP switching.

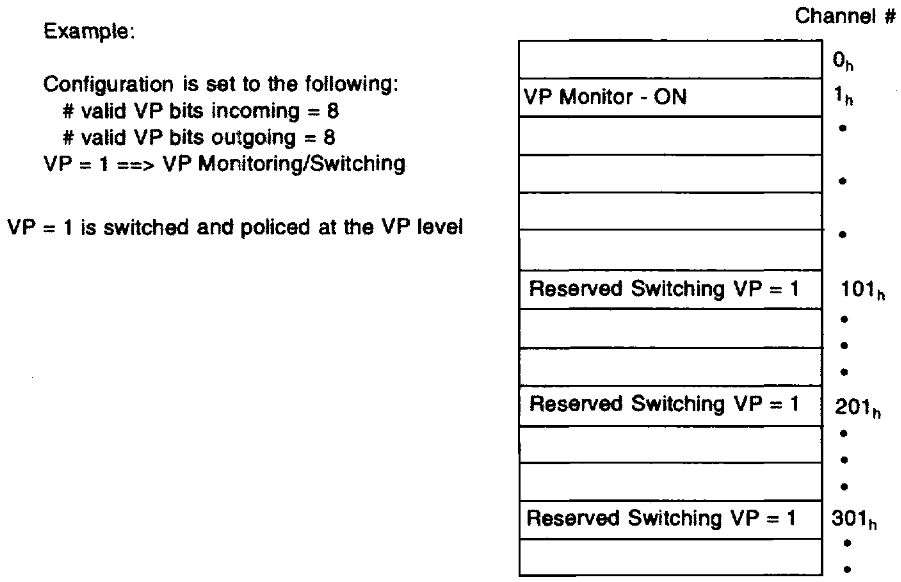


Figure 38. VP Switching Reservations During Translation

9.10.4 OAM Processing

The WAC-186-B can perform all VP-level OAM processing except for activation/deactivation and system management. If the WAC-187 is performing the VC-level switching, IgT recommends using the WAC-187 to queue the unsupported cell types to the processor. The WAC-187 cannot terminate any OAM cells if it is performing VP-level switching. In this situation, network management must perform activation/deactivation for continuity checking and performance monitoring.

9.10.5 Summary

The total number of VP/VCs that the combination of the WAC-186-B and the WAC-187 can support is determined by the following:

4096 = 8 × #VPs switched as entire VPs
+ #VCs switched as VCs
+ # of reserved by the WAC-186-B for VPs given by $2^{\text{NUMBER OF INCOMING VALID VP BITS}}$
+ # of reserved VCs (for example, signaling OAM)

9.11 OAM Functions

9.11.1 Network Configuration

For OAM support, the WAC-186-B must be programmed with knowledge of the network configuration. The location of the segment points and end points of both the VCs and VPs are important to the OAM flow. When a channel is set up, it must be configured as an end point, segment point, or intermediate point. This information determines where to terminate and strip the OAM flow. All channels will ignore OAM flows not intended for them. For example, if a VP is configured as a segment point, it ignores all end-to-end F4 flows. If a VP is configured as an intermediate point, it ignores all incoming OAM flows but can generate alarms (for example, an AIS). If a VP is configured as an end point, it terminates both segment and end-to-end flows. However, if both segment and end-to-end OAM flows of the same type are occurring simultaneously, the first to commence is supported and the second one is identified as an unexpected OAM cell, dropped from the cell stream, and optionally passed to the external OAM cell FIFO for processing by the host processor. VC flows exhibit the same behavior in relationship to F5 flows.

9.11.2 F4/F5 Support

The WAC-186-B supports four types of OAM flows:

- F4 Segment
- F4 End-to-end
- F5 Segment
- F5 End-to-end

The WAC-186-B sources and sinks only one type of flow per channel. F4 and F5 flows are supported on different channels and are independent of each other. F4 flows are supported via the dedicated VP channels and the F5 flows are supported via the remaining VC channels. For support of F5 flows, a channel must be set-up for that VPI/VCI.

9.11.3 AIS and RDI Support

AIS/RDI OAM cells are supported on every active channel simultaneously.

9.11.3.1 AIS Generation and RDI Generation

Software controls all AIS cell generation and may control RDI cell generation. A connection may be desired to generate RDI cells directly without receiving AIS cells if the end point of the connection detects a defect condition. When the WAC-186-B receives a software command to start generating AIS or RDI cells, the chip generates the first cell within 0.5 seconds, and then generates cells at an average frequency of one cell per second. Cell generation continues until stopped by a software command.

9.11.3.2 AIS Reception and RDI Generation

The WAC-186-B indicates the termination of an AIS cell on a channel by transitioning into the AIS state on that channel. The channel remains in the AIS state until a valid user cell is received, a CC cell is received, or no further AIS cells have been received for 2.5 ± 0.5 seconds. While a channel is in the AIS state, it transmits RDI cells in the downstream direction at an average frequency of one cell per second. The first RDI cell will be sent within 0.5 seconds of the transition into the AIS state. A transition into or out of the AIS state optionally causes an interrupt to occur.

9.11.3.3 RDI Reception

The WAC-186-B indicates the termination of an RDI cell on a channel by transitioning into the RDI state on that channel. The channel remains in the RDI state until no further RDI cells have been received for 2.5 ± 0.5 seconds. A transition into or out of the RDI state optionally causes an interrupt to occur.

9.11.4 CC Support

CC cells are supported on every active channel simultaneously. The WAC-186-B may be enabled to detect and/ or generate CC cells. The device generates CC cells at an average frequency of one cell per second. When the WAC-186-B is enabled to detect CC cells, it sets an LOC state on a channel if no user or CC cells are received on that channel within 3.5 ± 0.5 seconds. The channel exits the LOC state when it receives a valid user cell or a CC cell. A transition into or out of the LOC state optionally causes an interrupt.

9.11.5 Loopback Support

The WAC-186-B supports the insertion of LB cells at segment points and end points. Support for LB cell insertion at intermediate points requires the use of the optional extended loopback feature (refer to section 7.2.2 "GLOBAL_CONFIG" on page 48.) When an LB cell is inserted in a connection at its source point, the LB indication field has a value of 1. When an LB cell is received with the LB indication field equal to 1, the cell is at its loopback point. At this point, the LB indication field is changed to a 0 and the cell is sent back toward its source. When an LB cell is received with an LB indication equal to 0, the LB cell is at its termination point. At the termination point, the correlation tag is checked. If it matches the originating correlation tag, the loopback is determined to be successful. In the WAC-186-B, loopback has two parts, as shown in Figure 39:

- The source/termination point
- The loopback point

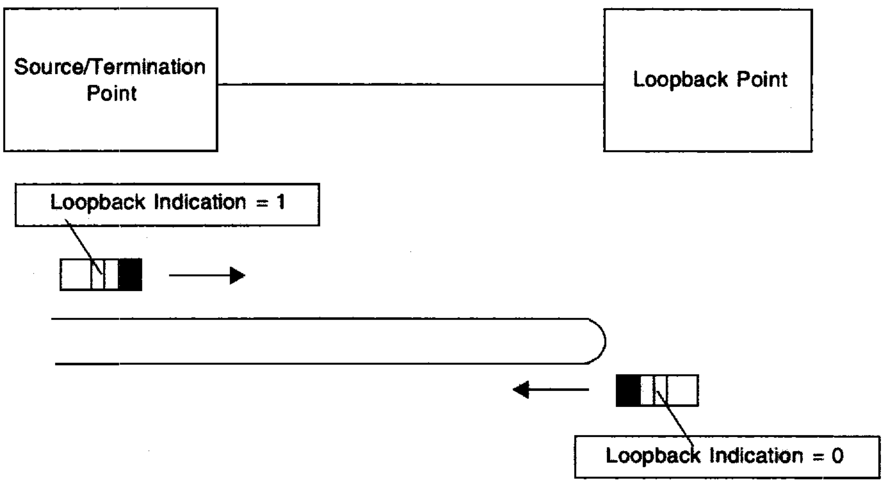


Figure 39. Loopback Indication Function

9.11.5.1 Source/Termination Point

The WAC-186-B supports loopback source/termination points for 32 channels simultaneously. Any active channel may be a loopback source/termination point. The 32 simultaneous loopbacks are each assigned a session number. When a software command initiates an LB cell, the desired loopback session number is required (0-31). Software tracks which LB sessions are in use. When an LB cell is initiated, the WAC-186-B stores the VPI/VCI of the transmitted cell and the local time that the cell was scheduled for transmission in the LB Control Block for that session. The correlation tag placed in the LB cell is the 5-bit session number concatenated with the 27 LSBs of the local time (refer to section 8.2.6.2 "TX_TIME/CORR" on page 76). When an LB cell is received and detected to be at its termination point, the GFC/VPI/VCI and correlation tag are compared to the stored values. If a match occurs, the loopback is determined to be completed and the local time of the LB cell reception along with an indication of valid completion are stored in the LB session. An interrupt is optionally generated at the completion of the loopback procedure.

NOTE: Since all fields in the header are checked with the fields sent on LB cell processing within the WAC-186-B, the user must ensure that the GFC/VPI(11:8) value that is received is the same as the one that is transmitted.

9.11.5.2 Loopback Point

When the WAC-186-B receives an LB cell with an LB indication field of 1, the LB cell is determined to be at its loopback point. The WAC-186-B supports LB cells at their loopback points for all active channels. Loopback support at the loopback point is limited only by the transmit/receive rate mismatch. The WAC-186-B may store a maximum of three LB cells. LB cells have the highest priority for transmission, thus, if the transmit side is experiencing back pressure and does not send the LB cells, LB cells will be dropped after three cells have been queued. If no back pressure is experienced, no LB cells will be lost.

9.11.5.3 Extended Loopback Support

Extended loopback support uses the optional source ID and the optional loopback ID to allow loopback cells to be inserted and/or looped back at intermediate points in the circuit. When an LB cell is received and the extended loopback feature (EXTENDED_LB) is enabled, the loopback ID and the source ID in the cell are compared with the local source ID. If either match, the cell is removed and processed.

9.11.6 Performance Monitoring (PM) Support

The WAC-186-B supports unidirectional PM on up to 32 channels simultaneously. PM cell generation is supported according to ITU I.610 (refer to Appendix B, "References", on page 108). Data collection is optionally performed on both forward PM reports and backward PM reports. Data is accumulated for the following:

- SECBs
- Errored cells
- Lost cells for CLP = 0 + 1
- Lost cells for CLP = 0
- Misinserted cells
- Impaired blocks
- Total lost cells for CLP = 0 + 1
- Total lost cells for CLP = 0
- SECBs due to errored cells
- SECBs due to misinserted cells
- Total cells with CLP = 0 + 1
- Total cells with CLP = 0

All data collection is stored as 32-bit values, allowing over 2.5 hours of PM data collection at maximum cell rate before the values rollover.

9.11.7 Activation/Deactivation and User-User System Management Support

Insertion of activation/deactivation and user-user system management OAM cells may be accomplished with the TX_OAM_FIFO. The WAC-186-B loads the desired cell into the FIFO, then a software command is issued to transmit the cell. Cell reception may be accomplished by programming the WAC-186-B to place unrecognized OAM cells in an external FIFO. The software then reads and processes the FIFO.

9.11.8 OAM Summary Tables

Table 28 and Table 29 on page 100 summarize how the WAC-186-B handles OAM cells in different configuration modes.

Table 28. How VC OAM Cells are Handled in the Different VC Configuration Modes

VC OAM Cell Type	VC Configuration Mode		
	VC Intermediate Point	VC Segment Point	VC End-to-End Point
Activation/Deactivation and System Management VC(F5) segment and end-to-end cells	Passed transparently	Not handled (optionally removed from cell stream)	Not handled (optionally removed from cell stream)
AIS/RDI VC(F5) segment and end-to-end cells	Passed transparently	Segment cells handled (removed from cell stream); end-to-end cells passed transparently	Handled (removed from cell stream)**
PM VC(F5) segment and end-to-end cells	Passed transparently	Segment cells handled (removed from cell stream); end-to-end cells passed transparently	Handled (removed from cell stream)**
LB VC(F5) segment and end-to-end cells	Passed transparently*	Segment cells handled (removed from cell stream); end-to-end cells passed transparently	Handled (removed from cell stream)
CC VC(F5) segment and end-to-end cells	Passed transparently	Segment cells handled (removed from cell stream); end-to-end cells passed transparently	Handled (removed from cell stream)**

NOTES: *LB cells with matching Loopback Location ID or Source ID may be handled if the WAC-186-B has Extended Loopback enabled.
** Only one OAM cell of either segment or end-to-end flow type may be handled at a given time. If two flows exist; the second one is not handled and may be optionally dropped.

Table 29. How VP OAM Cells are Handled in the Different VP Configuration Modes

VP OAM Cell Type	VP Configuration Mode		
	VP Intermediate Point	VP Segment Point	VP End-to-End Point
Activation/Deactivation and System Management VP(F4) segment and end-to-end cells	Passed transparently	Not handled (optionally removed from cell stream)	Not handled (optionally removed from cell stream)
AIS/RDI VP(F4) segment and end-to-end cells	Passed transparently	Segment cells handled (removed from cell stream); end-to-end cells passed transparently	Handled (removed from cell stream)**
PM VP(F4) segment and end-to-end cells	Passed transparently	Segment cells handled (removed from cell stream); end-to-end cells passed transparently	Handled (removed from cell stream)**
LB VP(F4) segment and end-to-end cells	Passed transparently*	Segment cells handled (removed from cell stream); end-to-end cells passed transparently	Handled (removed from cell stream)
CC VP(F4) segment and end-to-end cells	Passed transparently	Segment cells handled (removed from cell stream); end-to-end cells passed transparently	Handled (removed from cell stream)**

NOTES: * LB cells with matching Loopback Location ID or Source ID may be handled if the WAC-186-B has Extended Loopback enabled.
** Only one OAM cell of either segment or end-to-end flow type may be handled at a given time. If two flows exist, the second one is not handled and may be optionally dropped.

9.12 Programmers' Notes

The ATM UPC/OAM Processor Software Driver (WAC-186-DRV) is available from IgT. The software driver provides an Application Programmers' Interface (API) to easily perform the operations described in this section.

9.12.1 Setting Up a UPC VC Monitoring Session

1. Check the VP UPC control block (reserved location) to determine if the VP-level monitoring is currently enabled. Either VP-level monitoring OR VC-level monitoring can be performed. If the UPC is configured such that VP-level monitoring is enabled, only VP-level UPC functions will be performed.
2. Choose an unused channel number.
3. Calculate the desired GCRA coefficients.
4. Initialize the UPC Control Block at the chosen channel number:
   - Load the four GCRA coefficients. The GCRA coefficient offsets are 2_h, 3_h, 5_h, and 6_h.
   - Initialize all five counters (viol0, viol1, cells, oam, clp0) to 0. The counter offsets are 7_h, 8_h, 9_h, A_h, and B_h.
   - Initialize the status field to 0. The offset for the status field is C_h.
   - Initialize the VPI/VCI field to VPI/VCI and tag/priority of the session. The offset for the VPI/VCI field is D_h.
   - Initialize the UPC_CONFIG register (refer to section 8.2.2.1 "UPC_CONFIG" on page 62). The offset for the UPC_CONFIG register is 0_h.
5. Initialize the VPI/VCI Connection Lookup Table to point to the chosen channel number and activate the channel.

9.12.2 Setting Up a UPC VP Monitoring Session

1. Calculate the desired GCRA coefficients.
2. Initialize the UPC Control Block at VP reserved channel number:
   - Load the four GCRA coefficients. The GCRA coefficient offsets are 2_h, 3_h, 5_h, and 6_h.
   - Initialize all five counters (viol0, viol1, cells, oam, clp0) to 0. The counter offsets are 7_h, 8_h, 9_h, A_h, and B_h.
   - Initialize the status field to 0. The offset for the status field is C_h.
   - Initialize the VPI/VCI field to VPI/VCI and tag/priority of the session. The offset for the VPI/VCI field is D_h.
   - Initialize the UPC_CONFIG register (refer to section 8.2.2.1 "UPC_CONFIG" on page 62). The offset for the UPC_CONFIG register is 0_h.

9.12.3 Enabling OAM VC Functions on Channels Policed at the VP Level

1. Choose an unused channel number. If translating, this chosen unused channel number can be a channel within the restricted VP translation entries.
2. Initialize the UPC Control Block at the chosen channel number:
   - Initialize status to 0.
   - Initialize VPI/VCI field to VPI/VCI and tag/priority of session.
   - Initialize the PM_CONFIG register (refer to section 8.2.4.1 "PM_CONFIG" on page 68).
3. Initialize the VPI/VCI Connection Lookup Table to point to the chosen channel number and activate the channel.

9.12.4 Setting Up a VP PM Session

1. Choose an unused PM session.
2. Initialize the PM Control Block:
   - Initialize all fields to 0.
   - Initialize VPI/VCI field to VPI/VCI and tag/priority of session.
3. Initialize the UPC_CONFIG register (refer to section 8.2.2.1 "UPC_CONFIG" on page 62) of the reserved UPC Control Block for that VP to point to the PM session.

9.12.5 Setting Up a VC PM Session

1. Choose an unused PM session.
2. Initialize the PM Control Block:
   - Initialize all fields to 0.
   - Initialize VPI/VCI field to VPI/VCI and tag/priority of session.
3. Initialize the UPC_CONFIG register (refer to section 8.2.2.1 "UPC_CONFIG" on page 62) of UPC Control Block at the channel number of the VP/VC to point to the PM session.

10 FREQUENTLY ASKED QUESTIONS

Question 1: Is it possible to choose which VCI bits to look at?

Answer: No, active VCI bits are always the least significant bits.

Question 2: Is it possible to completely ignore all VCI bits and perform all functions on a VP level?

Answer: Yes. To configure the WAC-186-B to perform functions on the VP level and ignore the VCI bits, disable the range-checking function via the DROP_OUT_OF_RANGE field in the microprocessor configuration register at address 1_h (refer to section 7.2.2 "GLOBAL_CONFIG" on page 48).

Question 3: Is OAM insertion and extraction possible only to and from the line interface and not from the switch side?

Answer: Yes. OAM, AIS, RDI, and CC cells can be transmitted and received (when received processed) on the ATM interface side of the WAC-186-B that is toward the PHY layer device (for example, the WAC-034 PDH ATM UNI Processor). The WAC-186-B can not generate and process on the PHY interface side that is toward the ATM device (switch fabric side) (see Figure 24 on page 79). To send OAM cells to both sides of the circuit, you would need two WAC-186-Bs, where one of the devices is connected "backward", as shown in Figure 27 on page 83.

Question 4: Can the numbers of detected AIS, RDI, and CC cells be read out externally? If so, is the counter cleared after read out?

Answer: Only the OAM cells that are not processed and pass through the WAC-186-B are counted. The counter does not clear on read (refer to section 8.2.2.10 "TOT_OAM_PASSED" on page 65). If OAM cells, such as AIS, RDI, and CC, are processed, these cells are not counted and can not be externally extracted.

Question 5: What happens to unhandled OAM cells?

Answer: Unhandled OAM cells will route to either an external FIFO or a routing table. Unhandled OAM cells are not counted.

Question 6: Does OAM extraction require an external FIFO?

Answer: If you are using IgT's ATM Routing Table (WAC-187), no external FIFO is necessary. If you are not using the WAC-187, the external FIFO interface is provided for extracting activation/deactivation and system management OAM cells. System administration OAM cells refer to user-user system management OAM cells (refer to Table 1 on page 15).

Question 7: What happens if cells are directed to the external FIFO interface but no FIFO is implemented?

Answer: As in the case when the external FIFO is full, cells will be dropped if no external FIFO is implemented.

Question 8: When the WAC-186-B is placed between IgT's ATM Cell Multiplexer (WAC-185) and the WAC-187, how could the WAC-185 prioritize cells transmitted from the WAC-187?

Answer: The cell priority is carried on the TX_MUX_TAG bus of the WAC-187. This priority is carried, along with the cell, through the WAC-186-B, although the WAC-186-B does not use it. The WAC-186-B then delivers the priority to the WAC-185.

Question 9: Can I connect a cell-level handshaking device to the receive/transmit ATM UTOPIA interface of the WAC-186-B?

Answer: Yes, the receive/transmit ATM UTOPIA interface of the WAC-186-B can connect to both cell-level handshaking and octet-level handshaking devices.

Question 10: Can I connect a cell-level handshaking device to the receive/transmit PHY UTOPIA interface of the WAC-186-B?

Answer: Yes, the receive/transmit PHY UTOPIA interface of the WAC-186-B can use both octet-level and cell-level handshaking devices.

Question 11: I am using the WAC-186-B with the rest of IgT's ATM family of devices, which supports a 25 MHz UTOPIA bus. What are the consequences of using the WAC-186-B with a 25 MHz TPHY_CLK and RPHY_CLK instead of the maximum 33 MHz? How will this affect the performance parameters specified in this user's manual?

Answer: There are no consequences. The performance parameters are not affected. The only issue in considering the UTOPIA clock rate is the throughput, or cell bandwidth. The WAC-186-B requires at least 19.073 MHz to reach a full OC-3c bandwidth (based on one overhead cycle in transferring cells).

Question 12: If PM is inactive in the A-to-B and B-to-A directions, how will it affect the received PM cells for a VP segment point, a VC segment point, a VP end point, and a VC end point?

Answer: A and B are the PM handshake reference points. Segment cells are terminated at the segment point and end cells are terminated at the end point. Terminated refers to cell dropping on the receive side. Refer to the ITU 1.610 recommendation and the ATM Forum B-ICI 2.0 specification (refer to Appendix B, "References", on page 108) for details of performance monitoring.

Question 13: When internally generated or transmit FIFO OAM cells are transmitted, will they be regarded as misinserted cells in the PM session?

Answer: The WAC-186-B PM session counts only user cells. If internally generated OAM cells or transmit FIFO cells with OAM format are sent, they will not be interpreted as misinserted cells.

Question 14: Can the WAC-186-B interface with a non-compliant UTOPIA UNI device?

Answer: The WAC-186-B is designed to interface with UTOPIA-compliant devices, such as IgT's 51/155 Mbps SONET ATM UNI Processor (WAC-013), the Quad 51/155 Mbps SONET ATM UNI Processor (WAC-413), and the PDH ATM UNI Processor (WAC-034). Additional buffer/FIFO circuits must be designed in for non-UTOPIA-compliant devices.

Question 15: Can you suggest some SRAM parts for use with the WAC-186-B?

Answer: Various manufacturers' SRAM can be used with the WAC-186-B, including Samsung's MK681002, Motorola's MCM622B, and Micron Semiconductor's MT5C2568P.

NOTE: Manufacturers' data sheets are subject to change. Please confirm specifications before using these parts.

Question 16: What is the typical frequency at which the SRAMs run? The total current for a WAC-186-B chip and four SRAMs can be as high as 1.0 A. If it is 1.0 A, then for a 16-port switch with a WAC-186-B on all ports, the total current for the WAC-186-Bs alone will be 16.0 A.

Answer: The maximum frequency of SRAM accesses is one per cycle, or a maximum of 25 MHz for a throughput of 195 Mbps. The typical frequency depends on the traffic characteristics and the system design characteristics. For example, typical frequency is affected by the type of policing (single or dual GCRA), the amount of performance monitoring, the amount of microprocessor access to the memory, and the amount of data.

If you chose the MT5C2568P (32K × 8) from Micron Semiconductor, Inc., the typical power is 100 mA, which drops to about 80 mA when adjusted for the cycle time of 40 ns (according to TN-05-07 in the Micron 1995 SRAM data book). Therefore:

Total current = 200 + 4 × 80 = 520 mA per WAC-186-B + 4 SRAMS.

Also, depending upon your line rate, you can drop the operating frequency. For example, 20 MHz will still maintain 155 Mbps throughput, and you can use even lower frequencies for lower-speed ports.

Question 17: Are all counters per channel or global per device?

Answer: All counters are per channel.

Question 18: What should we set the CDVT to?

Answer: This value is system-dependent, but a typical value is 50 µs.

APPENDIX A NOMENCLATURE

A.1 Definitions

In this document, OAM cells are referred to by function type rather than by cell type. Refer to Table 1 on page 15 for more information.

A.2 Signal Name Prefixes

All pins and alarm names in the WAC-186-B have prefixes indicating the functional layer they implement (refer to Table 30).

Table 30. Prefixes and Associated Functional Layers

Pin Name Prefix	Associated Functional Layer
RATM	Receive UTOPIA ATM Layer. These signals should be connected to the PHY layer.
TATM	Transmit UTOPIA ATM Layer. These signals should be connected to the PHY layer.
RPHY	Receive UTOPIA PHY Layer. These signals should be connected to the ATM layer.
TPHY	Transmit UTOPIA PHY Layer. These signals should be connected to the ATM layer.

Figure 40 shows example connections between several IgT ATM and PHY layer devices. It illustrates how the signal name prefixes help indicate a signal's function and the type of device or interface to which it is connected.

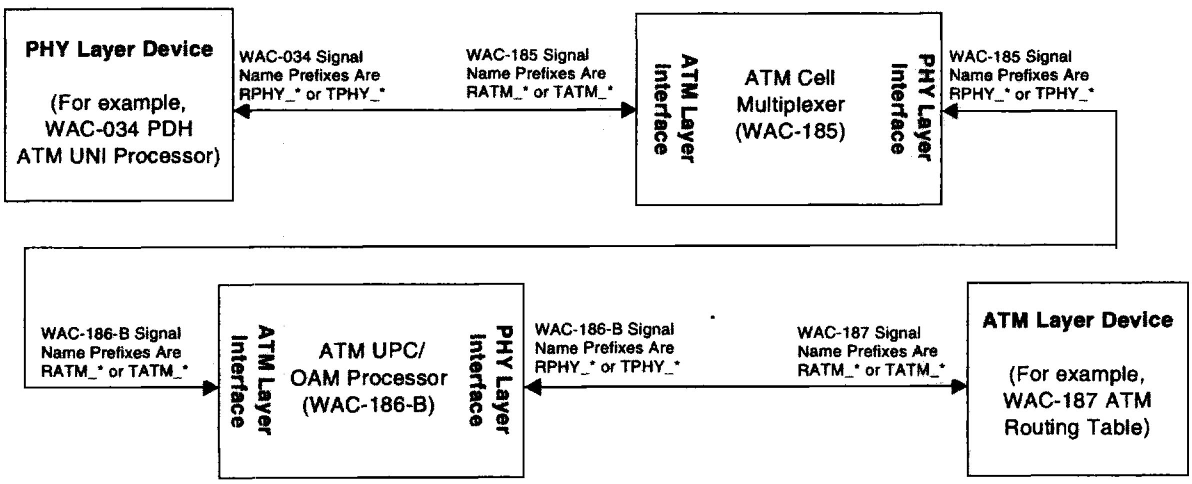


Figure 40. How Signal Name Prefixes are Determined

A.3 Numbers

- Hexadecimal numbers are followed by the suffix "$_h$", for example: 1_h, $2C_h$.
- Binary numbers are followed by the suffix "$_b$", for example: 00_b.
- Decimal numbers appear without suffixes.

A.4 Glossary of Abbreviations

Table 31. Standard Abbreviations

Abbreviation	Description
AIS	Alarm Indication Signal
API	Application Programmers' Interface
ATM	Asynchronous Transfer Mode
BEDC	Block Error Detection Code
BG	Background
BIP	Bit Interleave Parity
BIPV	Bit Interleave Parity Violation
BLER	Block Error Result
CAC	Connection Admission Control
CC	Continuity Check
CDV	Cell Delay Variation
CDVT	Cell Delay Variation Time
CLP	Cell Loss Priority
CRC	Cyclic Redundancy Check
FM	Fault Management
GCRA	Generic Cell Rate Algorithm
LB	Loopback
LOC	Loss Of Continuity
MBS	Maximum Burst Size
MCSN	Monitoring Cell Sequence Number
MPHY	Multi-PHY
MSB	Most Significant Byte
NNI	Network Node Interface
OAM	Operations, Administration, and Maintenance
PCR	Peak Cell Rate
PHY	Physical
PM	Performance Monitoring
PQFP	Plastic Quad Flat Pack
PTI	Payload Type Indicator

Table 31. Standard Abbreviations (Continued)

Abbreviation	Description
RDI	Remote Defect Indicator
SCR	Sustainable Cell Rate
SECB	Severely Errored Control Block
SPHY	Single PHY
SRAM	Static Random Access Memory
SSRAM	Synchronous Static Random Access Memory
TAT	Theoretical Arrival Time
TRCC	Total Received Cell Count
TS	Time Stamp
TUC	Total User Cells
TUCD	Total User Cell Difference
UPC	Usage Parameter Control
VPC	Virtual Path Connection
VPI	Virtual Path Identifier

APPENDIX B REFERENCES

- ATM Forum, *Traffic Management*, V4.0, draft, December, 1995.
- ATM Forum, *User-Network Interface (UNI) Specification*, V3.1, September, 1994.
- ATM Forum, *UTOPIA – An ATM - PHY Interface Specification*, Level 1, V2.01, March 1994.
- ATM Forum, *UTOPIA – An ATM - PHY Interface Specification*, Level 2, V1.0, June 1995.
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- ITU-T I.610, draft, November, 1994.

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