Z86015

PCMCIA INTERFACE WITH DMA SUPPORT

FEATURES	BENEFITS
■ 256 Bytes of Internal Attribute Memory	Sufficient Memory Space for TUPLES in Most Applications
■ Supports External Attribute Memory	For Peripherals that Require Greater than the Internal 256 Bytes of Attribute Memory
■ Five Configuration Registers	Confirming to PCMCIA Standards
■ EXCA Register Compatible	Platform Independent, Plug and Play
■ EEPROM Sequencer Circuitry for Automatic Loading of Internal Registers and TUPLE from a Local EEPROM, Master Mode	No Need for an External MCU, Lower Cost
■ Three Additional Registers to Support Remote EEPROM Programming	On-the-fly Programming of the EEPROM through the HOST Interface
■ Serial Peripheral Interface (SPI) Circuitry	Allows Control Through the Local Microprocessor, no Need for an EEPROM
■ Three Programmable Memory or I/O Map Ranges	Responds to Three DOS Specified Maps
■ Two Independent DMA Channel. DMA Operation can be Controlled from the Serial Interface or the PCMCIA Host Interface	Internal DMA Support Eliminates the Need for an External GLUE Logic in LAN or Multimedia Type of Applications
■ Supports On-Chip Local Peripheral Interface Bus (LPI) Arbitration	Permits Multiple Bus Masters on the Peripheral Bus
■ Supports up to 64 Kbytes FIFO Emulation Function	Lower CPU Overhead When Interfacing with Real-Time Peripherals
■ Supports Remote DMA Operation with Popular Ethernet Bus Master Devices	Faster and More Efficient Operation, Lower CPU Overhead
■ Supports 8 Bits or 16 Bits Operation	Allows Easy Implementation of Multi-Functions PCMCIA Cards, such as LAN and MODEM Card
■ Operates from a 3V to 5V Power Supply	Same IC may be used for Existing and Future Cards
■ Low Power Dissipation: 25 mW at 5V 250 µW in Power-Down Mode	Longer Battery Life. Critical in Battery Operating Systems
■ 100-Pin Low Profile VQFP Package	Smaller Footprint and Height
■ Advance 0.8 Micron CMOS Technology	Allowing a More Cost Effective Solution

GENERAL DESCRIPTION

The Z86015 is a general-purpose PCMCIA adapter chip used on the peripheral side, providing interface and control logic. Z86015 easily configures to all types of memory and I/O mapped PCMCIA card sockets. Mapping is performed from the I/O and Memory mapped PCMCIA to a Local Peripheral Interface bus that supports such devices as Ethernet controllers, UARTs, Modems, multimedia, wireless LAN, and other peripheral devices without the use of external hardware. Multimedia LAN/Ethernet solutions are illustrated in Figures 2, 3, and 4.

The Z86015 is stand-alone configurable without the use of a local processor by providing all of the attribute memory, CCRs, range, interrupt types through a serial EEPROM. The serial EEPROM is read automatically using an internal EEPROM sequencer. The Z86015 can also be configured through a local processor in a more intelligent fashion for use on intelligent controller systems. In addition to the local serial EEPROM and remote microprocessor programming methods, the Z86015 can be programmed with an external parallel (8-bit wide) EEPROM.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

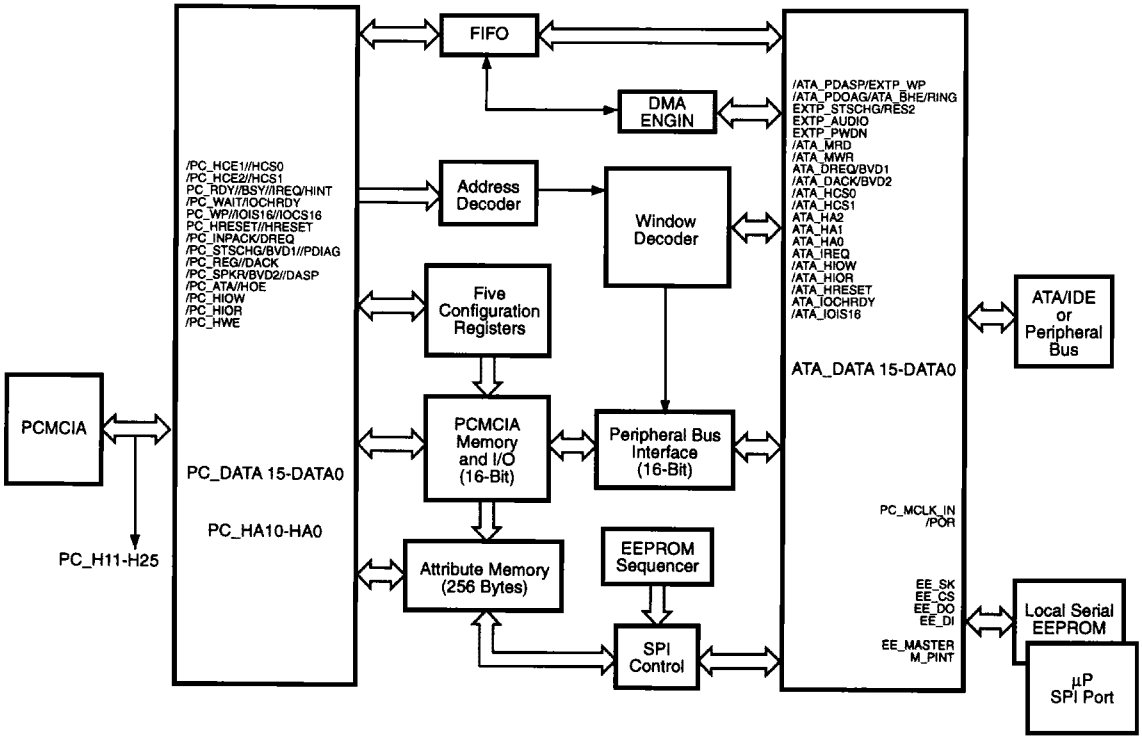

Figure 1. Z86015 Block Diagram

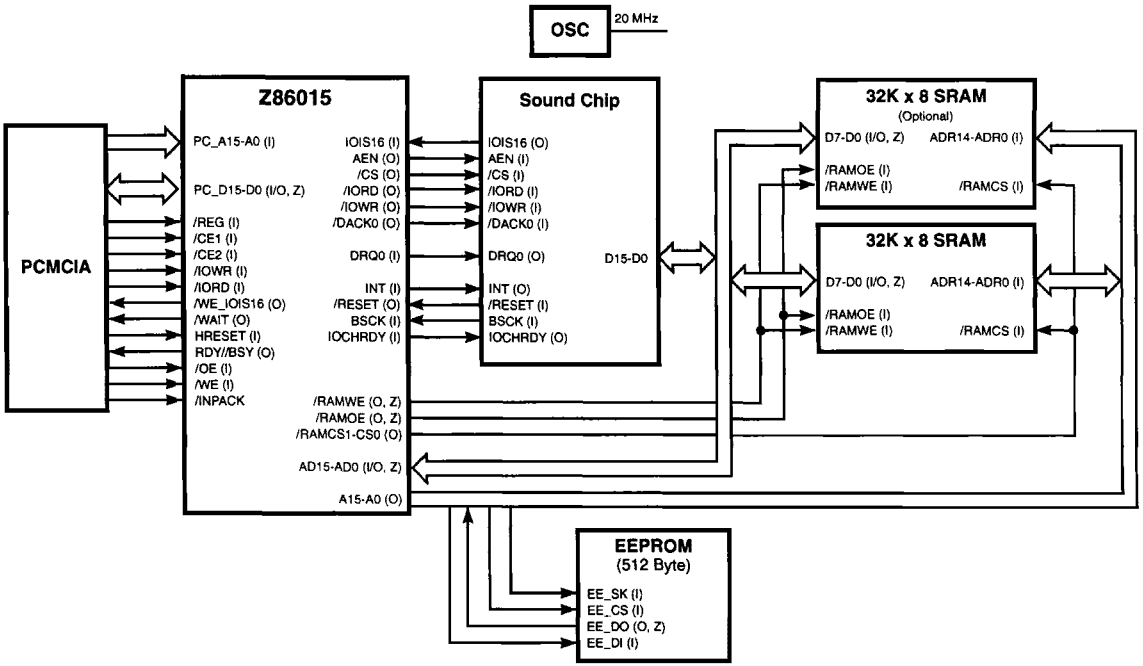

Figure 2. Z86015 Multimedia Application

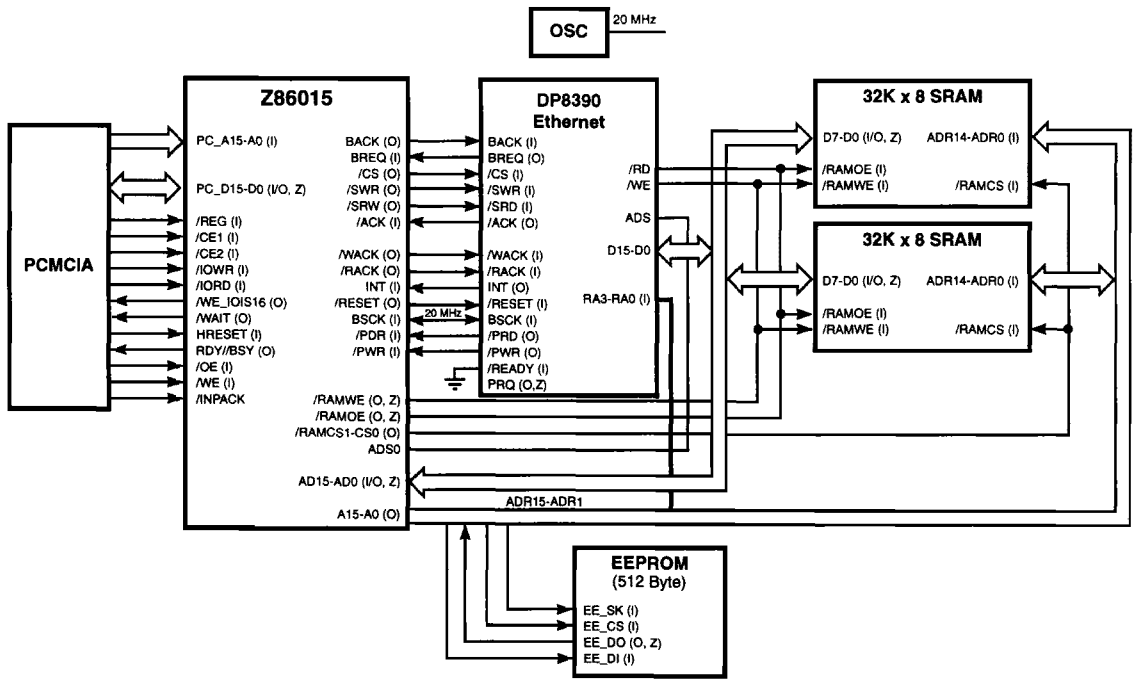

Figure 3. Z86015 LAN/Ethernet Adapter Solution No.1

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GENERAL DESCRIPTION (Continued)

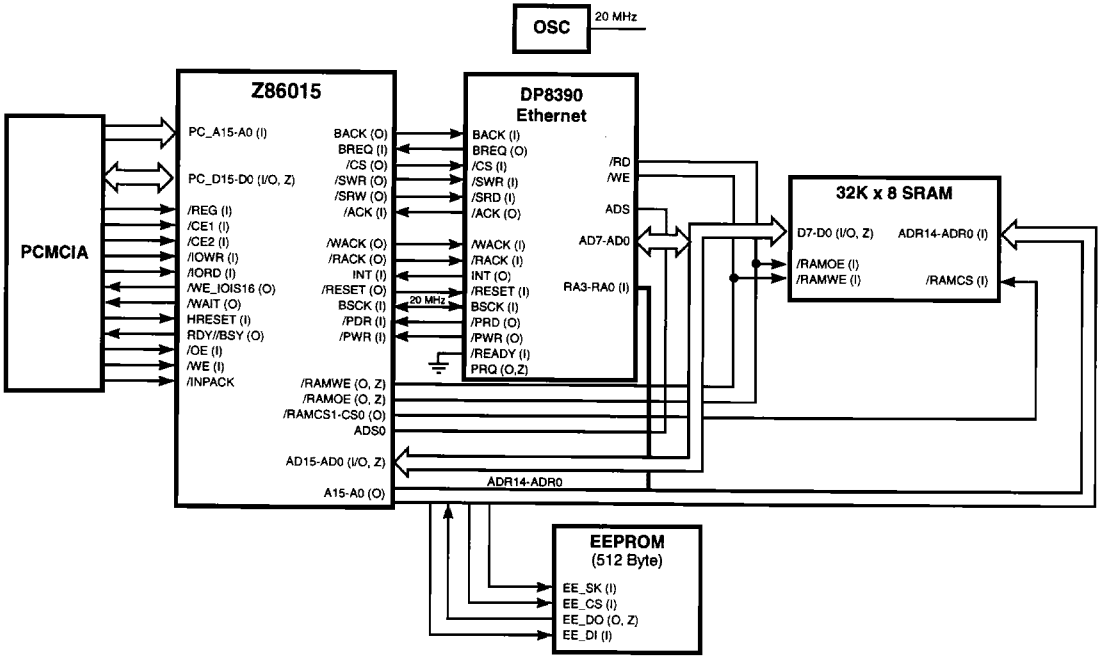

Figure 4. Z86015 LAN/Ethernet Adapter Solution No.1

PIN DESCRIPTION

Table 1. Z86015 Pin Description

Item	Pin Name	Pin Function
1	'PC_HCE1*	PCMCIA, Card Enable 1, active low input
2	'PC_HCE2*	PCMCIA, Card Enable 2, active low input
3	'PC_HA15/ STSCHG*	PCMCIA, Address bit 15, input Alternate pin definition: Status change output pin. Active low
4	'PC_HA14/ EXTP_STSCHG'	'PCMCIA, Address bit 14, input Alternate pin definition: External input: status change in
5	'PC_HA13/ PC_SPKR'	'PCMCIA, Address bit 13, input Alternate pin definition: PCMCIA Speaker output
6	'PC_HA12/ EXTP_AUDIO'	'PCMCIA, Address bit 12, input Alternate pin definition: Audio input pin
7	'PC_HA11'	'PCMCIA, Address bit 11, input
8	'PC_HA10'	'PCMCIA, Address bit 10, input
9	'PC_HA9'	'PCMCIA, Address bit 9, input
10	'PC_HA8'	'PCMCIA, Address bit 8, input
11	'PC_HA7'	'PCMCIA, Address bit 7, input
12	'PC_HA6'	'PCMCIA, Address bit 6, input
13	'PC_HA5'	'PCMCIA, Address bit 5, input
14	'PC_HA4'	'PCMCIA, Address bit 4, input
15	'PC_HA3'	'PCMCIA, Address bit 3, input
16	'PC_HA2'	'PCMCIA, Address bit 2, input
17	'PC_HA1'	'PCMCIA, Address bit 1, input
18	'PC_HA0'	'PCMCIA, Address bit 0, input
19	'PC_RDY/BSY/IREQ*	PCMCIA(memory mode), Ready(high)/Busy(low), (I/O mode) this is the active low interrupt request signal. Output
20	'PC_WAIT*'	PCMCIA, WAIT requested (low), output
21	'PC_WP/IOIS16*	PCMCIA(memory mode), write protected output (high), (I/O mode) this is the I/O is 16 bits wide active low output
22	'PC_HIOR*'	'PCMCIA, I/O read strobe, active low input
23	'PC_HIOW*'	'PCMCIA, I/O write strobe, active low input

PIN DESCRIPTIONS (Continued)

Table 1. Z86015 Pin Description (Continued)

Item	Pin Name	Pin Function
24	'PC_REG*	PCMCIA, REG active low input
25	'PC_INPACK*	PCMCIA, input acknowledge output, active low
26	'PC_HRESET'	'PCMCIA, Reset input, active high
27	'PC_HWE*'	'PCMCIA, memory write strobe input, active low
28	'PC_HOE*'	'PCMCIA, memory output enable input, active low
29	'PC_DATA0'	'PCMCIA Data bus bit 0, input/output
30	'PC_DATA1'	'PCMCIA Data bus bit 1, input/output
31	'PC_DATA2'	'PCMCIA Data bus bit 2, input/output
32	'PC_DATA3'	'PCMCIA Data bus bit 3, input/output
33	'PC_DATA4'	'PCMCIA Data bus bit 4, input/output
34	'PC_DATA5'	'PCMCIA Data bus bit 5, input/output
35	'PC_DATA6'	'PCMCIA Data bus bit 6, input/output
36	'PC_DATA7'	'PCMCIA Data bus bit 7, input/output
37	'PC_DATA8'	'PCMCIA Data bus bit 8, input/output
38	'PC_DATA9'	'PCMCIA Data bus bit 9, input/output
39	'PC_DATA10'	'PCMCIA Data bus bit 10, input/output
40	'PC_DATA11'	'PCMCIA Data bus bit 11, input/output
41	'PC_DATA12'	'PCMCIA Data bus bit 12, input/output
42	'PC_DATA13'	'PCMCIA Data bus bit 13, input/output
43	'PC_DATA14'	'PCMCIA Data bus bit 14, input/output
44	'PC_DATA15'	'PCMCIA Data bus bit 15, input/output
45	'LPI_HCS0'	'Local Peripheral Interface, Chip select 0 output. This signal can be programmed low or high active
46	'LPI_HCS1A'	'Local Peripheral Interface, Chip select 1A output. This signal can be programmed low or high active and also can be programmed to be active on even byte transfers if an odd/even word peripheral bus is used
47	'LPI_HCS1B'	'Local Peripheral Interface, Chip select 1B output. This signal can be programmed low or high active and also can be programmed to be active on odd byte transfers if an odd/even word peripheral bus is used
48	'LPI_IREQ'	Local Peripheral Interface, interrupt request input
49	'LPI_HIOR*'	'Local Peripheral Interface, I/O read strobe, active low output
50	'LPI_HIOW*'	'Local Peripheral Interface, I/O write strobe, active low output

Table 1. Z86015 Pin Description (Continued)

Item	Pin Name	Pin Function
51	'LPI_HRESET'	'Local Peripheral Interface, Reset output
52	'LPI_AD0/ LPI_DATA0'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 0 Alternate pin definition: Local peripheral data bus bit 0
53	'LPI_AD1/ LPI_DATA1'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 1 Alternate pin definition: Local peripheral data bus bit 1
54	'LPI_AD2/ LPI_DATA2'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 2 Alternate pin definition: Local peripheral data bus bit 2
55	'LPI_AD3/ LPI_DATA3'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 3 Alternate pin definition: Local peripheral data bus bit 3
56	'LPI_AD4/ LPI_DATA4'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 4 Alternate pin definition: Local peripheral data bus bit 4
57	'LPI_AD5/ LPI_DATA5'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 5 Alternate pin definition: Local peripheral data bus bit 5
58	'LPI_AD6/ LPI_DATA6'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 6 Alternate pin definition: Local peripheral data bus bit 6
59	'LPI_AD7/ LPI_DATA7'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 7 Alternate pin definition: Local peripheral data bus bit 7
60	'LPI_AD8/ LPI_DATA8'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 8 Alternate pin definition: Local peripheral data bus bit 8
61	'LPI_AD9/ LPI_DATA9'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 9 Alternate pin definition: Local peripheral data bus bit 9

PIN DESCRIPTION (Continued)

Table 1. Z86015 Pin Description (Continued)

Item	Pin Name	Pin Function
62	'LPI_AD10/ LPI_DATA10'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 10 Alternate pin definition: Local peripheral data bus bit 10
63	'LPI_AD11/ LPI_DATA11'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 11 Alternate pin definition: Local peripheral data bus bit 11
64	'LPI_AD12/ LPI_DATA12'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 12 Alternate pin definition: Local peripheral data bus bit 12
65	'LPI_AD13/ LPI_DATA13'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 13 Alternate pin definition: Local peripheral data bus bit 13
66	'LPI_AD14/ LPI_DATA14'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 14 Alternate pin definition: Local peripheral data bus bit 14
67	'LPI_AD15/ LPI_DATA15'	'Local Peripheral Interface, multiplexed address/data bus I/O bit 15 Alternate pin definition: Local peripheral data bus bit 15
68	'LPI_MRD*'	'Local Peripheral Interface, memory read strobe, active low output
69	'LPI_MWR*'	'Local Peripheral Interface, memory write strobe, active low output
70	'LPI_IOCHRDY'	'Local Peripheral Interface, I/O channel ready input. Programmable active high or active low
71	EE_CS	Serial interface chip select, active high. IN master mode, this is an output pin, in slave mode, this is an input pin
72	'BSCK'	'Master bus clock input

Table 1. Z86015 Pin Description (Continued)

Item	Pin Name	Pin Function
73	'WACK*/ DRQ0'	'Write acknowledge output This signal is used to indicate that the PCMCIA host system has written data in the internal holding latches during remote DMA transfers Alternate pin definition: DMA channel 0, data request 0. Active high input used to request a data transfer from the Z86015's DMA controller
74	'RACK*/ DACK0*'	'Read acknowledge output This signal is used to indicate that the PCMCIA host system has read data from the internal holding latches during remote DMA transfers Alternate pin definition:
		DMA channel 0, data Acknowledge 0. Active low output used to acknowledge that a data transfer with the 86015's DMA controller and the peripheral device
75	'PRD*/ DRQ1'	'Port read input Used to enable data from the internal latch to the local bus during a memory write cycle to local memory and remote DMA operation Alternate pin definition: DMA channel 1, data request 1. Active high input used to request a data transfer from the 86015's DMA controller
76	'PWR*/ DACK1*'	'Port write input Used to enable data from the internal latch to the local bus during a memory write cycle to local memory and remote DMA operation Alternate pin definition: DMA channel 1, data Acknowledge 1. Active low output used to acknowledge that a data transfer with the Z86015's DMA controller and the peripheral device.
77	ADS/AEN	Address strobe, programmable active high or low output, or an input when the Z86015 is not mastering the local data bus. This signal is used to latch the address on the multiplexed address/data peripheral bus. Alternate pin definition: Address enable. Used to indicate when a DMA transfer is in progress. AEN is set high or low (Programmable)
78	'LPI_LADR15/ M_PINT'	'Local peripheral interface, latched address output bit 15 Alternate pin definition: Local processor interrupt
79	'LPI_LADR14/ EE_SK'	'Local peripheral interface, latched address output bit 14 Alternate pin definition: Serial clock output connect to Serial EEPROM clock input, or remote programming serial clock input

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PIN DESCRIPTION (Continued)

Table 1. Z86015 Pin Description (Continued)

Item	Pin Name	Pin Function
80	'LPI_LADR13/ EE_DO'	'Local peripheral interface, latched address output bit 13 Alternate pin definition: Serial data output connected to serial EEPROM data input or remote programming device input
81	'LPI_LADR12/ EE_DI'	'Local peripheral interface, latched address output bit 12 Alternate pin definition: Serial data input connected to EEPROM data output or remote programming device output
82	'LPI_LADR11/ EE_MASTER'	'Local peripheral interface, latched address output bit 11 Alternate pin definition: After power on reset, the local peripheral address bus is not driven and this bit is sampled as: Pulled up: Serial bus is master. The Z86015 will initiate all writing to a local serial EEPROM
83	'LPI_LADR10/ EXT_PROM*'	'Local peripheral interface, latched address output bit 10 Alternate pin definition: On power on reset, this pin is sampled to determine the method of reading the attribute memory. If the line is tied low during power on, the Z86015 will fetch all internal programming information from an external prom, and all attribute memory fetches will be done in the external parallel (8-bit) prom. The prom size can be up to 64 Kbytes deep
84	'LPI_LADR9/ RING_IN'	'Local peripheral interface, latched address output bit 9 Alternate pin definition: Ring indicate input
85	'LPI_LADR8/ RES1'	'Local peripheral interface, latched address output bit 8 Alternate pin definition: Reserved Modem Event 1
86	'LPI_LADR7/ RES2'	'Local peripheral interface, latched address output bit 7 Alternate pin definition: Reserved modem Event 2
87	'LPI_LADR6/ PACKET_IN'	'Local peripheral interface, latched address output bit 6 Alternate pin definition: Packet indicate input

PIN DESCRIPTION (Continued)

Table 1. Z86015 Pin Description (Continued)

Item	Pin Name	Pin Function
88	'LPI_LADR5'	'Local peripheral interface, latched address output bit 5
89	'LPI_LADR4'	'Local peripheral interface, latched address output bit 4
90	'LPI_LADR3'	'Local peripheral interface, latched address output bit 3
91	'LPI_LADR2'	'Local peripheral interface, latched address output bit 2
92	'LPI_LADR1'	'Local peripheral interface, latched address output bit 1
93	'LPI_LADR0'	'Local peripheral interface, latched address output bit 0
94	'BACK/ EXTP_PWDN'	'Bus Acknowledge Output signal granting peripheral master device on the peripheral bus permission to acquire the bus
95	'BREQ/ EXTP_IOIS16*'	'Bus request Input signal from the peripheral master device requesting the local peripheral bus
96	V_{DD}	Power pin
97	V_{DD}	Power pin
98	V_{SS}	Ground pin
99	V_{SS}	Ground pin
100	V_{SS}	Ground pin

****Note:** actual pin out of this device is to be defined

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