T-49-19-16

GEC PLESSEY

SEMICONDUCTORS

S10103ADS Issue 2.3 October 1990

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

2

Features

- Radiation hard
- 3 MIP DAIS throughput @ 22 MHz clock
- MIL-STD-1750 A or B operation
- Silicon-on-sapphire technology
- High performance architecture
- 64kWord address space; expandable to 1 MWord (1750A) or 8 MWord (1750B) with optional MMU
- Single chip CPU

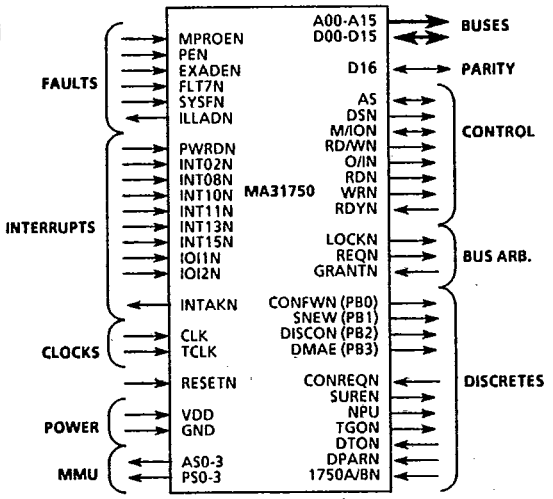


Figure 1: Pin definition; 1750A (1750B) mode

General Description

The Marconi MA31750 is a single-chip microprocessor that implements the full MIL-STD-1750A Instruction Set Architecture or option 2 of Draft MIL-STD-1750B. The processor executes all mandatory instructions and many optional features are also included. Interrupts, fault handling, memory expansion, Console, timers A and B, and their related optional instructions are also supported in full accordance with MIL-STD-1750.

The MA31750 offers a considerable performance increase over the existing MAS281. This is achieved by using a 32-bit internal bus structure with a 24 x 24 bit multiplier and 32-bit ALU. Other performance-enhancing features include a 32-bit shift network and a dedicated address calculation unit.

The MA31750 has on-chip parity generation and checking, to enhance system integrity.

A comprehensive built-in self-test has also been incorporated, allowing the processor functionality to be verified at any time.

Console communication is supported through a parallel interface using command/data registers in I/O space. A number of discrete output signals are produced to minimise external logic.

Three pins are provided to allow inclusion of the MA31750 into a multiprocessor or DMA system.

The processor can directly access 64kWords of memory in full accordance with MIL-STD-1750A This increases to 1MWords when used with the optional MA31751 memory management unit (MMU) 1750B mode allows the system to be expanded to 8MWord with the MMU.

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

GEC PLESSEY

SEMICONDUCTORS

1 Architecture

The Marconi MA31750 Microprocessor is a high performance implementation of the MIL-STD-1750A (Notice 1) instruction set architecture. Figure 2 depicts the architectural details of the chip. Two key features of this architecture which contribute to the overall high performance of the MA31750, are a 32-bit shift network and a 24-bit parallel multiplier. These subsystems allow the MA31750 to perform multi-bit shifts, multiplications, divisions and normalisations in a fraction of the clock cycles required on machines not having such resources. This is especially true of floating-point operations, in which the MA31750 excels. Such operations constitute 16% of the Digital Avionics Instruction Set (DAIS) mix and a generally much higher percentage of many signal processing algorithms, therefore having a significant impact on system performance.

1.1 Operating modes

The MA31750 may be operated in one of two basic user selectable modes. 1750A mode follows the requirements of MIL-STD-1750A (Notice 1) and implements all of the mandatory features of this standard. In addition, many of the optional features such as interval timers A and B, a watchdog timer and parity checking are included. 1750B mode, when selected, allows the user access to a range of new instructions and features as described in the Draft MIL-STD-1750B, Option 2. These include a range of unsigned arithmetic operations and expanded addressing support instructions.

In accordance with MIL-STD-1750A, the MA31750 can access a 64K-word address space. With the addition of an external Marconi MA31751 chip configured as a Memory Management Unit (MMU), this address space may be expanded to 1MWord (1750A mode) or 8MWord (1750B mode). The MA31751 data sheet gives further information on the MMU/BPU chip. Note that although a partial implementation of MIL-STD-1750B with only 512 page registers is permitted, expanding the system to give the full compliment of page registers (8192) specified by 1750B would require several MMU chips.

For those applications not requiring adherence to the address space requirements of MIL-STD-1750 the MMU may optionally be configured with up to one megaword each of instruction and operand space (1750A) or 8MWord each (1750B).

The basic MMU function allows write or execute protection to be applied on 4kWord block boundaries. This may be further resolved to 1kWord blocks by the inclusion of a Block Protect Unit (BPU). The MA31751 can act as both an MMU and a BPU in 1750A mode, operating with the full compliment of 1MWord of memory. It will also support expansion to 8MWord in accordance with Draft MIL-STD-1750B.

In addition to implementing all of the required features of MIL-STD-1750A and the Draft standard MIL-STD-1750B, the MA31750 also incorporates a number of optional features. Interval timers A and B as well as a trigger-go counter are provided. Most specified XIO commands are decoded directly on the chip and an additional set of commands, associated with MMU and BPU operations, are decoded on chip. All commands not directly decoded by the processor are output for decoding by external logic in accordance with the XIO and VIO protocols of MIL-STD-1750A and B.

The MA31750 offers a number of extra lines to allow its use in a system utilising multiple processors. A bus request and grant system coupled with external arbitration logic allows common data and address buses to be used between devices. A lock request pin is also provided to allow the processor to maintain control of the buses when accessing areas of shared memory and executing read-modify-write instructions.

1.2 Internal Features

Key features include: (1) a three-bus (R, S, and Y) data path consisting of an arithmetic/logic unit (ALU), three-port register file, shift network, parallel multiplier and flags block; (2) instruction fetch registers C0,C1, IA, and IB; (3) operand transfer registers A, DI, and DO; (4) a state sequencer; and (5) microinstruction decode logic. A brief description of these features follows:

1.2.1 Arithmetic/Logic Unit (ALU)

A full function 32-bit ALU performs arithmetic and logic operations on one or two 32-bit operands in a single machine cycle. The ALU supports 8-bit (exponent), 16-bit (word), 24-bit (mantissa) and 32-bit (double) data in two's complement form. The ALU performs all necessary shifting and sign-extensions to allow results to be calculated and placed correctly.

GEC PLESSEY

SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

1.2.2 Three Port Register File

A 28-word by 16-bit wide register file is used to store operands, addresses, base pointers, stack pointers, indexes, and temporary values. Registers R0 through R15 are general purpose and user accessible in accordance with MIL-STD-1750A; remaining registers are accessible by microcode and are not directly accessible to the user. Wrap-around concatenation of R0 through R15 allows 32- and 48-bit operands to be stored. Each register file port is 32-bits wide and the three-port architecture allows two operands to be read and a third operand to be written within one microcycle.

1.2.3 Parallel Multiplier/Accumulator

This multiplies a 24-bit multiplicand by a 24-bit multiplier in a single machine cycle. Only one iteration through the multiplier is required to complete a 16-bit by 16-bit multiply. During floating point multiply operations, the ALU generates the exponent whilst the mantissa product is being formed by the multiplier. This allows a floating point multiply operation to be accomplished in only one machine cycle.

1.2.4 Shift Network

This shifter is a 32-bit shift network, allowing multibit shifts to be accomplished in a single machine cycle. It is used by the microcode for all shift, rotate, and normalise operations.

1.2.5 Quotient Shift Network

A separate 32-bit shift register, which can be serial/parallel loaded and unloaded, is attached to the ALU. Its function is to supply quotient bits to the ALU during divide operations. The result of the divide is returned bit by bit to the Qshift block to be assembled.

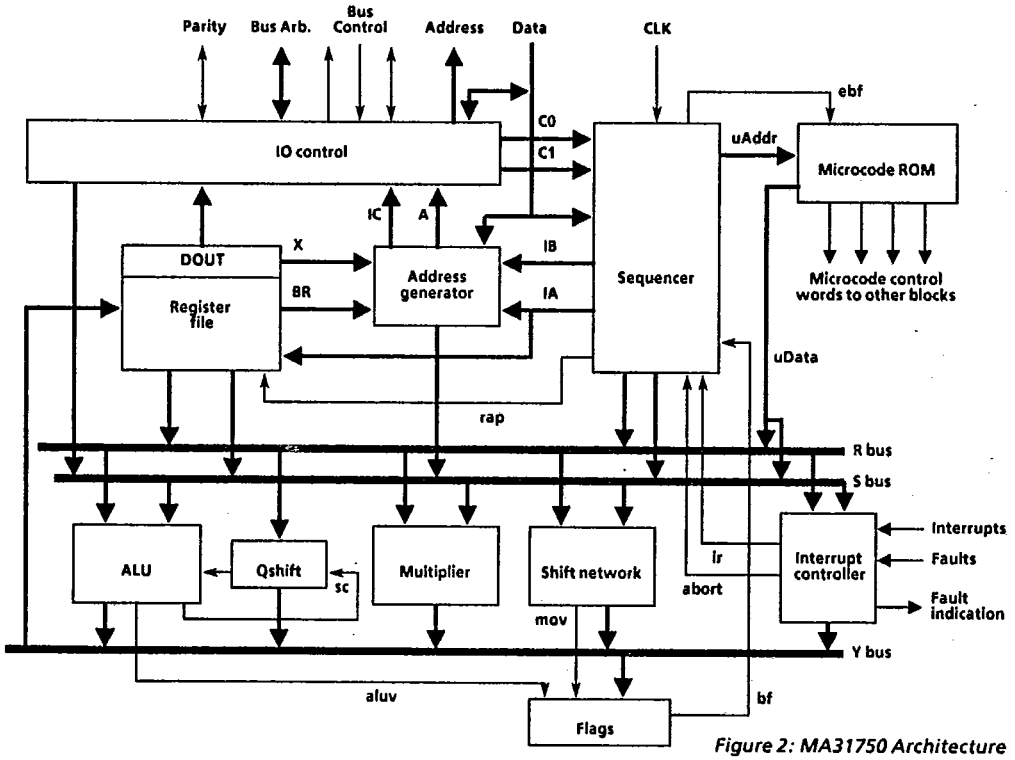


Figure 2: MA31750 Architecture

MA31750

High Performance MIL-STD-1750 Microprocessor (Advance data)

GEC PLESSEY

SEMICONDUCTORS

1.2.6 Flags Block

This block holds the condition status (CS) bits C, P, Z, and N (part of the system status word); the internal microcode flags (not user-accessable) and the flag decode logic. The flags are derived from the value on the Y-bus at the end of each cycle. The type of microcode operation being performed determines the position of the result on the bus.

1.2.7 Sequencer Block

A state machine, clocked by the system oscillator, generates processor timing and control signals. These signals constitute the lowest level of control available within the module, and provide the framework for basic operations such as selecting the next microinstruction to be executed or performing an operation within the ALU. Each complete pass through the state machine corresponds to one such operation and constitutes a machine cycle.

The microsequencer controls the execution of each MIL-STD-1750A or macro instruction by stepping through its corresponding microcode sequence. If the macroinstruction is a conditional, the CS bits of the status word will be interrogated to determine the necessary course of action. At the completion of each macroinstruction, the microsequencer checks to see if a Hold request or an interrupt is pending. If so, the microsequencer will branch to the appropriate microinstruction sequence. If not, the microsequencer begins sequencing the next macroinstruction.

Note that the microsequencer is under its own control. Each processor machine cycle corresponds to the execution of a single microinstruction.

All internal cycles and external cycles when running with no wait states are two system clocks (CLK) long. Any external cycle may be lengthened by adding an integral number of wait states which will extend the basic cycle by one clock period per wait state added.

1.2.8 Instruction Pipeline

There are four, 16-bit pipeline registers: IA and IB are in the sequencer block and hold the instruction currently executing (and its postword, if any); C0 and C1 are in the IO block and hold the next instruction (and postword).

During the execution of any MIL-STD-1750A or B instruction, instruction fetches are performed to replace the number of words in the current instruction.
In this way, at the end of the current instruction the pipeline already contains the next instruction. The sequencer decodes the next instruction before its execution, allowing the first microcode word in the instruction sequence to be made available right at the start of the instruction.

1.2.9 Microcode ROM Block

This is a 1.25k- (1280) word by 64-bits/word ROM which stores the microinstructions that implement the MIL-STD-1750A and B instruction sets. In addition to the microinstruction sequences corresponding to the MIL-STD-1750A/B instructions, the microcode ROM also stores sequences for performing initialisation, interrupt response, bus hold response, instruction prefetch and built-in-test (BIT). The address of the next microinstruction to be accessed is generated by the microsequencer. The accessed microinstruction is latched at the very start of each microcycle (machine cycle) and broadcasted to the rest of the processor.

1.2.10 IO Block

The IO block handles the sequencing of the bus control signals to effect a memory or IO transfer. It also manages the bus arbitration signals and the external ready interface. The Data In (DI), and Data Out (DO) registers serve to buffer transfers between the data path and the system address and data busses. These registers are used under microcode control and are not directly accessible by software. A description of the use of these registers during memory and I/O operations is provided in section 3.0.

1.2.11 Address Generator Block

The address generator block holds the two system address registers: IC - the instruction to be fetched next; A - the address of any operands associated with the current instruction. The block contains its own 16-bit ALU which allows address calculations such as (base + index) to be performed independently of the main ALU.

GEC PLESSEY
SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor
(Advance data)

1.3 Interrupt Block
The interrupt block incorporates a pending interrupt register, a mask register, a priority encoder, a fault register, a status word, two interval timers (A and B), a trigger-go counter, XIO command decode logic, and microcode control logic. A brief description of these features follows.

1.3.1 Pending Interrupt Register (PI)
This 16-bit register is used to capture and hold interrupts until they can be processed by software, using a logic 1 to represent a pending interrupt. The PI supports three dedicated external, six user-definable external, and seven dedicated internal interrupts. Level-sensitive interrupts are captured at the beginning of each machine cycle, whilst edge sensitive interrupts are captured immediately.

1.3.2 Mask Register (MK)
This 16-bit register is used to store the interrupt mask. Interrupts are masked by ANDing each mask bit with its corresponding PI register bit. Interrupts which are masked will be captured in the PI register but will not be acted on until unmasked. Interrupt level 0 can not be masked. A logic 0 in a given bit position indicates that the corresponding bit in the PI register will be masked.

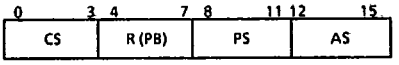
1.3.3 Priority Encoder
This encoder generates an interrupt request to the CU whenever one or more unmasked interrupts are pending and enabled in the PI and encodes the highest priority unmasked pending interrupt as a 4-bit vector. This vector is read during interrupt servicing in order to create the interrupt Linkage and Service pointers.

1.3.4 Fault Register
This 16-bit register is used to capture and hold both internal and user implemented external faults using positive logic, i.e., a logic "1" represents a fault. Bus cycle faults are captured at the end of each machine cycle whilst the two general purpose faults SYSFN and FLT7N are edge-triggered. Setting any one or more faults in FT will cause a level 1 (machine error) interrupt request. Once a fault is set in FT, it may only be cleared via an XIO command.

In 1750B mode, a fault mask register is provided to allow selective masking of fault conditions. Section 5 (Software Considerations) contains further information.

1.3.5 Timers A and B
These are two 16-bit software controllable timers. Timer A is clocked by the TCLK input while Timer B is clocked by the internally generated TCLK/10. Timers A and B will generate interrupt levels 7 and 9, respectively, when their maximum counts are reached. In 1750B mode, each timer has a reset register to give greater control over the count period. Section 5 (Software Considerations) contains further information.

1.3.6 Status Word
Figure 3 depicts the status register format. This 16-bit word is divided into four, 4-bit sections. Three of these sections [AS, PS and, (1750B mode) PB] are control bits for implementing expanded memory with an external MMU. The fourth section, CS, is held within the flags block. The AS field is used during expanded memory access to define the page register set to be used for instruction and operand memory references. The PS field is used during memory protect operations to define the access key used for memory accesses. The PS field is also used during execution of privileged instructions. PS must be zero for such operations to be legal. The PB field is used in conjunction with the AS field in 1750B mode to expand the number of page registers available. Note that attempting to set AS or PB to a non-zero value with no MMU, or setting PB to a non-zero value in 1750A mode is illegal. This will be aborted and a fault II will be generated (SW will remain unchanged).



Field	Bits	Description
CS		CONDITION STATUS:
	0	C- Carry from an addition or no borrow from a subtraction
	1	P- Result >0
	2	Z- Result = 0
	3	N- Result <0
R	4 - 7	RESERVED (= 0) in 1750A mode PAGE BANK SELECT in 1750B mode
PS	8 - 11	PROCESSOR STATE: (a)- Memory access key code (b)- Privileged instruction enable
AS	12 - 15	ADDRESS STATE: Page register sets for expanded memory addressing

Figure 3: Status Word Format

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

GEC PLESSEY
SEMICONDUCTORS

1.3.7 Trigger-Go Counter

This 16-bit counter is clocked by the TCLK input, is enabled during system initialisation, and may be preset under software control to give a wide range of timeout intervals.

The timer is stopped upon overflow or by presetting to zero. Overflow is signalled by a low level on the TGON discrete output, which remains low until the counter is reset by software. This counter is typically used as a system "watchdog" timer. Note that the action of the timer is independent of the main CPU and will continue to run (and produce TGON) even if CLK is disabled.

1.3.8 XIO Command Decode Logic

This logic decodes all internally supported XIO commands and generates the control signals necessary to carry out the commanded action. In addition, the validity of a command not implemented internally is verified. Figure 22c in Section 6 identifies the XIO commands which are internally supported by the MA31750.

2 Pin Descriptions

A description of each pin function follows. The function name is presented first, followed by its acronym and description. Function type is either input, output, high impedance (Hi-Z), or a combination thereof. Full timing characteristics of each of the functions are shown in section 7.

All signals - with the exception of power, ground and clock signals are TTL compatible, and are provided with Electrostatic Discharge (ESD) protection circuitry. Throughout this data sheet, active low signals are denoted either by placing a bar over the signal name, or by following the signal name with an "N" suffix, e.g., DSN. If a signal has a dual function, both function names will be used separated by a "/". The function name to the left of the "/" will be active high while the function to the right will be active low, again with an "N" suffix, e.g., RD/WN.

Pin Name	Pin N°	Function	Description
POWER			
VDD		Power supply	DC power supply input
GND		Ground	0V reference point.
CLOCK SIGNALS			
CLK		System clock	Input clock signal
TCLK		Timer clock	This clock input is used by the internal 16-bit timers A and B, and by the Trigger-Go counter. MIL-STD-1750 requires this signal to have a frequency of 100kHz.
SYSTEM BUSES			
A00-A15		System address bus	An active-high address bus which is tri-state during bus cycles not assigned to this CPU. A00 is the most significant bit.
D00-D16		System data bus	An active-high data bus which is tri-state during bus cycles not assigned to this CPU. D00 is the most significant bit, D16 is the parity check bit.
EXTERNAL REQUESTS			
RESETN		System reset	This active-low input should be asserted low to reset the processor. The low to high transition will start the initialisation sequence which will perform a Built-In-Test and will initialise the processor in accordance with MIL-STD-1750.

Figure 4. Pin Descriptions

T-49-19-16

GEC PLESSEY
SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

Pin Name	Pin No	Function	Description
BUS CONTROL			
AS		Address strobe	This active-high bidirectional signal establishes the beginning and end of each bus cycle. The trailing edge (high-low transition) is used to sample bus cycle-related faults into the fault register The leading edge guarantees that a valid address is on the address bus. The line is an input during cycles not assigned to this CPU.
DSN		Data strobe	This active-low signal indicates the presence of data on the system data bus During a processor read cycle, DS goes low to indicate that the processor is no longer driving the bus. This signal is tristate in bus cycles not assigned to this CPU
M/ION		Memory/IO select	This bidirectional signal indicates whether the current bus cycle is accessing memory (high) or IO (low) addressing space. This signal becomes valid shortly after the start of a machine cycle and remains valid throughout The signal is an input during cycles not assigned to this CPU.
RD/WN		Read/write select	This signal indicates the direction of data transfer on the system data bus Data is read in by the processor when high, and written out when low This signal becomes valid shortly after the start of a machine cycle and remains valid throughout. RD/WN is tristate during cycles not assigned to this CPU
O/IN		Operand/instruction select	This signal indicates whether the current bus cycle is accessing operand (high) or instruction (low) addressing space. This signal becomes valid shortly after the start of a machine cycle and remains valid throughout. O/IN is tristate during cycles not assigned to this CPU
RDN		Read strobe	This active-low output is asserted low with DSN during read cycles. The rising edge of this signal indicates the time at which the processor reads the data bus This signal is tristate in bus cycles not assigned to this CPU.
WRN		Write strobe	This active-low output signal is asserted low with DSN during write cycles. The rising edge should be sed by the system to latch data from the data bus This signal is tristate in bus cycles not assigned to this CPU
RDYN		Ready	This input signal allows the basic machine cycle of the processor to be extended to accomodate slower peripheral or memory devices. Ready may be pulled high to add an integral number of CLK cycles (wait states) to the machine cycle The line must be pulled low to allow processing to proceed. RDYN has no effect on cycles dedicated to internal operations [Note: If RDYN is held high during two consecutive TCLK high-to-low transitions (with DSN low), a bus timeout fault will occur and will be indicated in the appropriate bit in the fault register. The occurrence of this fault will cause the state sequencer to terminate the current machine cycle and begin a new machine cycle. Also, the presently executing macroinstruction will be aborted and execution will branch, unless masked, to the machine error interrupt (level 1) software routine. The DTON signal may be used to override this feature.]
BUS ARBITRATION			
LOCKN		Bus lock	This active-low output signal allows the system busses to be locked to one processor for successive cycles The CPU will lock the bus during read-modify-write instructions such as DECM and TSB. During non-locked cycles, this signal remains high.
REQN		Bus request	This active-low output signal is driven low when the CPU requires the bus in the next cycle. An external arbiter should sample this signal at the third clock edge in a machine cycle. The signal becomes invalid when the CPU has started that cycle
GRANTN		Bus grant	This active-low signal is produced by an external bus arbiter to indicate that the CPU currently has the highest priority bus request. If the bus is not locked, the CPU may begin a bus cycle commencing with the next CPU clock cycle. If the CPU is currently locking the bus then GRANTN is ignored.

Figure 4 (continued). Pin Descriptions

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

GEC PLESSEY
SEMICONDUCTORS

Pin Name	Pin No	Function	Description
INTERRUPTS			
PWRD		Power down interrupt	A low on this active low input will be captured in the PI register and sets pending interrupt 0. This is the highest priority interrupt and cannot be masked or disabled.
INT02N INT08N INT10N INT11N INT13N INT15N		User interrupt levels 2, 8, 10, 11, 13 and 15	A low on any of these active low inputs will be captured in the PI register and will set pending interrupt levels 2, 8, 10, 11, 13, and 15, respectively. Level 2 is the highest priority user level while level 15 is the lowest priority. These interrupts are maskable and can be disabled. If edge sensitivity has been selected, interrupts will be captured on the falling edge of the interrupt input, otherwise the interrupt will be latched by the falling edge of AS. [NOTE: Interrupt levels 1, 3, 4, 5, 6, 7, and 9 are dedicated to internal machine interrupts] Unused inputs should be pulled up to VDD.
IOI1N IOI2N		I/O dedicated interrupts levels 1 and 2	A low on either IOI1N or IOI2N will be captured in the PI register and will set pending interrupt levels 12 and 14, respectively. These inputs are level sensitive only and are captured by the falling edge of AS Unused inputs should be pulled up to VDD
INTAKN		Interrupt acknowledge	This active-low output indicates the start of an interrupt service When low, the processor outputs the linkage pointer (LP) address to the system The INTAKN signal may be used to remove level-sensitive interrupt inputs: the current interrupt priority can be ascertained by reading the address bus
FAULTS			
MPROEN		Memory protect error	A low placed on this active-low input, sampled on falling AS, indicates that an access fault, execute protect or write protect fault has been detected. Bit 0 of the fault register is set if this signal is applied during a memory cycle; bit 1 is set if the line goes low during an IO cycle. Either condition sets pending interrupt level 1 and, in the case of a memory cycle error, aborts the current 1750 instruction. Although the MA31750 aborts the macroinstruction, system memory management, and/or block protect hardware is responsible for preventing the erroneous bus cycle from accessing memory To effectively use this feature, MPROEN should be pulled low prior to the start of the next machine cycle. This can be accomplished by injecting wait states to hold off the new cycle until the system protection circuitry can decide whether or not to allow the transaction.
PEN		Parity error	A low on this active-low input, sampled on falling AS, informs the CPU that an external parity error has occurred. Bit 2(memory), 3(I/O) or 4(DMA) of the fault register is set, depending upon the type of transfer taking place. This asserts a level 1 pending interrupt,
EXADEN		External address error	A low on this active-low input, sampled on falling AS, informs the CPU that an external address error has occurred. Bit 8 of the fault register is set if this signal goes low during a memory cycle; bit 5 is set if the signal goes low during an IO cycle Either error condition asserts a level 1 pending interrupt and causes an abort of the current 1750 instruction.
FLT7N		General purpose fault input	A low at any time on this active-low input sets bit 7 of the fault register, causing a pending interupt level 1 This fault is user-definable
SYSFN		System fault input	A low at any time on this active-low input sets bits 13 and 15 of the fault register, causing a pending interupt level 1 This fault is user-definable.
ERROR INDICATION			
ILLADN		Illegal address	This active-low output drops low if the EXADEN input drops low or if the bus fault timeout circuitry causes an interface timeout

Figure 4 (continued). Pin Descriptions

GEC PLESSEY

SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

Pin Name	Pin N°	Function	Description
MMU CONTROL			
AS0-AS3		Address state bus	This active-high bus indicates the current address state of the CPU. The value on this bus is copied from the status register within the CPU. These lines are tristate during bus cycles not assigned to this CPU.
PS0-PS3		Processor state bus	This active-high bus indicates the current process state of the CPU. The value on this bus is copied from the status register within the CPU. These lines are tristate during bus cycles not assigned to this CPU.
PB0-PB3		Page bank select bus	This active-high bus indicates the current CPU page bank when operating in 17508, 8 MWord addressing mode. The value on this bus is copied from the status register within the CPU. These lines are tristate during bus cycles not assigned to this CPU. When operating in 1750A mode, these lines have the alternative functions CONFWN (PB0), SNEW (PB1), DISCON (PB2) and DMAE (PB3)
DISCRETES			
CONFWN		Configuration word read	This active-low output signal is driven low when the processor reads the external configuration register. The line may be used as an output enable for this register. The configuration register is read during initialization to determine the system configuration. (Note: In 1750B mode this pin is reassigned to PB0. To derive this signal in B mode, the user must decode the IO read from locaton 8410)
SNEW		Start new cycle	This active-high output will be asserted high during the first cycle of each new MIL-STD-1750 instruction sequence. This signal may be used for test purposes. (Note: In 1750B mode this output is reassigned to PB1)
DISCON		Discrete output select	This active-low output will be asserted low by the processor during an XIO DO command. It may be used as the enable signal for an external discrete output register. (Note: In 1750B mode this output is reassigned to PB2).
DMAE		DMA enable	This active-high output indicates that an external DMA device is enabled. It is disabled (low) following a reset and is toggled under program control using XIO commands DMAE and DMAD (Note: In 1750B mode this output is reassigned to PB3)
CONREQN		Console request	This active-low input initiates and controls console operation following the end of a 1750 instruction. Commands and data are passed to the processor in this mode via three dedicated registers in IO space. Pending interrupts always take precedence over console operation.
SUREN		Start-up ROM enable	This active-low output indicates that start-up ROM is enabled. The signal is asserted low following initialisation or by XIO ESUR. The signal remains asserted until removed with XIO DSUR. When a start-up ROM is present on the system, this signal should be used to qualify its chip select or output enable such that the ROM may be accessed only when SUREN is low. [NOTE: Instruction pipelining must be considered in transitioning from Start-Up ROM to RAM. See Section 5 on Software Considerations]
NPU		Normal power-up	This output is driven high to indicate that the Built-In Test (BIT) sequence, performed on reset or power-up, has completed successfully. This output drops low when an external reset is applied. It may also be reset by software using the XIO RNS command

Figure 4 (continued). Pin Descriptions

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

GEC PLESSEY

SEMICONDUCTORS

Pin Name	Pin No	Function	Description

DISCRETES (Continued)

TGON		Trigger-go output	This active-low output drops low whenever the trigger-go counter overflows (rolls over to 0000). It returns to the high state when the counter is reset by software (using XIO GO command).
DTON		Disable timeout	A low on this input will reset and disable the bus fault timeout circuitry.
DPARN		Disable parity	A low on this input will reset and disable the on-chip parity verification. Note that parity generation on write data is not disabled by this pin.
1750A/BN		1750A/1750B mode select	This input line allows the operating mode of the processor (1750A/1750B) to be selected. When high, the processor will be placed in 1750A mode. When low, the processor assumes 1750B mode. This line allows the new 1750B instructions to be trapped as illegal in 1750A mode, and switches the function of the dual-purpose control lines PB0-PB3.

Figure 4 (continued). Pin Descriptions

GEC PLESSEY
SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

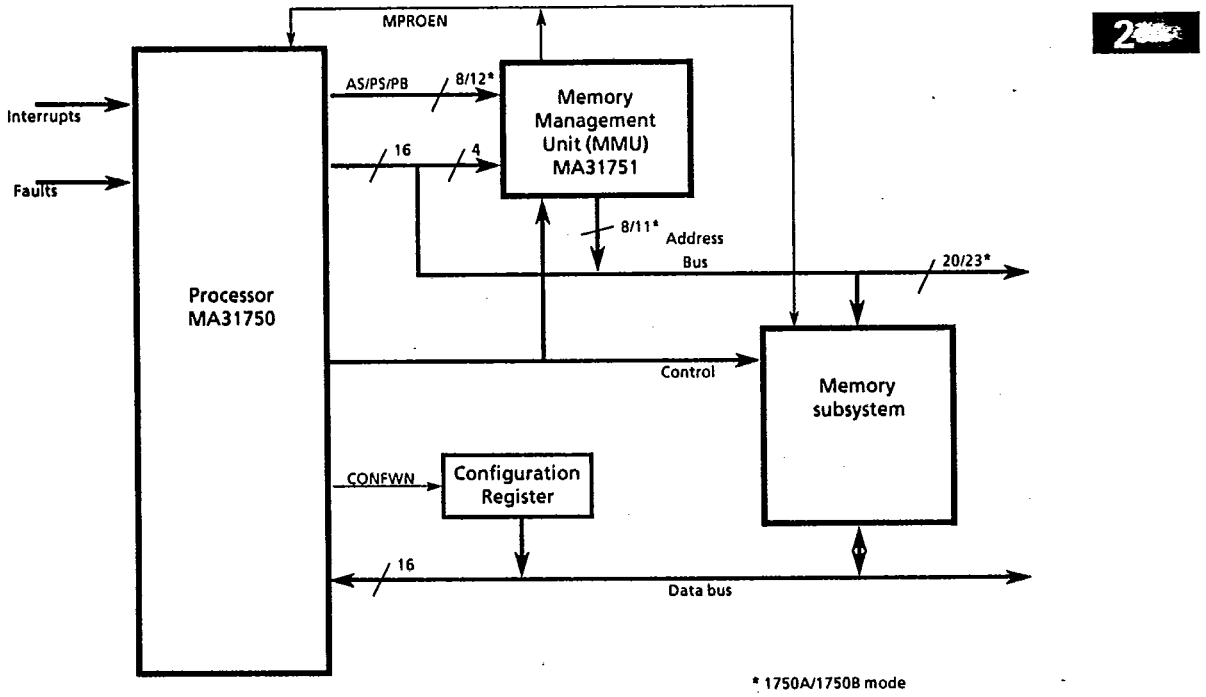


Figure 5: Typical MA31750/MA31751 System Interface

MA31750

High Performance MIL-STD-1750 Microprocessor
(Advance data)

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Configuration Register

The system configuration register allows the MA31750 to function with a variety of different system designs. Implemented features such as an BPU should be indicated as present by setting a bit in an externally-implemented, 16-bit latch in IO space defined by the table of XIO commands, figure 22c.

The configuration register is read by the processor during Initialisation. Alternatively, the register may be read from software by executing an XIO RCW command. The processor decodes this command internally and produces a discrete output signal CONFWN which may be used as the register Output Enable control. Alternatively the user may decode the IO command RCW to derive CONFWN (this must be done in 1750B mode since CONFWN is not available).

The bit position corresponding to each feature or optional device is shown in figure 6 below. Note that bits 8 through to 15 are unused by the processor. These may be used as discrete input lines by the user if required.

Although it is possible to change the system configuration in operation, this is not recommended. For example, if the interrupt level/edge trigger select bit (bit 4) is changed during normal operation of the device, one or more spurious interrupts may occur. It is strongly recommended that the user reset the processor following a change in the system configuration.

When in 1750B mode, the processor needs to know how many Page Banks are implemented in the external system so that Status Word changes can be protected properly. MIL-STD-1750B allows the options 0,1,2,4,8 or 16. The actual selection should be coded into the three configuration register bits MMU0, MMU1 and MMU2 as shown in figure 7 below.

Note that in 1750A mode, setting any of the MMU select bits indicates the presence of an MMU, the actual code is unimportant in this mode.

Bit No.	Function
0	MMU select 0
1	1 = BPU in system
2	1 = Console operation
3	MMU select 1
4	Interrupts (1 = Level, 0 = edge)
5	MMU select 2
6	Parity, 1 = odd, 0 = even
7	BIT on power-up, 1 = yes, 0 = no
8-15	Not used (may be used as discrete inputs)

Figure 6: Configuration Register Bit Assignment

Selected bit			Function
MMU2	MMU1	MMU0	
0	0	0	No MMU in system
0	0	1	1 Page Bank (PB0)
0	1	0	2 Page Banks (PB0-1)
0	1	1	4 Page Banks (PB0-3)
1	0	0	8 Page Banks (PB0-7)
1	0	1	16 Page Banks (PB0-15)
1	1	X	16 Page Banks (PB0-15)

Figure 7: MMU Select Bit Assignments

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MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

3 Operating Modes

MA31750 operating modes include: (1) initialisation, (2) instruction execution, (3) interrupt servicing, (4) fault servicing, (5) Console support and (6) timer operations.

3.1 Initialisation

The module executes a microcoded initialisation routine in response to a hardware reset. This routine clears module registers, disables and masks interrupts, reads the configuration register, resets the output discrete register (if implemented), initialises the MMU and BPU (if implemented), performs Built-In-Test (BIT), raises the Start-Up ROM enable discrete, clears and starts timers A and B, resets the trigger-go counter, and loads the instruction pipeline. Figure 8 summarises the resulting initialisation state.

BIT consists of ten subroutines, as outlined in figure 9, and begins by pulling NPU low. This is the first time after reset that NPU is guaranteed low. If all ten subroutines execute successfully, NPU is raised high. If any part of BIT fails, a corresponding bit identifying the failed subroutine is set in General Register R0, Fault Bit 13 is set in the Fault register (FT) and NPU is left in the low state. Figure 9 defines the coding of BIT results in R0. In the event of such a failure, the resulting module reset state will be dependent on where in BIT the error occurred and may not be the same as that shown in figure 8. A BIT failure indication in FT will set the level 1 interrupt request bit of the Pending Interrupt (PI) register. Since initialisation disables and masks interrupts, this interrupt request will not be asserted. Any external interrupts or faults occuring during BIT will be ignored and cleared before program execution begins.

The last action performed by the initialisation routine is to load the instruction pipeline. Instruction fetches start at memory location zero with AS = 0, PS = 0 and PB = 0 and will be from the Start-Up ROM if implemented. Whether BIT passes or not, the processor will begin instruction execution at this point. The system start-up code may include a routine to enable and unmask interrupts in order to detect and respond to a BIT failure if required.

MA31750	
Instruction Counter	Zero
Status Word	Zero
Fault Register	Zero
Fault Mask Register (1750B)	All ones
Pending Interrupt Register	Zero
Interrupt Mask Register	Zero
General Registers	Indeterminate
Interrupts	Disabled
Timers A and B	Zeroed and started
Timer Reset Registers (1750B)	Zero
Start Up ROM	Enabled
DMA Enable	Disabled
Triger Go Counter and TGON line	Reset and started
MMU	
Page Registers	Bank 0, Group 0, PS = 0
Page Register AL/W/E Fields	Zero
Page Register PPA Field	Logical to physical
BPU	
Memory Protect RAM	Disabled, zero
Global Memory Protect	Enabled

Figure 8: Initialisation State

3.2 Instruction Execution

Once initialisation has been completed, the module will begin instruction execution. Instruction execution is characterised by a variety of operations, each one or more machine cycles in duration. Depending on the instruction being executed at the time, these operations include: (1) internal CPU cycles, (2) instruction fetches, (3) operand transfers, and (4) input/output transfers. Instruction execution may be interrupted at the end of any individual machine cycle by an interrupt or console request.

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

GEC PLESSEY
SEMICONDUCTORS

3.2.1 Internal CPU Cycles

Internal CPU cycles are used to perform all CPU data manipulation operations. Internal CPU cycles are two clock periods in duration and are characterised by AS low, DSN high and M/ION high. Tables 22a and 22b in Section 6 provide machine cycle counts associated with each MIL-STD-1750A instruction.

3.2.2 Instruction Fetches

Instruction Fetches are used to keep the instruction pipeline full. This ensures that the next instruction is always ready for execution when the preceding instruction is completed. During jump and branch instruction execution the pipeline is flushed and refilled with two consecutive instruction fetches starting at the new instruction location. The pipeline is also refilled as part of interrupt request processing.

Instruction fetches are characterised by OP/IN low but are otherwise identical to an operand read transfer. For a detailed explanation of the function of various bus control signals during instruction fetches, refer to the discussion of operand transfers below. Section 6.5 provides timing characteristics for instruction fetches. Machine cycles associated with instruction fetches are a minimum of two oscillator periods in duration. The RDYN signal may be used to insert wait states to accommodate slow memory. Machine cycle counts included in figure 22a of Section 6.5 include instruction fetches.

Instruction fetches use instruction pipeline registers IA, IB, C0, C1, the instruction counter (IC) and the data input register (DI). Action is as follows. The contents of IC are placed on the A bus. The returned value, which will be an instruction, is stored in the IB or C0 register depending upon whether the current instruction is one or two words long. If the current instruction is two words long, the value in IC is incremented (via its dedicated counter) and the next fetch is performed. This second returned value, which may be either an instruction or an immediate operand, is stored in either C0 or C1 (again dependent upon the length of the current instruction).

At the end of the currently executing macroinstruction, the complete pipeline is advanced by either one or two places, thus bringing the new prefetched macroinstruction into IA and its associated post-word (if any) into IB. Since the opcode section of the new instruction (most significant 8 bits) has been prefetched the decoding of the instruction may be performed during the last cycle of the preceeding instruction, allowing the microcoded control information relevant to the new instruction to be made available right from the start of that instruction.

3.2.3 Operand Transfers

Operand transfers are used to obtain (read in) operands to be used by an instruction and to save (write out) any results of an instruction's execution. Section 7 provides timing characteristics for operand transfers. Machine cycles associated with operand transfers are a minimum of two oscillator periods in duration. The RDYN signal may be used to insert wait states to accommodate slow memory. Machine cycle counts in figure 22a of Section 6.5 include operand transfers.

Operand transfers use the address register (A), the data input register (DI), and data output register (DO). Before the operand transfer begins, the processor calculates the effective operand address in the address generator and stores this value in A. For write transfers, the processor loads the operand into the DO register.

All operand transfers between the CPU and memory are referenced to the AS and DSN bus control signals and are characterised by O/IN high and by M/ION high. The transfer begins by placing the contents of A (the address register) onto the A bus immediately following the start of the machine cycle. The AS strobe then goes high to indicate the presence of a valid address and remains high until the end of the cycle.

GEC PLESSEY

SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

The RD/WN signal indicates the direction of the transfer. If the operation is a write, the operand in DO is placed onto the data bus, indicated by WRN low. DSN should be used to enable any data buffers present in the system. Data is guaranteed valid at the low-to-high transition of WRN. The memory system must pull RDYN low to conclude the transfer.

During operand read transfers, the data bus drivers are placed in a high impedance state before DSN is asserted low to give the memory system access to the bus. This transition can be used by the memory system to generate an output enable. The memory system must pull RDYN low to conclude the transfer. Data will be read into the DI register on the RDN rising edge.

3.2.4 Input/Output Transfers

Input/Output transfers utilize the MIL-STD-1750 XIO and VIO protocols and are characterized by M/ION low and O/IN high. RD/WN defines the direction of the transfer. AS, DSN and WRN cycle as with operand transfer operations. IO transfers may be divided into three groups; those commands which are implemented internally by the CPU; those commands which are implemented by external system hardware; and those commands defined as illegal by MIL-STD-1750A and B.

During the execution of an XIO command the processor will perform a test to determine the instruction group as defined above. If the instruction is implemented internally (e.g. Read Timer A) then the XIO data will be directed to or read from an internal register. If the instruction is implemented externally then data will be written to or read from the external system via the system data bus. In both of these cases the command appears on the system address bus but in the case of an internal transfer the data will be ignored (read) or invalid (write).

BIT	Test Coverage	Cycles
7	Temporary Registers (T0 - T11)	47
7	General Registers (R0 - R15)	79
8	Flags Block	18
9	Sequencer Operation and ROM checksum	5129
10	Divide routine Quotient Shift Network	12
11	Multiplier and ALU	13
12	Barrel shift Network	13
13	Interrupts and fault handling and detection	17
14	Address generator block	13
15	Instruction pipeline	15

Note: BIT pass is indicated by all zeros in FT bits 13, 14, and 15

Figure 9. Built-in Test Coverage and Timing

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

GEC PLESSEY

SEMICONDUCTORS

If a command is implemented internally, no RDYN pulse will be required to complete the cycle. A complete list of commands implemented internally by the MA31750 appears in figure 22c.

If an instruction is determined as illegal, or an EXADEN occurs during the execution of an optional external command then the instruction will be treated as a NOP but will set the appropriate bit in the system fault register (as defined in MIL-STD-1750A and B).

XIO is a priviledged instruction and, as such, may only be executed when the Status Word, PS field equals zero. Any attempt to violate this condition will be trapped by the command microsequence.

3.3 Interrupt Servicing

Nine user interrupt request inputs are provided for programmed response to asynchronous system events. A low on any of these inputs will be detected at the falling edge of AS and latched into the Pending Interrupt (PI) register on the following sync falling edge (where sync is an internal clock running at half the frequency of CLK. Stalling the CPU stops sync.) This sequence occurs whether interrupts are enabled or disabled or whether the specific interrupt is masked or unmasked.

All of the user interrupts INT02N-INT15N may be programmed to be either level or edge sensitive by setting or clearing the appropriate bit in the system configuration register (if implemented). If edge sensitivity is selected then an interrupt request input must transition to the high state before a subsequent request on that input will be detected. If level sensitivity is selected then holding an interrupt input low will cause a new interrupt to be latched following each service. Note that interrupts IOI1 and IOI2 are level sensitive only.

In order that the system may recognise when a service has been started, an interrupt acknowledge pin has been provided. At an early stage in the service of an interrupt, the processor will execute XIO command RLP and place a 4-bit code onto the data bus to indicate the service priority level. At the same time this command will be decoded internally to cause the INTAKN line to be asserted low. This signal may be used to release the latched interrupt line.

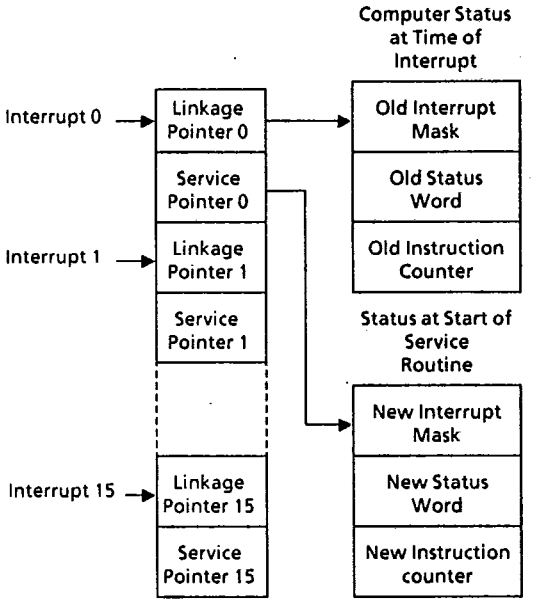

Figure 10. Interrupt Vectoring

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SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

When an interrupt request is latched into PI, it is ANDed with its corresponding mask bit in the mask register (MK). Interrupt level 0 is not maskable. Any unmasked pending interrupts are output to the priority encoder where the highest priority is encoded as a 4-bit vector. If interrupts are enabled, and an unmasked interrupt is pending, the priority encoder will assert an interrupt request to the sequencer.

Upon completing execution of a given MIL-STD-1750A or B instruction, the sequencer checks the state of the priority encoder's interrupt request. If an interrupt request is asserted, the sequencer branches to the microcode interrupt service routine. This routine performs a read of the priority encoder's 4-bit pending interrupt vector and then uses this value to calculate the appropriate interrupt linkage and service pointers. The pointers serve as addresses to data structures used in servicing interrupts. Figure 10 depicts this relationship. Figure 11 defines the pointer values.

Using the linkage and service pointers, the microcode interrupt service routine performs the following: (1) the current contents of the status word, mask register, and instruction counter are saved; (2) a write status word (WSW) I/O command is executed with an all zero data word; (3) the new mask is loaded into MK and interrupts are disabled; (4) the new status word is read and checked for a valid Address State (AS) field - If the address state is non-zero and an MMU is not present, the AS is set to zero and fault 11 (address state error) is set in the fault register FT; (5) a write status word command using the new status word is performed; and (6) the new IC value is loaded into IC, the instruction pipeline is flushed and refilled starting at the new address, and instruction execution begins.

[NOTE: The steps listed above represent a summary of actions performed during interrupt servicing and do not necessarily reflect the actual order in which these events take place.]

If an interrupt is latched during the interrupt service routine, it will not be processed until interrupts are re-enabled. If an AS fault occurs during the service routine, interrupt level 1 will be set. This interrupt will be serviced when interrupts are re-enabled unless it is masked by the new value in MK.

3.4 Fault Servicing

Five user fault inputs are provided. A low on any of the three bus-cycle-related fault inputs EXADE, MPROEN or

	Interrupt	LP Address	SP Address
PWRD	0	20	21
ME	1	22	23
INT02	2	24	25
FI.P o/f	3	26	27
Fx.P o/f	4	28	29
BEX	5	2A	2B
FI.P u/f	6	2C	2D
Timer A	7	2E	2F
INT08	8	30	31
Timer B	9	32	33
INT10	10	34	35
INT11	11	36	37
IOI1	12	38	39
INT13	13	3A	3B
IO12	14	3C	3D
INT15	15	3E	3F

Figure 11. Interrupt Pointer Definitions

MPE will be latched into the Fault Register (FT) on the next falling edge of AS. A low on either of the two general-purpose fault inputs FLT7N or SYSFN will set the appropriate fault bit immediately.

No falling edge detectors are provided to prevent repeat latching of faults held low beyond the first falling edge of AS. However, all FT bits are ORed together and input to the PI bit 1 through an edge detector to prevent the fault register from causing multiple level 1 interrupts.

The sequence of events following a fault capture depends on the type of fault as follows:

3.4.1 MPROEN, EXADEN, PEN and Bus Fault Time-Out

The capture of one or more of these faults sets pending interrupt level 1 (machine error) of the Pending Interrupt (PI) register on the falling edge of AS. Furthermore, the instruction currently executing is aborted at the AS high-to-low transition following the AS high-to-low transition that latched the fault. The IC value saved in the interrupt linkage table for the level 1 interrupt always points to the instruction which was in instruction pipeline register IA at the time of the abort. Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT.

MA31750

High Performance MIL-STD-1750 Microprocessor
(Advance data)

GEC PLESSEY
SEMICONDUCTORS

The microcoded interrupt service routine reads the interrupt priority vector from the Interrupt Unit and clears the serviced interrupt from the PI. However, the FT maintains the interrupting bit(s). Therefore, a level 1 interrupt would be latched again if there was no anti-repeat logic to prevent a never-ending loop of interrupts.

3.4.2 FLT7N and SYSFN
The capture of one or bothof these faults immediately sets pending interrupt level 1 (machine error) of the Pending Interrupt (PI) register. Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT.

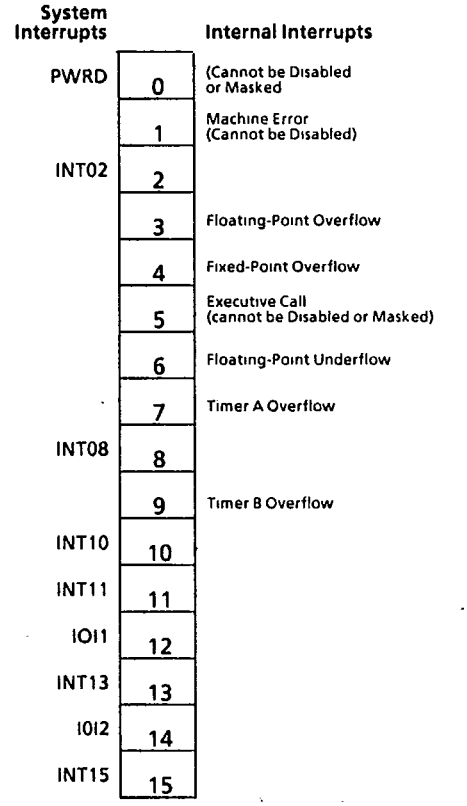

Figure 12. Pending Interrupt Register Bit Assignments

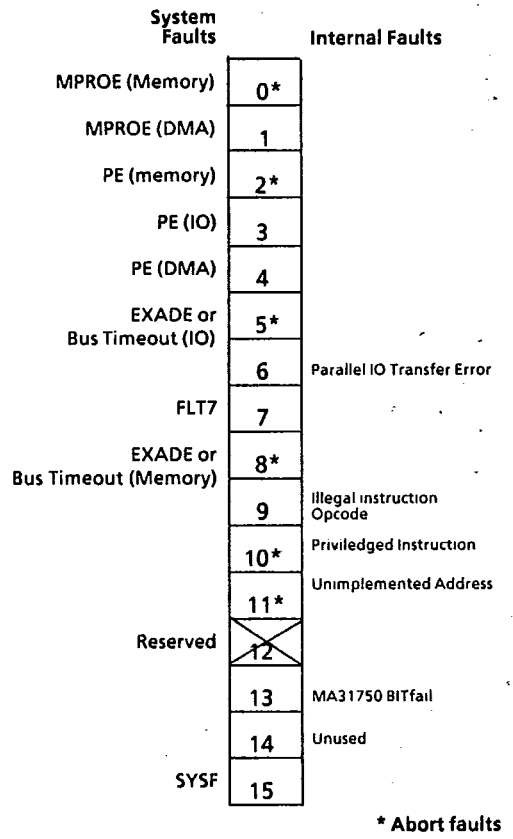

Figure 13. Fault Register Bit Assignments

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SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

Faults 0, 2, 5, 8, 10 and 11 cause the current instruction to be aborted. Although the current instruction will complete, any attempted writes to either the internal register file or to the sytem will be inhibited. The RDYN line will be ignored during these inhibited cycles.

During the machine cycles between fault capture and the beginning of the microcode interrupt handling routine, AS, DSN, RDN and WRN are forced to their inactive states. In the case of MPROEN, which may reflect an attempted write violation, it is required that system hardware provide the additional protection necessary to inhibit any memory write strobe.

Interrupts are serviced at the end of the currently executing instruction if not masked and if interrupts are enabled. System software servicing level 1 interrupts must clear the FT via the XIO RCFR command at some point in the routine to allow subsequent faults to latch a level 1 interrupt request. A non-destructive read of the FT is provided by the command XIO RFR, but this command should be used carefully.

3.4.3 Parity Generation and Checking

The MA31750 features on-chip parity generation and checking on all data bus transfers. Data generated by the processor has a parity bit attatched to it to allow external logic to verify write transfers. On read transfers, the processor will check the incoming parity (if enabled) and will generate the appropriate parity error fault if detected. Parity checking may be disabled when operating with devices which do not support parity generation by asserting the DPARN (Disable Parity) input low. The checking polarity (odd or even) is selectable with Configuration register bit 6.

2

3.5 Console Operations

The MA31750 will interface directly to an external console, allowing the operator to examine and change the contents of internal registers, memory and IO devices. All console transactions are conducted through one of three addresses in IO space:

Address	Function
8402_{16}	Console command input
$C000_{16}$	Data input
4000_{16}	Data output

Console mode may be entered in one of two ways:

1. By driving the CONREQN input low. This causes the processor to perform an IO read of the Console command (8402_{16}) following the completion of the current 1750 instruction and no pending interrupt. Valid console commands are shown in figure 15.

2. By executing the breakpoint (BPT) instruction. When the CPU encounters a BPT the internal copy of the system configuration register is read. If a console device is indicated then the MA31750 enters console mode and reads the command previously placed in 8402_{16}. If no console is present, BPT is treated as a NOP.

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

GEC PLESSEY
SEMICONDUCTORS

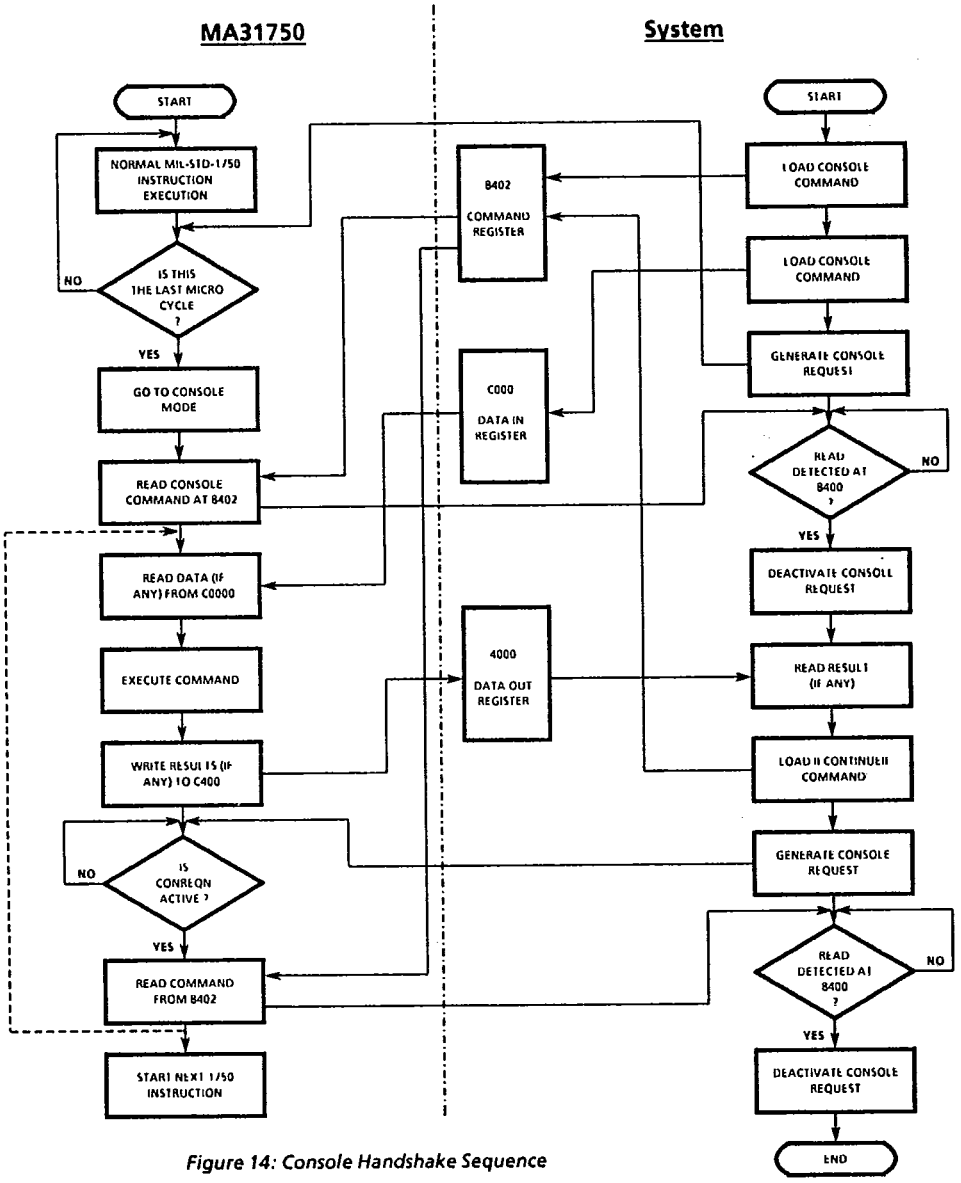

Figure 14: Console Handshake Sequence

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SEMICONDUCTORS

MA31750

T-49-19-16

High Performance MIL-STD-1750 Microprocessor

(Advance data)

CODE	FUNCTION
1	READ REGISTER
2	WRITE REGISTER
3	READ & CLEAR FAULT REGISTER
4	WRITE STATUS WORD
5	READ MEMORY
6	WRITE MEMORY
7	READ NEXT MEMORY
8	WRITE NEXT MEMORY
9	XIO
A	NEXT XIO
0	CONTINUE
B	DISABLE

REGISTER(S)	DESCRIPTION OF REGISTER(S)	HEX.
RN = R0-R15	GENERAL PURPOSE REGISTERS R0 TO R15	000-00F
TN = T0-T11	MICROCODE REGISTERS T0-T11	010-01B
A	OPERAND ADDRESS REGISTER	01C
IC	INSTRUCTION COUNTER	01D

Figure 15: Console Command and Register Definitions

MA31750

High Performance MIL-STD-1750 Microprocessor (Advance data)

GEC PLESSEY
SEMICONDUCTORS

3.5.1 Using BPT

Console mode may be entered by executing a BPT instruction with Console present indicated in the Configuration Word. On encountering a BPT instruction, the processor reads the Configuration Word to check for the presence of a Console. If a Console is indicated, the microsequencer branches to the microcode BPT Console service routine. This routine decrements IC once and enters the Console state.

To release the MA31750 from a BPT initiated Console state, the CONREQN input must be pulsed low following a continue command in accordance with the timing diagrams in Section 7. When CONREQN returns high, the Hold state will be released on the following AS high-to-low transition. Instruction execution resumes with the first instruction loaded into the pipeline.

3.5.2 Single-Stepping

Software can be single-stepped through the proper use of the CONREQN input and the BPT instruction. Use the BPT instruction to mark the beginning of the section of code which will be stepped through. Pulse CONREQN low to release the BPT initiated Hold state and then pull CONREQN low again during the two subsequent machine cycles that refill the instruction pipeline. When the first instruction following Hold release completes execution, the module will once again enter the Hold state. Again pulling CONREQN low will cause the next instruction to execute. This process may be repeated as long as required. Raising CONREQN high will resume normal operation.

3.6 Timer Operations

The MA31750 implements interval timers A and B, a trigger-go counter, and a bus fault timer. A discussion of each follows:

3.6.1 Timers A and B

Timer A is clocked by the TCLK input; timer B is clocked by an internally generated TCLK/10. The divider circuitry is reset when Timer B is reset to give deterministic processor operation. MIL-STD-1750A requires TCLK to be a 100-kHz pulse train. If allowed to overflow, timers A and B will set level 7 and level 9 interrupt requests, respectively. Timing characteristics of each timer are defined in Section 7. Each timer can be read, loaded, started and stopped by using XIO commands as identified in figure 15 of Section 3.5.

Each timer has associated with it a reset register from which the timer is automatically loaded following a software reset or overflow. These registers are initially loaded with zero but may be reloaded from software to provide greater control over the count period.

The MA31750 timers A and B will be disabled upon execution of a BPT software instruction when a Console is connected, as required by MIL-STD-1750A (Notice 1).

3.6.2 Trigger-Go Counter

The trigger-go counter is also clocked by the TCLK input. In order that the count period may be controlled, a reset register is provided. On reset, this register is loaded with the maximum count of $FFFF_{16}$ but can be reloaded under software control to take any value between 0 and $FFFF_{16}$ (a value of zero disables the timer and TGON). This allows the timeout period to be varied between 20us and 0.65s.

The counter is decremented on each machine cycle. Whenever the trigger-go counter overflows, TGON drops low and remains low until the counter is reloaded from the reset register via the GO internal XIO command. Timing characteristics for trigger-go counter operation are defined in Section 7.

3.6.3 Bus Fault Timer

All bus operations are monitored to ensure timely completion. A hardware timeout circuit is enabled at the start of each memory and I/O transfer (DSN high-to-low transition) and is reset upon receipt of the external ready (RDYN) signal. If this circuit fails to reset within a minimum of one TCLK period or a maximum of two TCLK periods, either bit 8 (if the transaction is with memory) or bit 5 (if the transaction is with I/O) of the Fault Register (FT) is set. This sets pending interrupt level 1 and causes the current bus cycle to be terminated by forcing DSN high. The MIL-STD-1750A instruction is aborted, and control passes to the level 1 interrupt service routine (if the level 1 interrupt is unmasked). The timeout mechanism is disabled and reset if DTON is asserted low.

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SEMICONDUCTORS

T-49-19-16

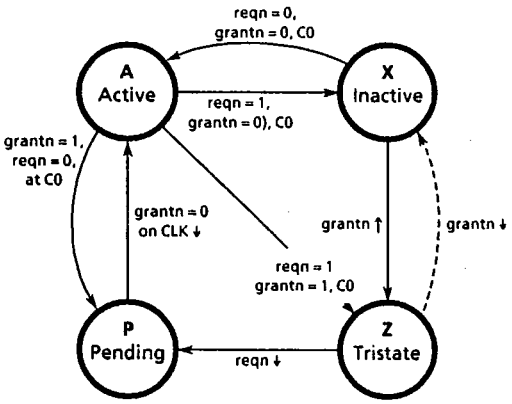
MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

2

Multiprocessor Support



C0 - Falling clock at end of cycle.

Figure 16: Processor Bus Arbitration State Diagram

4.1 Bus Arbitration

Once initialisation has been completed, the processor will begin instruction execution by executing a sequence of microinstructions each one machine cycle (two system clock periods) long. Each machine cycle may perform either an internal or an external operation; if the operation is purely internal then the system buses will not be in use and may be reassigned to another processor.

The MA31750 uses three signals to control the ownership of the system buses. The REQN (Bus Request) line drops low towards the end of a machine cycle to indicate that the CPU can make use of the busses on the next cycle. The GRANTN (Bus Grant) pin should be asserted by an external arbiter to signal to the processor that the buses are clear and available for use. This signal is polled by the CPU on each falling clock edge after REQN is asserted low; the CPU will wait in this pending (P) state until granted. When grant is recognised, the CPU begins to drive the system buses. REQN, however, is not asserted high until after AS rises, to prevent the bus being reassigned very early in the new cycle.

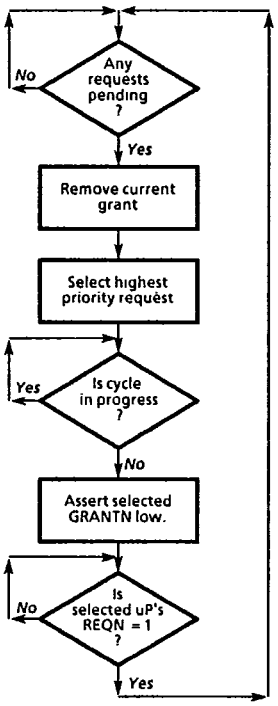


Figure 17: Possible Bus Arbitration Scheme

If the arbiter receives no further requests then GRANTN should be maintained low to prevent any delay from being introduced at the boundary between two consecutive transfers. The processor in this case will remain either in state A (during bus transfers) or state X (during internal cycles).

A third signal, LOCKN, signals that the CPU wishes to hold on to the bus prevent access by other processors during read-modify-write instructions. If a higher priority request is received, the arbiter must wait until the bus is inactive and unlocked before granting control to another processor. This is indicated by AS low and LOCKN high.

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

GEC PLESSEY
SEMICONDUCTORS

5 Software Considerations

5.1 Operating Modes

The MA31750 is capable of being operated in one of two basic modes, as previously mentioned. These are described in detail below:

5.1.1 1750A Mode

1750A mode is a full implementation of MIL-STD-1750A (Notice 1) and includes some of the optional features mentioned in this standard.

5.1.2 1750B Mode

1750B mode is an implementation of the proposed MIL-STD-1750B, Option 2, Draft of 17-July-1988. This mode extends the basic 1750A mode operation by allowing access to the larger address space and 'long' address-mode instructions of the 'B' standard. These instructions include the long load and store instructions and unsigned integer arithmetic. Note that the transcendental functions SIN, COS, LN etc. (Option 3 of MIL-STD-1750B) are not supported. Features new to MIL-STD-1750B which are in violation of MIL-STD-1750A are only enabled in 1750B mode. These include the new instructions, timer A and B reset registers, a Fault Mask register and the Page Bank select feature of the MMU.

There is a difference in the way in which 1750A and 1750B detect the overflow condition which may occur during floating point and extended floating point multiply and divide operations. In 1750A an overflow occurs if the sum (multiply) or difference (divide) of the exponents exceeds $7F_{16}$ or 80_{16} before the instruction is started. In 1750B the overflow is detected at the last point in the operation, i.e. after any normalization has taken place. The MA31750 takes the operating mode A or B into account when calculating the overflow in these cases, in order to comply with both specifications.

5.2 Using Start-Up ROM

The transition between code execution from Start-up ROM and system RAM must be made with care. If a system overlays RAM with the Start-Up ROM and the transition is made by simply executing XIO DSUR from the ROM, then the instruction pipeline will contain the value stored in the ROM location immediately following the XIO DSUR command. This value will be treated as an instruction and the module will attempt to execute it. In such cases, it is recommended that DSUR be followed by an unconditional branch instruction with offset, i.e., the BR instruction. An alternative approach is simply to jump to a portion of RAM not overlaid by the Start-Up ROM and execute DSUR from RAM.

5.3 Using Software Timers A and B

The MA31750 implements the two software timers A and B as defined int the MIL-STD 1750A specification. These are general purpose timers which are clocked at 100kHz and 10kHz respectively, giving clock 'tick' intervals of 10us and 100us respectively. They may be started using the XIO TAS and XIO TBS instructions, and stopped using XIO TAH and XIO TBH. If a timer is allowed to overflow ($FFFF_{16}$ - 0000_{16}) it will generate pending interrupt levels 7 (A) or 9 (B).

In 1750B mode, each timer has associated with it a reset register which may be loaded with any 16-bit value from software. If a timer is allowed to overflow, an automatic reset will take place which will reload the timer with the value held in its on-chip reset register, provided that the timer had previously been loaded using XIO OTA/OTB. If this is not the case then the timers will reset to zero on overflow. Each of the reset registers is initialised to zero but may be changed using XIO OTAR or XIO OTBR.

5.4 Fault Mask Register

A fault mask register is accessible in 1750B mode. Its function is similar to that of the Interrupt Mask register and allows selective enabling and disabling of all bits in the Fault Register. All faults are maskable. Setting a bit in this register allows the corresponding fault bit to be seen by the system. The register is loaded with all ones on initialisation.

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MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

6 Performance

6.1 Benchmarking

Figure 22 defines the number and type of machine cycles associated with each MIL-STD-1750A instruction. This information may be used when benchmarking MA31750 performance. The Digital Avionics Instruction Set (DAIS) mix, which defines a typical frequency of occurrence for MIL-STD-1750A instructions, is used here for this purpose.

One problem with the DAIS mix, however, is that it does not reflect the impact of data dependencies on system performance. For example, a multiplication in which the operand is zero may be performed much faster than one with two non-zero operands. Also, the DAIS mix does not specify such time consuming operations as normalization and alignment.

Realistic benchmarks must therefore take both the instruction mix and data dependencies into account. To this end, machine cycle counts in figure 22 which have data dependencies, are annotated with either an "a" or "wa" suffix.

An "a" suffix reflects an average number of machine cycles (where each of several possibilities is equally likely) and a "wa" suffix reflects a weighted average number of machine cycles (where some data possibilities are more likely than others).

Weighted averages are only applicable to floating-point operations. Weighted averages provided in figure 22 are based on the Sweeney (IBM) guidelines. These guidelines take a wide range of data dependencies into consideration. Normalization and alignment operations are also represented. Figure 18 shows MA31750 throughput, at various frequencies and wait states, for the DAIS mix using Sweeney data dependencies.

6.2 Expanded Memory Performance

The inclusion of an MMU (Memory Management Unit) will degrade the throughput performance of the processor in two ways. Firstly, each memory access will have an additional overhead associated with the formation of the extended address from the MMU. This may require that the system inserts wait states to lengthen each external cycle. Secondly, the MMU itself may require that some 'housekeeping' work be done by the processor, which will lengthen the program execution time.

No of waitstates	Frequency MHz			
	0	1	2	3
20	2.7	2.1	1.7	1.4
22	3.0	2.3	1.8	1.5
25	3.4	2.6	2.1	1.7

Figure 18. Throughput (MIPS) with waitstates.

There are no widely accepted benchmarks which may be used to measure the resultant decrease in throughput. The MA31751 MMU holds the references to the current instruction and operand pages in a fast translation-lookaside buffer which allows the extended address to be produced without having to add wait states, providing the current page has not been altered. If access to a different page is required then one wait state must be inserted into the first external cycle following the page register change. Note that if sequential code is being executed then one wait state will be inserted after each block of 4096 transfers (assuming no data waits).

6.3 Data Types

The MA31750 fully supports 16-bit fixed-point single-precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit extended precision floating-point data types. Figure 19 depicts the formats of these data types.

All numerical data is represented in two's complement form. Floating-point numbers are represented by a fractional two's complement mantissa with an 8-bit two's complement exponent. All floating-point operands are expected to be normalised. If not normalised, the results from an instruction are not defined.

6.4 Addressing Modes

The MA31750 supports the eight addressing modes specified in MIL-STD-1750A. These addressing modes are depicted in figure 21 and are defined below.

6.4.1 Register Direct (R)
The register specified by the instruction contains the required operand.

6.4.2 Memory direct (D,DX)
Memory Direct (without indexing) is an addressing mode in which the instruction contains the memory address of the required operand. In Memory Direct-Indexed (DX), the memory address of the required operand is specified by the sum of the contents of an index register (RX) and the instruction address field (A). Register R1 through R15 may be specified for indexing.

6.4.3 Memory Indirect (I, IX)
Memory Indirect (without indexing) is an addressing mode in which the memory address specified by the instruction contains the address of the required operand. In Memory Indirect with Pre-Indexing (IX), the sum of the contents of a specified index register and the instruction address field in the address that contains the address of the required operand. Registers R1 through R15 may be specified for pre-indexing.

6.4.4 Immediate Long (IM, IMX)
There are two formats which implement Immediate Long Addressing; one allows indexing and one does not. For the indexable form, if the specified index register, RX, is not equal to zero, the contents of RX are added to the immediate field to form the required operand; otherwise, the immediate field contains the required operand.

6.4.5 Immediate Short (IS)
In this mode the required 4-bit operand is contained within the 16-bit instruction. The Immediate Short addressing mode accommodates two formats; one which interprets the contents of the immediate field as positive data and the other which interprets the contents of the immediate field as negative data.

6.4.6 Immediate Short Positive (ISP)
The immediate operand is treated as a positive integer between 1 and 16.

6.4.7 Immediate Short Negative (ISN)
The immediate operand is treated as a negative integer between -1 and -16. Its internal form is a two's complement, sign-extended 16-bit number.

6.4.8 Instruction Counter Relative (ICR)
This addressing mode is used for 16-bit branch instructions. The contents of the instruction counter minus two (the address of the current instruction) is added to the sign-extended 8-bit displacement field within the instruction. This sum then points to the memory address to which control will be transferred if the branch is taken.

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T-49-19-16

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

6.4.9 Base Relative (B)

There are two formats which implement Base Relative Addressing; one allows indexing and one does not. For the non-indexable form, the contents of the instruction specified base register (BR = BR' + 12) is added to the 8-bit displacement field (DU) of the 16-bit instruction. In indexed mode, the sum of the contents of a specified index register and a specified base register forms the address of the required operand. Registers R1- R15 may be specified for indexing, whilst registers R12 - R15 may be specified as the base register.

6.4.10 Special

This addressing mode is applicable to instructions that do not follow the above formats. The instructions that use this special mode are indicated in figure 21.

2

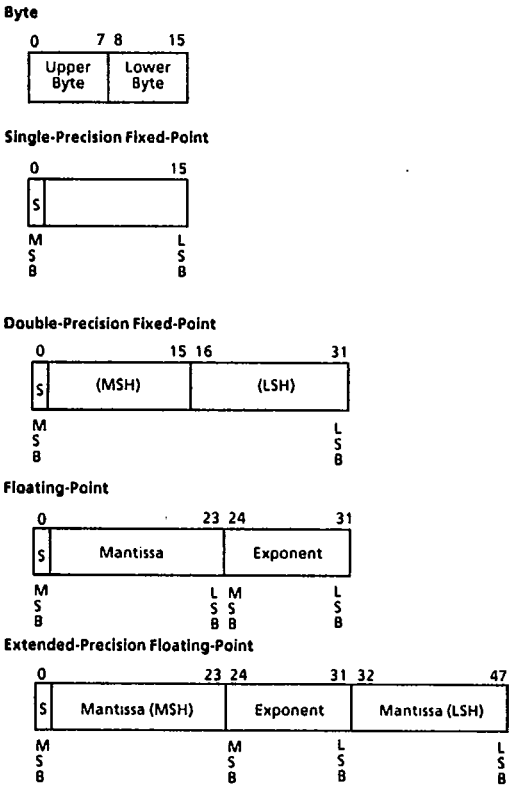

Figure 19. Data Formats

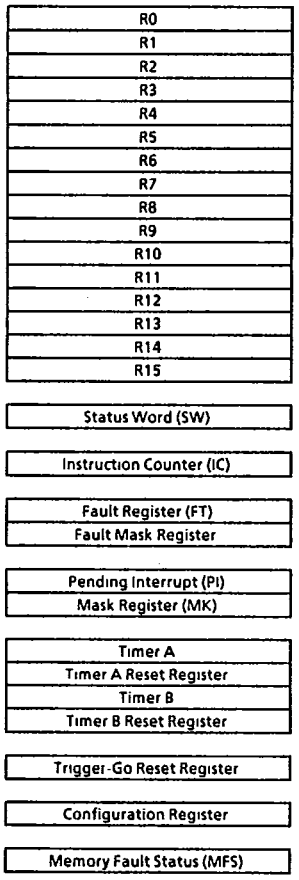

Figure 20. Register Set Model

MA31750

High Performance MIL-STD-1750 Microprocessor (Advance data)

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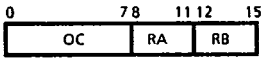
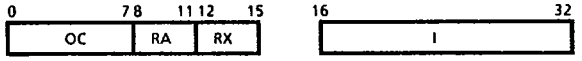
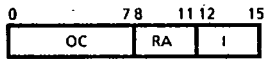
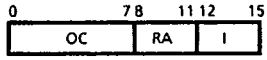
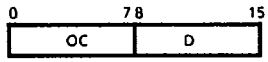
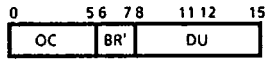
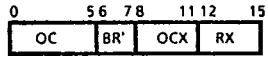
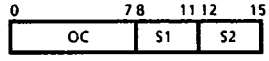
Mode	Format
1. Register Direct "R"	
2. MemoryDirect	
"D" "DX"	RX = 0 (Not-Indexed) RX ≠ 0 (Indexed)
3. Memory Indirect	
"I" "IX"	RX = 0 (Not-Indexed) RX ≠ 0 (Indexed)
4. Immediate Long a. Not Indexable "IM"	
b. Indexable	
"IM" "IMX"	RX = 0 (Not-Indexed) RX ≠ 0 (Indexed)
5. Immediate Short a. Positive "ISP"	
b. Negative "ISN"	
6. IC Relative "ICR"	
7. Base Relative a. Not Indexable "B"	 BR' = BR-12
b. Indexable	
"B" "BX"	RX = 0 (Not-Indexed) RX ≠ 0 (Indexed)
8. Special "S"	

Legend:

OC	= Operation Code
RA	= Destination Register
RB	= Source Register
RX	= Index Register
A	= Address (logical)
OCX	= Extension to Operation Code
I	= Immediate Data
D	= Displacement
BR'	= Base Register Reference
DU	= Displacement (Positive)
S1,S2	= Special Code

Figure 21. Addressing Modes

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MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

6.5 Instruction Summary

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
LOAD/STORE					
Single Precision Load	LR	R	81	1	0
	LB	B	0X	2	1
	LBX	BX	4X 0	2	1
	LISP	ISP	82	1	0
	LISN	ISN	83	1	0
	L	D,DX	80	3	0
	LIM	IM,IMX	85	2	0
	LI	I,IX	84	4	0
Double-Precision Load	DLR	R	87	1	0
	DLB	B	0X	3	1
	DLBX	BX	4X 1	3	1
	DL	D,DX	86	4	0
	DLI	I,IX	88	5	0
Single-Precision Store	STB	B	0X	2	0
	STBX	BX	4X 2	2	1
	ST	D,DX	90	3	0
	STI	I,IX	94	4	0
Store a Non-Negative Constant	STC	D,DX	91	3	0
	STCI	I,IX	92	4	0
Double-Precision Store	DSTB	B	0X	3	0
	DSTX	BX	4X 3	3	1
	DST	D,DX	96	4	0
	DSTI	I,IX	98	5	0
Load Multiple Registers	LM	D,DX	89	3 + n	0
Store Multiple Registers	STM	D,DX	99	2 + n	1
INTEGER ARITHMETIC					
Single-Precision Integer Add	AR	R	A1	1	0
	AB	B	1X	2	1
	ABX	BX	4X 4	2	1
	AISP	ISP	A2	1	0
	A	D,DX	A0	3	0
	AIM	IM	4A 1	2	0
Increment Memory by a Positive Integer	INCM	D,DX	A3	4	0
Single-Precision Absolute Value of Register	ABS	R	A4	1	1.5a
Double-Precision Absolute Value of Register	DABS	R	A5	1	1.5a

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists
n = number of registers specified by move instruction

Figure 22a. Instruction Summary

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

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SEMICONDUCTORS

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
Double-Precision Integer Add	DAR	R	A7	1	0
	DA	D,DX	A6	4	0
Single Precision Integer Subtract	SR	R	B1	1	0
	SBB	B	1X	2	1
	SBBX	BX	4X 5	2	1
	SISP	ISP	B2	1	1
	S	D,DX	B0	3	0
	SIM	IM	4A 2	2	0
Decrement Memory by a Positive Integer	DECM	D,DX	B3	4	0
Single Precision Negate Register	NEG	R	B4	1	1
Double-Precision Negate Register	DNEG	R	B5	1	1
Double-Precision Integer Subtract	DSR	R	B7	1	0
	DS	D,DX	B6	4	0
Single Precision Integer Multiply with 16-Bit Product	MSR	R	C1	1	1
	MISP	ISP	C2	1	1
	MISN	ISN	C3	1	2
	MS	D,DX	C0	3	1
	MSIM	IM	4A 4	2	1
Single Precision Integer Multiply with 32-Bit Product	MR	R	C5	1	0
	MB	B	1X	2	1
	MBX	BX	4X 6	2	1
	M	D,DX	C4	3	0
	MIM	IM	4A 3	2	0
Double-Precision Integer Multiply	DMR	R	C7	1	13.5a
	DM	D,DX	C6	4	13.5a
Single Precision Integer Divide with 16-Bit Dividend	DVR	R	D1	1	23.5a
	DISP	ISP	D2	1	23.5a
	DISN	ISN	D3	1	23.5a
	DV	D,DX	D0	3	23.5a
	DVIM	IM	4A 6	2	23.5a
Single Precision Integer Divide with 32-Bit Dividend	DR	R	D5	1	28a
	DB	R	1X	2	29a
	DBX	BX	4X 7	2	29a
	D	D,DX	D4	3	28a
	DIM	IM	4A 5	2	28a
Double-Precision Integer Divide	DDR	R	D7	1	41a
	DD	D,DX	D6	4	41a

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists

Figure 22a. (continued). Instruction Summary

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SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

Operation	Mnemonic	Format	Op Code/Ext	Cycles * M	Cycles * P
LOGICAL					
Inclusive Logical OR	ORR	R	E1	1	0
	ORB	B	3X	2	1
	ORBX	BX	4X F	2	1
	OR	D,DX	E0	3	0
	ORIM	IM	4A 8	2	0
Logical AND	ANDR	R	E3	1	0
	ANDB	B	3X	2	1
	ANDX	BX	4X E	2	1
	AND	D,DX	E2	3	0
	ANDM	IM	4A 7	2	0
Exclusive Logical OR	XORR	R	E5	1	0
	XOR	D,DX	E4	3	0
	XORM	IM	4A 9	2	0
Logical NAND	NR	R	E7	1	0
	N	D,DX	E6	3	0
	NIM	IM	4A B	2	0
Set Bit	SBR	R	51	1	0
	SB	D,DX	50	4	0
	SBI	I,IX	52	5	0
Reset Bit	RBR	R	54	1	0
	RB	D,DX	53	4	0
	RBI	I,IX	55	5	0
Test Bit	TBR	R	57	1	0
	TB	D,DX	56	3	0
	TBI	I,IX	58	4	0
Test and Set Bit	TSB	D,DX	59	2	2.5a
Set Variable Bit in Register	SVBR	R	5A	1	0
Reset Variable Bit in Register	RVBR	R	5C	1	0
Test Variable Bit in Register	TVBR	R	5E	1	0
Store Register Through Mask	SRM	D,DX	97	4	1
BYTE					
Load From Upper Byte	LUB	D,DX	8B	3	1
	LUBI	I,IX	8D	4	1
Load From Lower Byte	LLB	D,DX	8C	3	0
	LLBI	I,IX	8E	4	0
Store Into Upper Byte	STUB	D,DX	9B	4	0
	SUBI	I,IX	9D	5	0
Store Into Lower Byte	STLB	D,DX	9C	4	1
	SLBI	I,IX	9E	5	1
Exchange Bytes in Register	XBR	S	EC	1	0

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists

Figure 22a (continued). Instruction Summary

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

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SEMICONDUCTORS

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
COMPARE					
Single-Precision Compare	CR	R	F1	1	0
	CB	B	3X	2	1
	CBX	BX	4X C	2	1
	CISP	ISP	F2	1	1
	CISN	ISN	F3	1	0
	C	D,DX	F0	3	0
	CIM	IM	4A A	2	0
Compare Between Limits	CBL	D,DX	F4	4	2.7a
Double-Precision Compare	DCR	R	F7	1	0
	DC	D,DX	F6	4	0
JUMP/BRANCH					
Jump on Condition	JC	D,DX	70	3a	0
	JCI	I,IX	71	3.5a	0
Jump to Subroutine	JS	D,DX	72	2	1
Subtract One and Jump	SOJ	D,DX	73	3a	0
Branch Unconditionally	BR	ICR	74	2	1
Branch if Equal to (Zero)	BEZ	ICR	75	2a	0
Branch if Less than (Zero)	BLT	ICR	76	2a	0
Branch to Executive	BEX	S	77	11	14
Branch if Less than or Equal to (Zero)	BLE	ICR	78	2a	0
Branch if Greater than (Zero)	BGT	ICR	79	2a	0
Branch if Not Equal to (Zero)	BNZ	ICR	7A	2a	0
Branch if Greater than or Equal to (Zero)	BGE	ICR	7B	2a	0
SHIFT					
Shift Left Logical	SLL	R	60	1	0
Shift Right Logical	SRL	R	61	1	0
Shift Right Arithmetic	SRA	R	62	1	0
Shift Left Cyclic	SLC	R	63	1	0
Double Shift Left Logical	DSLL	R	65	1	0
Double Shift Right Logical	DSRL	R	66	1	0
Double Shift Right Arithmetic	DSRA	R	67	1	0
Double Shift Left Cyclic	DSLC	R	68	1	0
Shift Logical, Count in Register	SLR	R	6A	1	2
Shift Arithmetic, Count in Register	SAR	R	6B	1	5a
Shift Cyclic, Count in Register	SCR	R	6C	1	2
Double Shift Logical, Count in Register	DSLR	R	6D	1	2
Double Shift Arithmetic, Count in Register	DSAR	R	6E	1	5
Double Shift Cyclic, Count in Register	DSCR	R	6F	1	2

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists

Figure 22a (Continued). Instruction Summary

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SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
CONVERT					
Convert Floating-Point to 16-Bit Integer	FIX	R	E8	1	7.1a
Convert 16-Bit Integer to Floating-Point	FLT	R	E9	1	3
Convert Extended-Precision Floating-Point to 32-Bit Integer	EFIX	R	EA	1	8.5a
Convert 32-Bit Integer to Extended-Precision Floating-Point	EFLT	R	EB	1	9
STACK					
Stack IC and Jump to Subroutine	SJS	D,DX	7E	3	1
Unstack IC and return from Subroutine	URS	S	7F	3	1
Pop Multiple registers off the Stack	POPM	S	8F	1 + n (n = 0 to 15)	4
Push Multiple Registers onto the Stack	PSHM	S	9F	1 + n (n = 0 to 15)	8
I/O (See I/O Command Summary)					
Execute I/O	XIO**	IM,IMX	48	3	4.3a
Vectored I/O (n transfers)	VIO**	D,DX	49	2 + n	TBD
SPECIAL					
Move Multiple Words, Memory-to-Memory	MOV	S	93	1 + 2n	7
Exchange Words in Registers	XWR	R	ED	1	2
Load Status	LST**	D,DX	7D	6	1
	LSTI**	I,IX	7C	7	1
No Operation	NOP	S	FF	1	2
Break Point	BPT	S	FF	1	6

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists
** Privileged instruction.
n = number of words to be transferred

Figure 22a (Continued). Instruction Summary

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

GEC PLESSEY
SEMICONDUCTORS

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
FLOATING-POINT					
Extended-Precision Floating-Point Load	EFL	D,DX	8A	5	0
Extended-Precision Floating-Point Store	EFST	D,DX	9A	5	0
Floating-Point Absolute Value of Register	FABS	R	AC	1	2wa
Floating-Point Negate Register	FNEG	R	BC	1	3wa
Floating-Point Compare	FCR	R	F9	1	3.7wa
	FCB	B	3X	3	3.7wa
	FCBX	BX	4X D	3	3.7wa
	FC	D,DX	F8	4	3.7wa
Extended-Precision Floating-Point Compare	EFCR	R	FB	1	4wa
	EFC	D,DX	FA	5	2wa
Floating-Point Add	FAR	R	A9	1	7wa
	FAB	B	2X	3	8.5wa
	FABX	BX	4X 8	3	8.5wa
	FA	D,DX	A8	4	8.5wa
Extended-Precision Floating-Point Add	EFAR	R	AB	1	21wa
	EFA	D,DX	AA	5	20wa
Floating-Point Subtract	FSR	R	B9	1	9wa
	FSB	B	2X	3	10wa
	FSBX	BX	4X 9	3	10wa
	FS	D,DX	B8	4	9wa
Extended-Precision Floating-Point Subtract	EFSR	R	BB	1	23wa
	EFS	D,DX	BA	5	22wa
Floating-Point Multiply	FMR	R	C9	1	0
	FMB	B	2X	3	1
	FMBX	BX	4X A	3	1
	FM	D,DX	C8	4	0
Extended-Precision Floating-point Multiply	EFMR	R	CB	1	27wa
	EFM	D,DX	CA	5	26wa
Floating-Point Divide	FDR	R	D9	1	42.8wa
	FDB	B	2X	3	43.8wa
	FDBX	BX	4X B	3	43.8wa
	FD	D,DX	D8	4	42.8wa
Extended-Precision Floating-Point Divide	EFDR	R	DB	1	112.6wa
	EFD	D,DX	DA	5	112.6wa

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists
wa = weighted average favouring one or more possible alternatives

Figure 22a (Continued). Instruction Summary

GEC PLESSEY
SEMICONDUCTORS

MA31750 T-49-19-16

High Performance MIL-STD-1750 Microprocessor

(Advance data)

Operation	Mnemonic	Format	Op Code/Ext	Cycles *	
				M	P
1750B MODE INSTRUCTIONS The following instructions may only be executed in 1750B mode - illegal in 1750A					
'LONG' LOADS AND STORES					
Long Load Single	LSL	S	CC	3	11
Long Load Double	LDL	S	CD	4	20
Long Load Extended Precision Floating Point	LEFL	S	CE	5	27
Long Store Single	LSS	S	DC	4	9
Long Store Double	LDS	S	DD	6	16
Long Store Extended Floating Point	LEFS	S	DE	8	23
UNSIGNED ARITHMETIC					
Unsigned Integer Add	UAR UA	R D, DX	AD AE	1 3	4 4
Unsigned Integer Subtract	USR US	R D, DX	BD BE	1 3	4 4
Unsigned Integer Compare	UCR UC UCIM	R D, DX IM	FC FD 4A 0	1 3 2	5 5 5
BYTE LOADS AND STORES					
Load Byte	LBY	S	BF	2	3
Load Byte With Increment	LBYI	S	AF	2	3
Store Byte	SBY	S	DF	2	3
Store Byte With Increment	SBYI	S	CF	2	3
MISCELLANEOUS					
Search First Bit Set	SFBS	R	95	1	3.75a

*M = memory, P = processor (2 CLK cycles)
a = average if more than one alternative exists

Figure 22b: MIL-STD-1750B Instruction Summary

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

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6.6 I/O Comman Summary

Operation	Command Code (Hex)	Mnemonic
Implemented in MA31750 1750A or 1750B mode		
Set Fault Register		
Set Interrupt Mask	0401	SFR
Clear Interrupt Request	2000	SMK
Enable Interrupts	2001	CLIR
Disable Interrupts	2002	ENBL
Reset Pending Interrupt	2003	DSBL
Set Pending Interrupt Reg.	2004	RPI
Reset Normal Power Up Line	2005	SPI
Write Status Word	200A	RNS
Enable Start-Up ROM	200E	WSW
Disable Start-Up ROM	4004	ESUR
Direct Memory Access Enable	4005	DSUR
Direct Memory Access Disable	4006	DMAE
Timer A Start	4007	DMAD
Timer A Halt	4008	TAS
Output Timer A	4009	TAH
Reset Trigger-Go	400A	OTA
Timer B Start	400B	GO
Timer B Halt	400C	TBS
Output Timer B	400D	TBH
	400E	OTB
Read Configuration Word		
Read Fault Register,no Clear	8410	RCW
Read Interrupt Mask	8401	RFR
Read Pending Interrupt Reg.	A000	RMK
Read Status Word	A004	RPIR
Read and Clear Fault Reg.	A00E	RSW
Input Timer A	A00F	RCFR
Input Timer B	C00A	ITA
	C00E	ITB
MEDL Defined XIOs		
Write Internal config. word	040C	WCW
Read Fault Register (No clear)	8401	RFR
Read Linkage Pointer	8404	RLP
Read Processor Status	8405	RPS
Read OAS register	8406	ROS
Input Internal config. word	840C	ICW
Run Built In Test	840D	BIT
Read External Configuration	8410	RCW

Operation	Command Code (Hex)	Mnemonic
Implemented in MA31750 - 1750B mode only		
Output Timer A Reset Reg.	4002	OTAR
Output Timer B Reset Reg.	400F	OTBR
Input Timer A Reset Register	C002	ITAR
Input Timer B Reset Register	C00F	ITBR
Set Fault Mask	2006	SFMK
Write Page Bank Select	200F	WPBS
Read Page Bank Select	A00C	RPBS
Read Fault Mask	A006	RFMK
Implemented in BPU		
Memory Protect Enable	4003	MPEN
Load Memory Protect RAM	50XX	LMP
Read Memory Protect RAM	D0XX	RMP
Load Ext. Mem. Protect RAM	4XXX	LXMP
Read Ext. Mem. Protect RAM	CXXX	RXMP
Implemented in MMU		
Write Instruction Page Reg.	51XY	WIPR
Write Operand Page Reg.	52XY	WOPR
Read Memory Fault Status	A00D	RMFS
Read Instruction Page Reg.	D1XY	RIPR
Read Operand Page Reg.	D2XY	ROPR
Console Mode		
Console Output	4000	CO
Console input	C000	CI
Clear Console	4001	CLC
Reserved by MEDL (Not available to the user)		
Initialise PIC	0403	PICINIT
Load OAS register	0406	LOS
Set NPU	040A	RNPU

Figure 22c. Internal I/O Command Summary

T-49-19-16

GEC PLESSEY
SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

7 Timing Diagrams

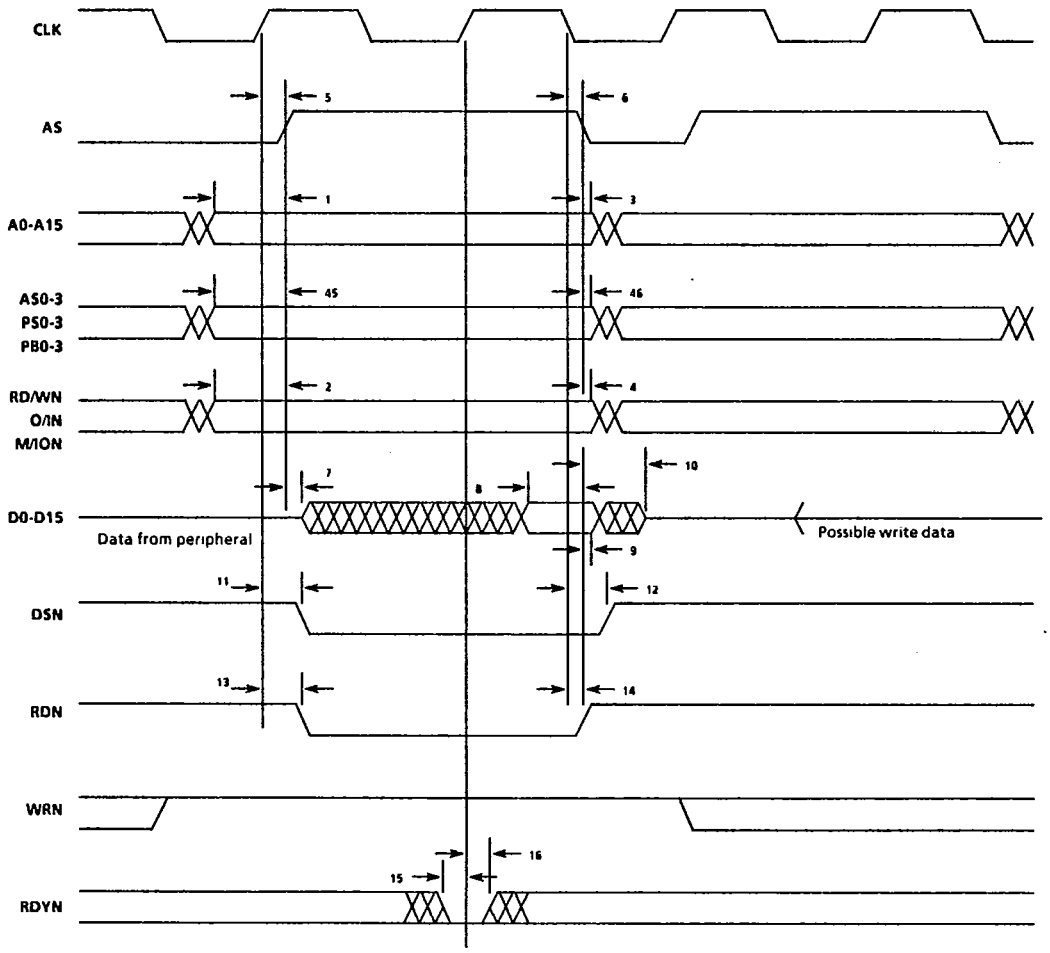

Figure 23: Read Cycle Timing

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

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SEMICONDUCTORS

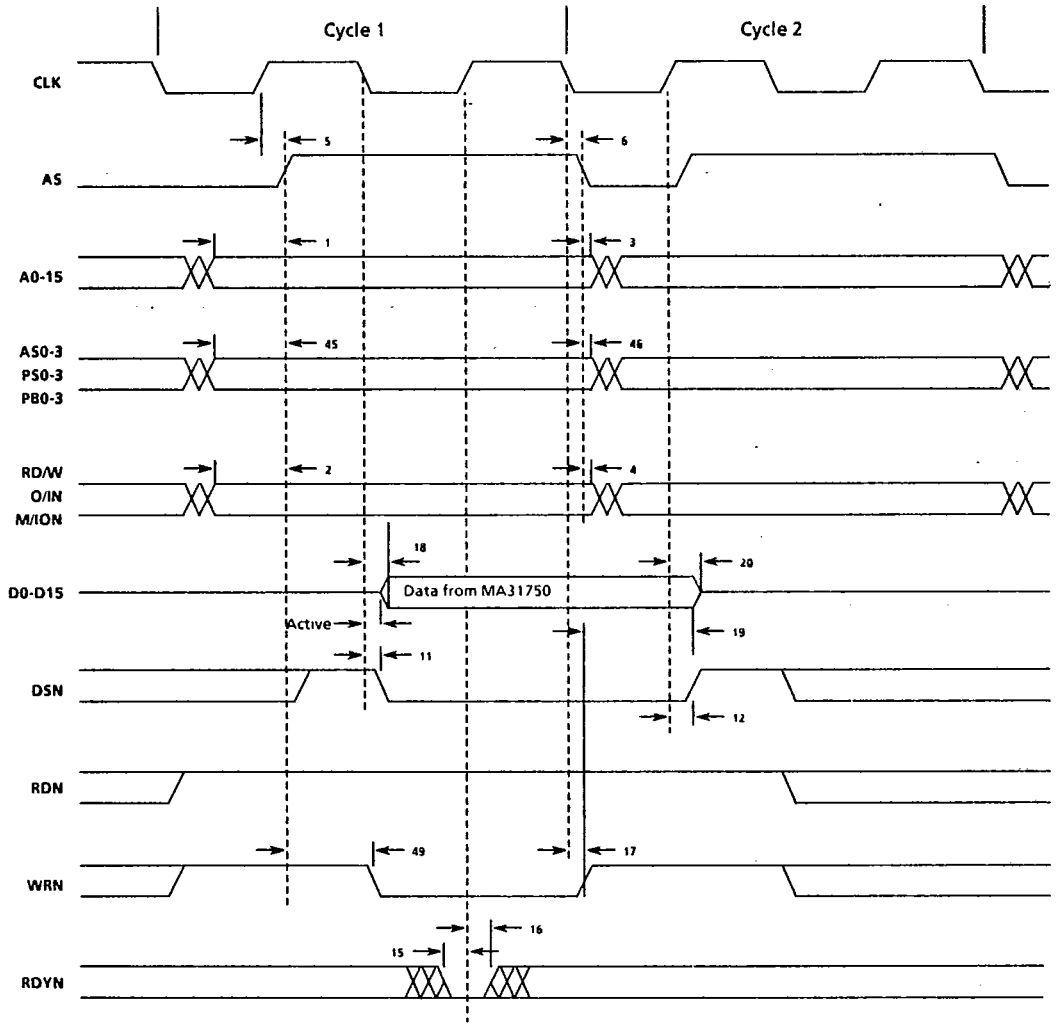

Figure 25: Write Cycle Timing

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T-49-19-16

MA31750

High performance MIL-STD-1750 Microprocessor

(Advance data)

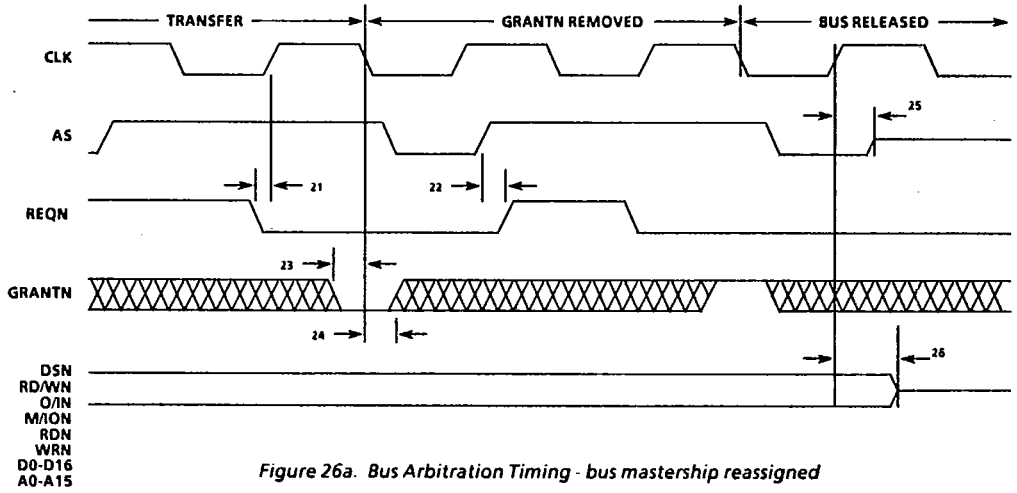

Figure 26a. Bus Arbitration Timing - bus mastership reassigned

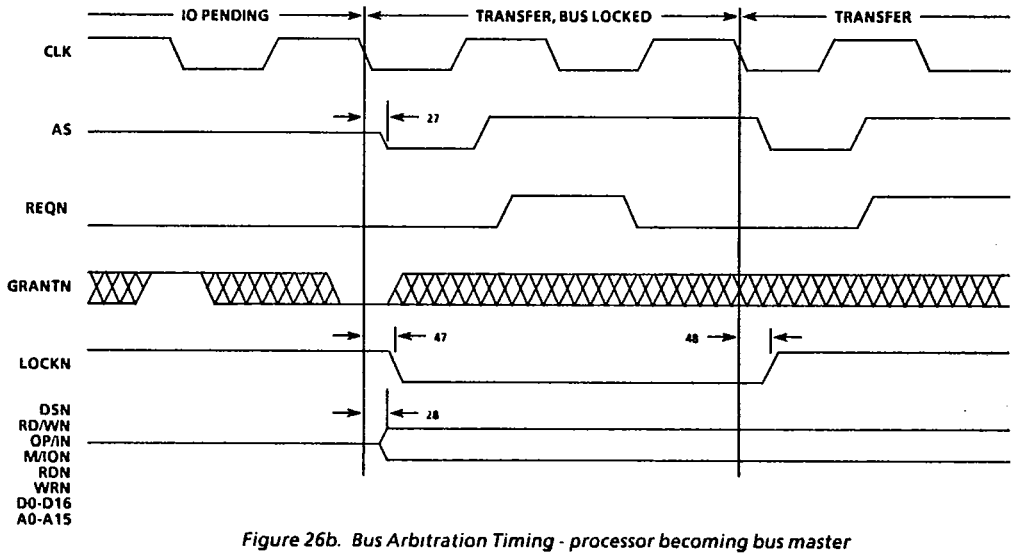

Figure 26b. Bus Arbitration Timing - processor becoming bus master

MA31750

High performance MIL-STD-1750 Microprocessor
(Advance data)

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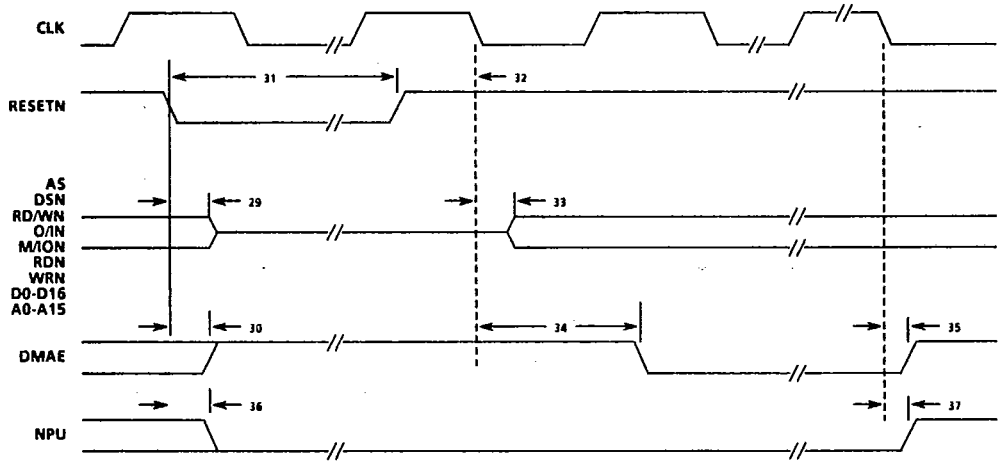

Figure 27. Reset Timing

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MA31750

High performance MIL-STD-1750 Microprocessor

(Advance data)

2

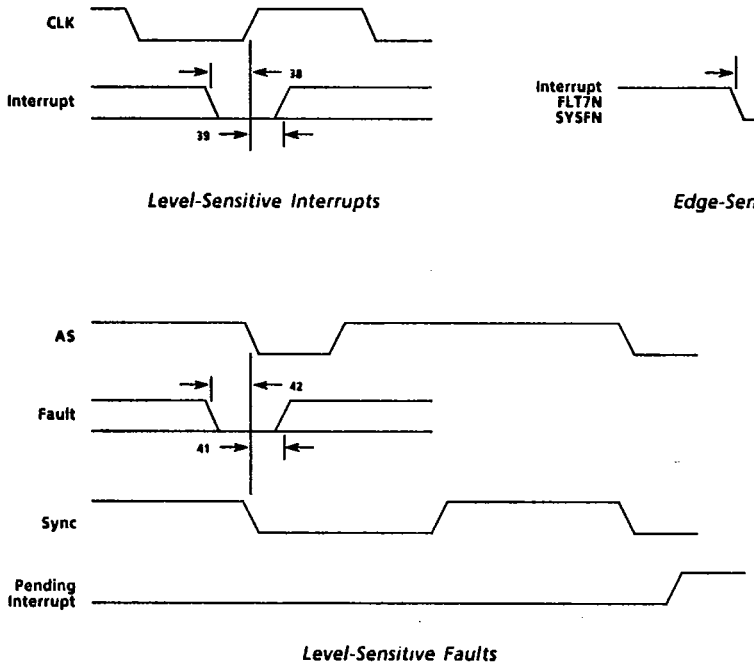

Figure 28. External Interrupt and Fault timing

MA31750

High performance MIL-STD-1750 Microprocessor

(Advance data)

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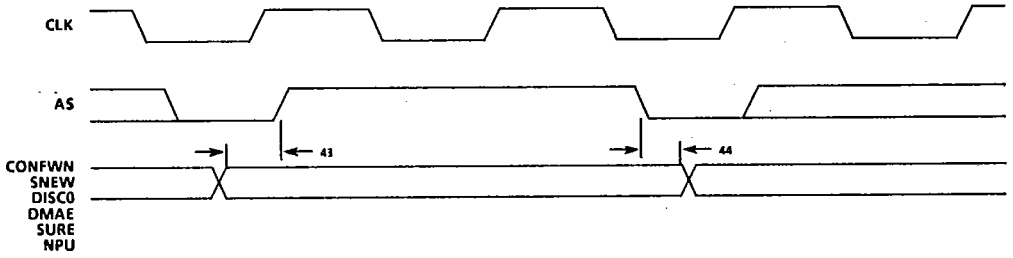

Figure 29. Discrete Output Timing

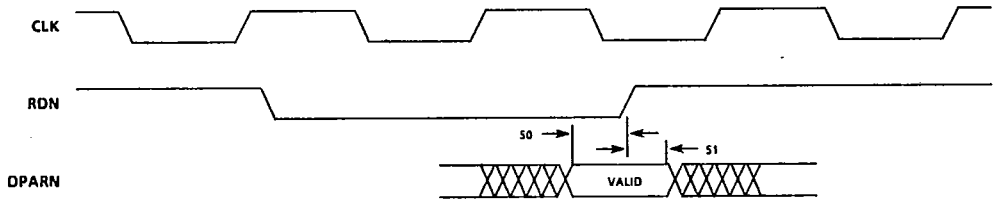

Figure 30. DPARN Input Timing

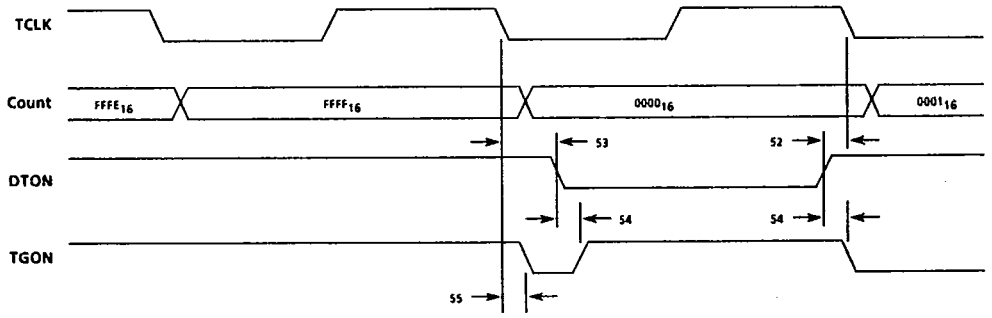

Figure 31. Trigger-Go Timing

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MA31750

High performance MIL-STD-1750 Microprocessor (Advance data)

8 Preliminary Timing Parameters

NO.	Parameter	Min.	Typ.	Max.	Units
1	Address valid to AS ↑	-	10	-	ns
2	RD/WN, OP/IN & M/ION valid to AS ↑	-	10	-	ns
3	Address hold after AS ↓	-	5	-	ns
4	RD/WN, OP/IN & M/ION valid after AS ↓	-	5	-	ns
5	AS ↑ from CLK ↑	-	10	-	ns
6	AS ↓ from CLK ↓	-	10	-	ns
7	AS ↑ to data bus low-Z (read)	5	-	-	ns
8	Data setup to RDN ↑ (read)	10	-	-	ns
9	Data hold after RDN ↑ (read)	-	-	0	ns
10	RDN ↑ to data bus high-Z (read)	-	-	30	ns
11	CLK ↓ to DSN ↓	-	10	-	ns
12	CLK ↑ to DSN ↑	-	10	-	ns
13	CLK ↑ to RDN ↓	-	10	-	ns
14	CLK ↓ to RDN ↑	-	-	5	ns
15	RDYN setup to CLK ↑	0	-	5	ns
16	RDYN hold after CLK ↑	0	-	5	ns
17	CLK ↓ to WRN ↑	-	10	-	ns
18	Data valid from CLK ↑	10	-	-	ns
19	Data valid after WRN ↑	20	-	-	ns
20	CLK ↓ to data bus high-Z (write)	-	-	15	ns
21	REQN ↓ to CLK ↑	0	-	-	ns
22	REQN ↑ from AS ↑	0	-	5	ns
23	GRANTN setup to CLK ↓	-	-	10	ns
24	GRANTN hold after CLK ↓	-	-	0	ns
25	CLK ↑ to AS high-Z	-	-	15	ns
26	CLK ↑ to control lines and busses high-Z	-	-	15	ns
27	CLK ↓ to AS low-Z	-	-	10	ns
28	CLK ↓ to control lines and busses low-Z	-	-	10	ns
29	RESETN ↓ to control lines and busses high-Z	-	-	10	ns
30	RESETN ↓ to DMAE ↑	-	-	10	ns
31	RESETN ↓ to RESETN ↑	3	-	-	CLK
32	RESETN ↑ setup to CLK ↓	10	-	-	ns
33	CLK ↓ to control lines and busses low-Z	-	-	10	ns
34	CLK ↓ to DMAE ↓	-	-	50	ns

Figure 32. Timing Parameters - PRELIMINARY INFORMATION ONLY

MA31750

High performance MIL-STD-1750 Microprocessor

(Advance Data)

GEC PLESSEY
SEMICONDUCTORS

Preliminary Timing Parameters (continued)

NO.	Parameter	Min.	Typ.	Max.	Units
35	CLK ↓ to DMAE ↑ (following XIO DMAE)	-	10	-	ns
36	RESETN ↓ to NPU ↓	-	10	-	ns
37	CLK ↓ to NPU ↑ (following successful power-up)	-	10	-	ns
38	Interrupt setup to CLK ↑	10	-	-	ns
39	Interrupt hold after CLK ↑	0	-	-	ns
40	Interrupt pulse width (edge-sensitive)	10	-	-	ns
41	Fault setup to AS ↓	10	-	-	ns
42	Fault hold after AS ↓	0	-	-	ns
43	Discretes valid after AS ↑	-	10	-	ns
44	Discretes valid after AS ↓	-	10	-	ns
45	AS0-3, PS0-3, PB0-3 valid to AS ↑	-	10	-	ns
46	AS0-3, PS0-3, PB0-3 invalid after AS ↓	-	10	-	ns
47	LOCKN ↓ from CLK ↓	10	-	-	ns
48	LOCKN ↑ from CLK ↓	10	-	-	ns
49	AS ↑ to WRN ↓	-	25	-	ns
50	DPARN setup to RDN ↑	10	-	-	ns
51	DPARN hold after RDN ↑	0	-	10	ns
52	DTON setup to TCLK ↓	0	-	10	ns
53	DTON hold after TCLK ↓	0	-	10	ns
54	DTON to TGON	0	-	15	ns
55	TCLK ↓ to TGON ↓	0	-	15	ns

Figure 32 (continued). Timing Parameters - PRELIMINARY INFORMATION ONLY

NOTE: Timing parameters shown are preliminary and should be used as a guide only. Accurate timings will be available following full device characterisation.

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SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

9 Ratings and Characteristics

Parameter	Min.	Max.	Units
Supply voltage	-0.5	10	V
Input voltage	-0.3	V_{DD} + 0.3	V
Current through any pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 33: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad (Si)			Total dose ≤1 MRad (Si)		Units
			Min.	Typ.	Max.	Min.	Max.	
V_{DD}	Supply voltage	-	4.5	5.0	5.5	4.5	5.5	V
V_{IH1}	TTL input high voltage	-	2.0	-	-	2.0	-	V
V_{IL1}	TTL input low voltage	-	-	-	0.8	-	0.3	V
V_{CKH1}	CLK input high voltage	-	V_{DD}-0.5	-	V_{DD}	-	-	V
V_{CKL1}	CLK input low voltage	-	0.0	-	0.5	-	-	V
V_{OH1}	Output high voltage	I_{OH} = -0.8mA	2.4	-	-	2.4	-	V
V_{OL1}	Output low voltage	I_{OL} = 2.0mA	-	-	0.4	-	0.4	V
I_{IL}	Input low current	-	-	-	10	-	100	uA
I_{IH}	Input high current	-	-	-	10	-	100	uA
I_{DDYN}	Dynamic power supply current	-	-	-	100	-	100	mA

V_{DD} = 5V ± 10%, over full operating temperature range.

Figure 34: Operating DC Electrical Characteristics

Parameter	Min.	Max.	Units
Clock Frequency CLK	0	25	MHz
Clock Duty Cycle	45	55	%

Figure 35: Operating AC Electrical Characteristics

MA31750

High performance MIL-STD-1750 Microprocessor

(Advance Data)

GEC PLESSEY

SEMICONDUCTORS

10 Pin Assignments and Outlines

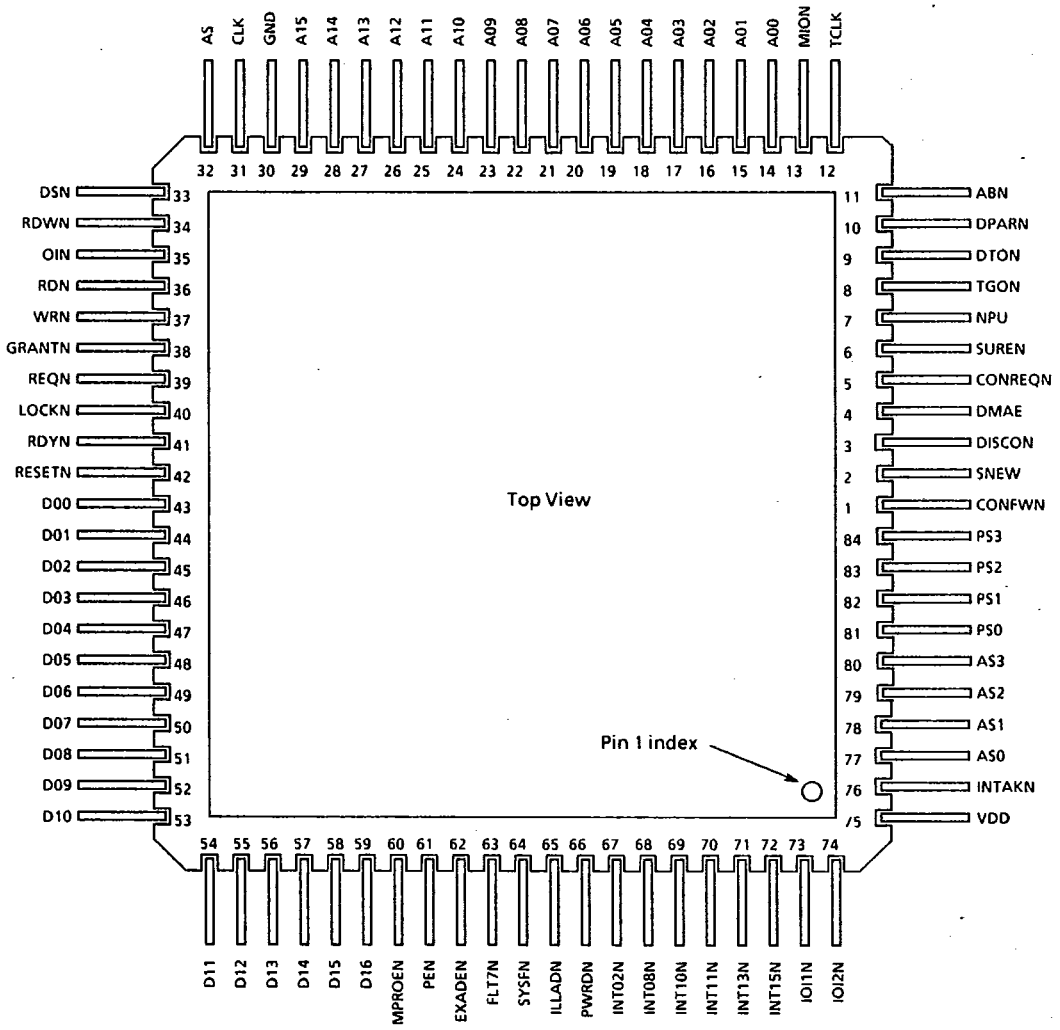

Figure 36: 84-Lead Flatpack Style F

T-49-19-16

GEC PLESSEY

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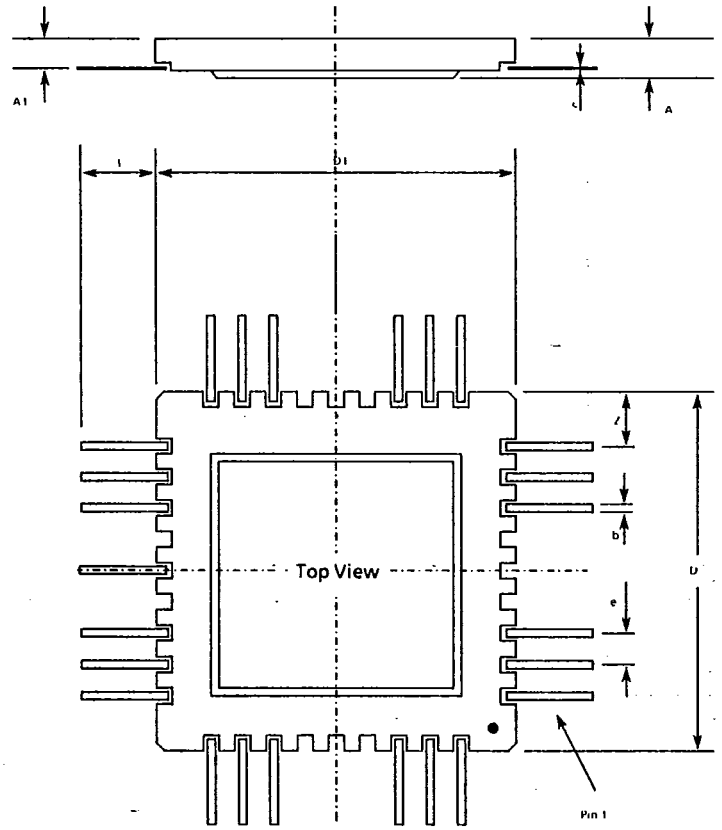
MA31750

High performance MIL-STD-1750 Microprocessor

(Advance Data)



Ref.	Inches		
	Max.	Nom.	Min.
A	0.081	-	-
A1	0.044	-	0.036
b	0.020	-	0.017
c	0.012	-	0.009
D, D1	1.173	-	1.149
e	-	0.050	-
L	0.325	-	0.290

XG524

MA31750

High performance MIL-STD-1750 Microprocessor

(Advance Data)

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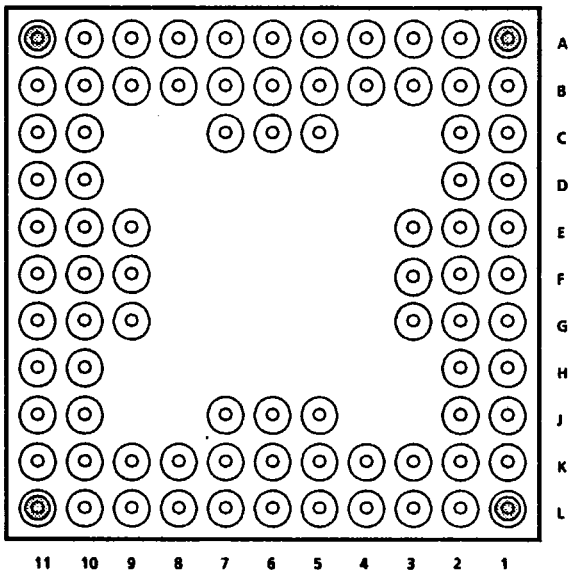
SEMICONDUCTORS



Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	IOI2N	B11	D08	F9	D00	K2	TCLK
A2	INT15N	C1	AS1	F10	RESETN	K3	MION
A3	INT13N	C2	INTAKN	F11	D04	K4	A02
A4	INT10N	C5	ILLADN	G1	DISCON	K5	A05
A5	PWRDN	C6	SYSFN	G2	DMAE	K6	A04
A6	INT08N	C7	MPROEN	G3	CONREQN	K7	A11
A7	EXADEN	C10	D09	G9	REQN	K8	A14
A8	D16	C11	D07	G10	LOCKN	K9	CLK
A9	D14	D1	AS3	G11	RDYN	K10	DSN
A10	D13	D2	AS2	H1	SUREN	K11	OIN
A11	D10	D10	D06	H2	NPU	L1	ABN
B1	AS0	D11	D05	H10	WRN	L2	A00
B2	VDD	E1	PS2	H11	GRANTN	L3	A01
B3	IOI1N	E2	PS1	J1	TGON	L4	A03
B4	INT11N	E3	PS3	J2	DPARN	L5	A06
B5	INT02N	E9	D01	J5	A07	L6	A09
B6	FLT7N	E10	D03	J6	A08	L7	A10
B7	PEN	E11	D02	J7	A12	L8	A13
B8	D15	F1	SNEW	J10	RDWN	L9	A15
B9	D12	F2	PS0	J11	RDN	L10	GND
B10	D11	F3	CONFWN	K1	DTON	L11	AS

XG640

Figure 37: 84-Pin Grid Array Style A

T-49-19-16

GEC PLESSEY

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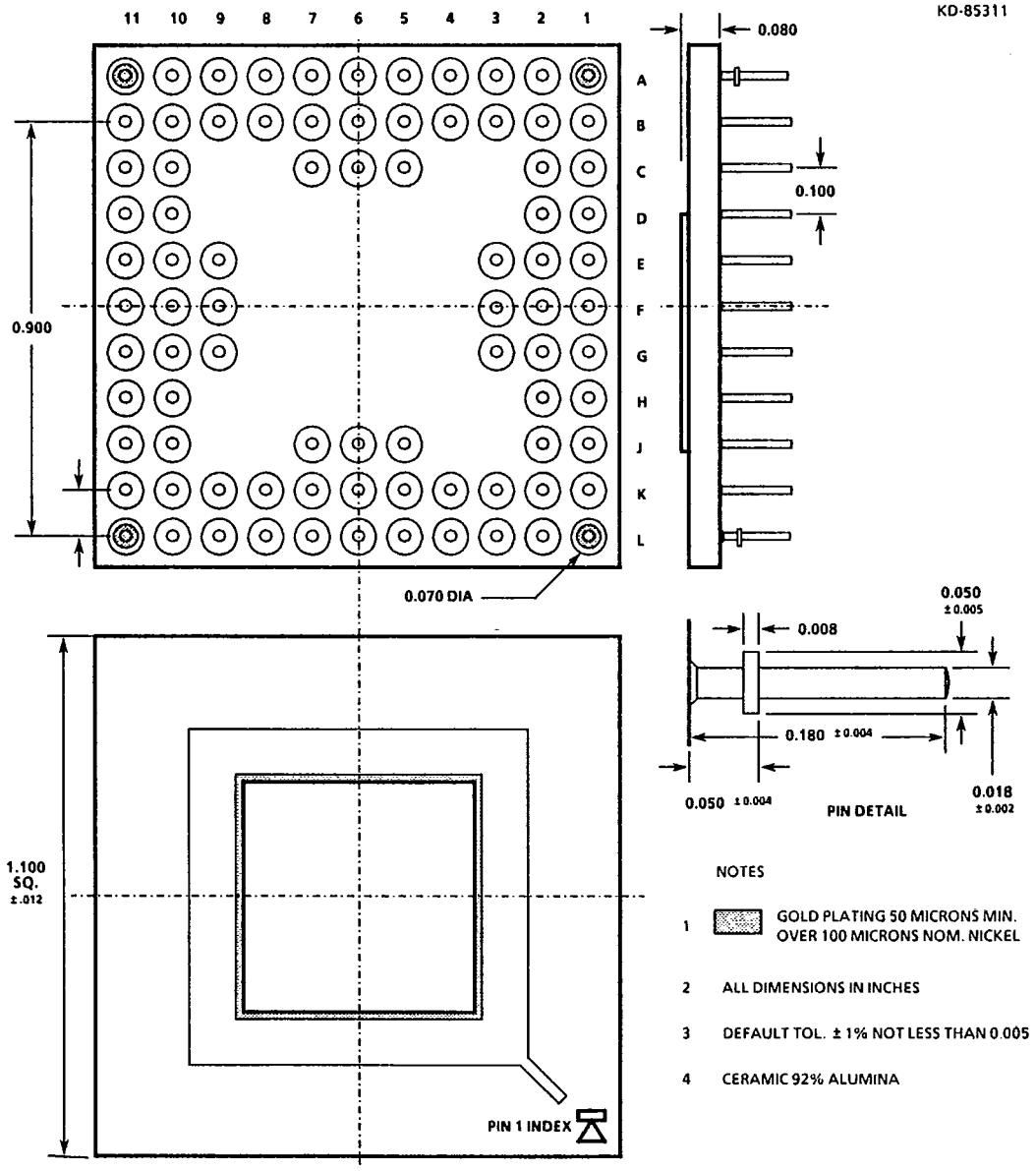
MA31750

High performance MIL-STD-1750 Microprocessor

(Advance Data)



NOTES

1. GOLD PLATING 50 MICRONS MIN. OVER 100 MICRONS NOM. NICKEL
2. ALL DIMENSIONS IN INCHES
3. DEFAULT TOL. ± 1% NOT LESS THAN 0.005
4. CERAMIC 92% ALUMINA

MA31750

High performance MIL-STD-1750 Microprocessor

(Advance Data)

GEC PLESSEY

SEMICONDUCTORS

11 Radiation Tolerance

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

Marconi Electronic Devices can provide radiation testing compliant with MIL STD 883C remote sensing method 1019 notice 5.

Total Dose (Function to specification) - note 1	$1x10^6$ Rad(Si)
Total Dose (Function to specification) - note 2	$3x10^5$ Rad(Si)
Transient Upset (stored data loss)	$3x10^{10}$ Rad(Si)/sec
Transient Upset (survivability)	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	10^{15}neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

Note 1: All CMOS inputs
Note 2: TTL inputs

Figure 40: Radiation Hardness Parameters

T-49-19-16

GEC PLESSEY
SEMICONDUCTORS

MA31750

High Performance MIL-STD-1750 Microprocessor

(Advance data)

12 Ordering Information

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards' section 9.