MN64782

D/A Converter for Digital Audio Equipment

■ Overview

The MN64782 is a CMOS digital-to-analog converter with a built-in 8-fold oversampling digital filter for pulse code modulation (PCM) digital audio equipment. It uses noise shaping technology to convert a digital signal into a PWM signal.

The D/A converter uses a switched capacitor to eliminate sensitivity to clock jitter.

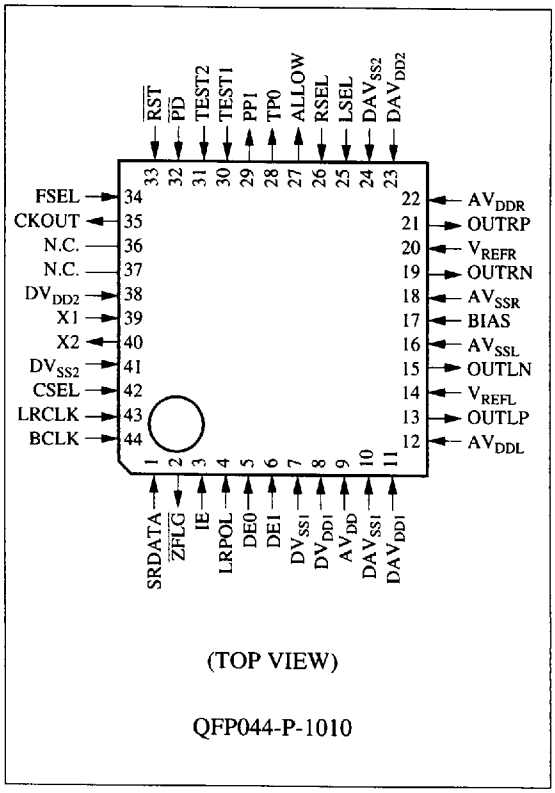
■ Features

- Built-in 8-fold oversampling digital filter
  - •Pass band: DC to 20kHz (f_s=44.1kHz)
  - •Cutoff band: 24.1kHz and up (f_s=44.1kHz)
  - •Ripple within pass band: ±0.015dB
  - •Attenuation within cutoff band: 60dB
- Built-in overflow limiter
- Built-in digital de-emphasis circuit supporting f_s frequencies of 32 kHz, 44.1 kHz, and 48 kHz
- Choice of 64- and 32-fold oversampling with 4th order noise shaping technology.
- Serial data input using 16-bit, two's complement, MSB first format. Supports both signal processing LSI and I²S formats.
- Internal resolution of 20 bits
- No zero cross distortion
- Sample-and-hold circuit is unnecessary
- Output pin for detecting zero input
- Power down mode pin
- Single 5V power supply

■ Applications

- CD, MD, and DAT players and other digital audio equipment

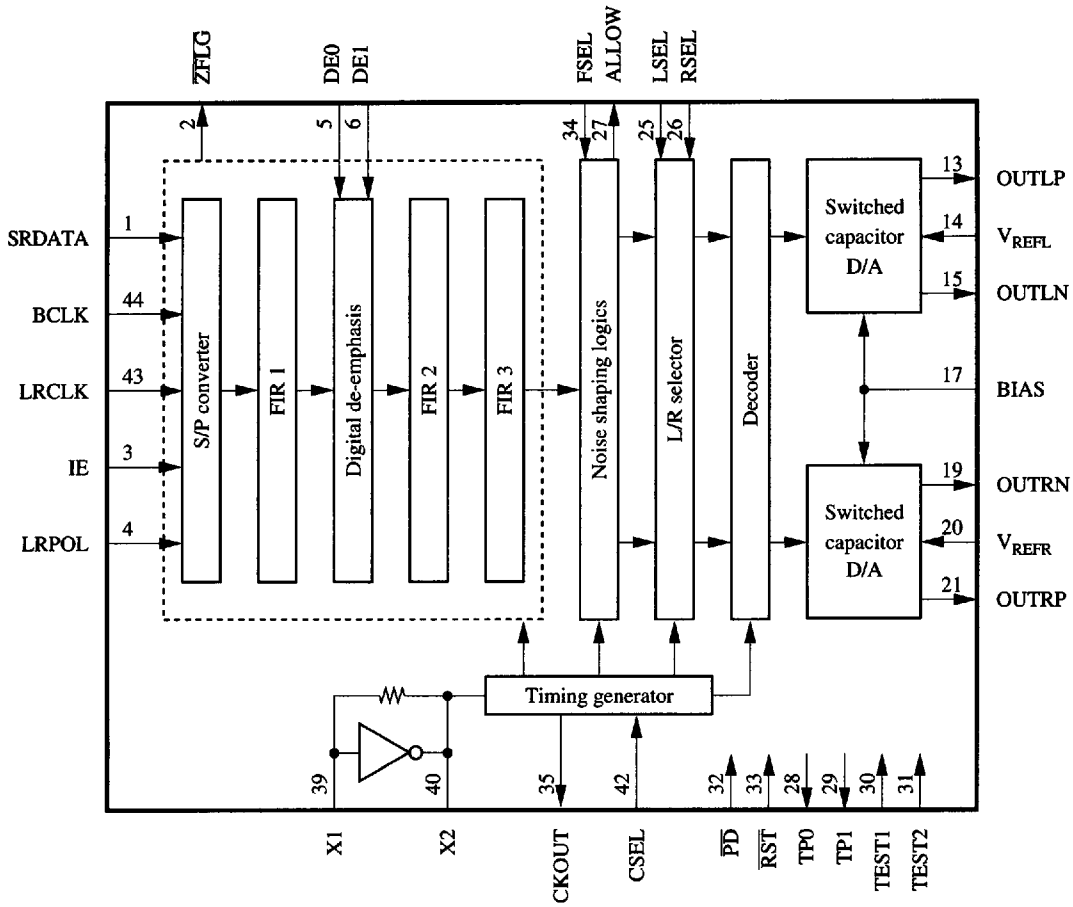
■ Pin Assignment



(TOP VIEW)

QFP044-P-1010

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	I/O	Function Description
1	SRDATA	I	Serial data input pin. This pin is inputted 16-bit serial data of two's complement and MSB first format.
2	$\overline{ZFLG}$	O	Output pin of zero input detecting flag. This pin goes to "L" level when the input data to the SRDATA pin for both left and right channels is zero for 8192 consecutive cycles.
3	IE	I	SRDATA input format selection pin. "L" level; signal processing LSI format "H" level; I^2S format.
4	LRPOL	I	LRCLK polarity selection pin. (See description of LRCLK pin.)
5	DE0	I	De-emphasis filter mode selection pins.
6	DE1	I	
7	DV_{SS1}	—	Ground pin for digital circuits. Connect this to 0V.
8	DV_{DD1}	—	Power supply pin for digital circuits. Connect this to a +5V supply.
9	AV_{DD}	—	Silicon substrate potential fixing pin. Connect this to the +5V analog power supply.
10	DAV_{SS1}	—	Ground pin for analog circuits. Connect this to 0V.
11	DAV_{DD1}	—	Power supply pin for analog circuits. Connect this to a +5V supply.
12	AV_{DDL}	—	Power supply pin for left channel analog circuits. Connect this to a +5V supply.
13	OUTLP	O	Left channel normal phase analog output pin.
14	V_{REFL}	I	Left channel reference voltage input pin.
15	OUTLN	O	Left channel inverted phase analog output pin.
16	AV_{SSL}	—	Ground pin for left channel analog circuits. Connect this to 0V.
17	BIAS	I	Operational amplifier bias pin.
18	AV_{SSR}	—	Ground pin for right channel analog circuits. Connect this to 0V.
19	OUTRN	O	Right channel inverted phase analog output pin.
20	V_{REFR}	I	Right channel reference voltage input pin.
21	OUTRP	O	Right channel normal phase analog output pin.
22	AV_{DDR}	—	Power supply pin for right channel analog circuits. Connect this to a +5V supply.
23	DAV_{DD2}	—	Power supply pin for analog circuits. Connect this to a +5V supply.
24	DAV_{SS2}	—	Ground pin for analog circuits. Connect this to 0V.
25	LSEL	I	Analog output selection pins.
26	RSEL	I	

DE0	L	L	H	H
DE1	L	H	H	L
Mode(f_s)	44.1kHz	48kHz	32kHz	OFF

LSEL	L	H	L	H
RSEL	L	L	H	H
Analog output	L/R STEREO output	Left channel output only	Right channel output only	Left and right channels reversed output

For Audio Equipment

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
27	ALLOW	O	Zero output detection flag output pin for noise shaping circuit. This pin goes to "H" level when the noise shaping circuit output data for both left and right channels is all zeros.
28	TP0	O	Test output pins. Leave these open.
29	TP1	O	Test output pins. Leave these open.
30	TEST1	I	Test input pins. Connect these to the DV_{SS} pin.
31	TEST2	I	Test input pins. Connect these to the DV_{SS} pin.
32	$\overline{PD}$	I	Power down pin. Pulling this pin to "L" level activates the power down mode.
33	$\overline{RST}$	I	Reset pin. "L" level input resets the LSI internals. Pull this pin low once after applying the power.
34	FSEL	I	Noise shaping operation clock selection pin. "L" level; 32-fold oversampling "H" level; 64-fold oversampling
35	CKOUT	O	Clock output pin. Output of the buffered master clock.
36	N.C.	—	No connection There are no wires between these and the chip.
37	N.C.	—	No connection There are no wires between these and the chip.
38	DV_{DD2}	—	Power supply pin for digital circuits. Connect this to a +5V supply.
39	X1	I	Clock input pin or crystal oscillator input pin. Input an external clock to this pin or connect this pin via a crystal oscillator to the X2 pin. Select the clock frequency with the CSEL pin.
40	X2	O	Crystal oscillator output pin. If using a crystal oscillator, connect this pin via a crystal oscillator to the X1 pin. Otherwise, leave it open.
41	DV_{SS2}	—	Ground pin for digital circuits. Connect this to 0V.
42	CSEL	I	Master clock selection pin. "L" level; the master clock of 256 f_s "H" level; of 384 f_s
43	LRCLK	I	L/R clock input pin. This pin determines the channel for SRDATA input data. The level at the LRPOL pin determines the polarity. When the LRPOL pin is at "L" level, "L" level of LRCLK indicates left channeldata input; "H" level input, right channel data input. When the LRPOL pin is at "H" level, "H" level of LRCLK indicates left channel data input; "L" level input, right channel data input.
44	BCLK	I	Bit clock input pin. The chip latches the SRDATA signal at the rising edge of this input.

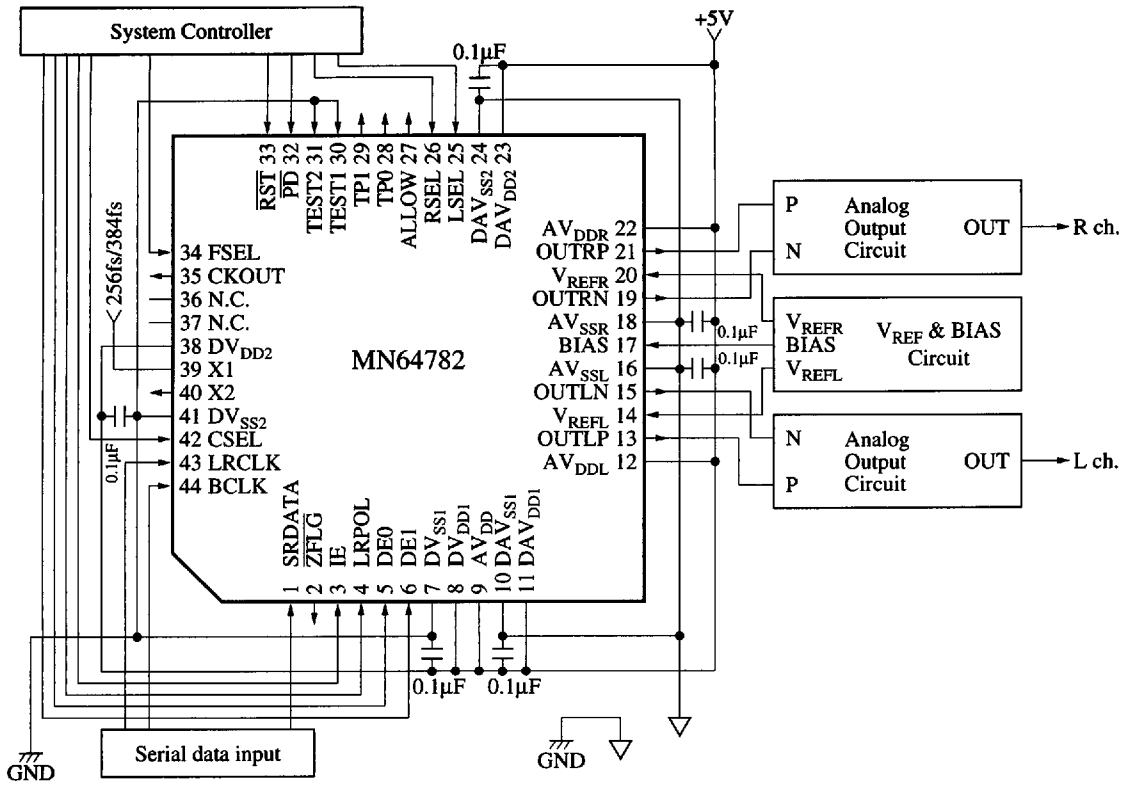
■ Conversion Characteristics

$DV_{DD}=AV_{DD}=5.0V$, $DV_{SS}=AV_{SS}=0V$, $f_{osc}=12.288MHz$, Ta=–20 to +70°C

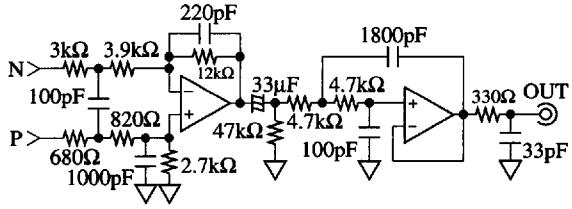
Parameter	Symbol	Test Conditions	min	typ	max	Unit
Analog characteristics *1						
Signal-to-noise ratio	S/N	EIAJ	92	96		dB
Dynamic range	D.R.	EIAJ	88	94		dB
Total harmonic distortion	THD + N	EIAJ		0.006	0.015	%
Crosstalk		EIAJ	92	96		dB
Output level		1 kHz full scale	1.5	1.8		V_{rms}

Note*1: These analog characteristics are for the application circuit example next page.

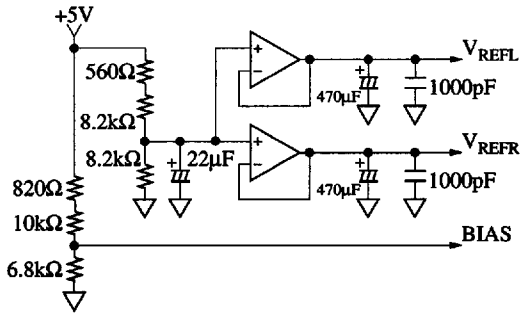
■ Application Circuit Example



Analog Output Circuit



V_{REF} & BIAS Circuit



■ Package Dimensions (Unit: mm)

QFP044-P-1010