OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -55° to +150°C
Lead Temperature Range (soldering, 10 seconds) . . . . . +325°C
Positive Voltage on any pin, with respect to Ground . . . . . V_{IO}+0.3V
Negative Voltage on any pin, with respect to Ground . . . . . -0.3V
Maximum V_{IO} . . . . . +7V
Maximum V_{CC} . . . . . V_{IO}

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C - 70°C, V_{cc} = +3.3 V ± 10%)
NOTE: NUMBERS APPEARING IN BOLD AND IN PARENTHESES REPRESENT THE VALUES FOR 5 VOLT OPERATION

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.2 **(3.0)**			V	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Input Leakage (All I and IS buffers except PWRGD)						
Low Input Leakage	I_{IL}	-10		+10	μA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	μA	V_{IN} = V_{IO}
Input Current PWRGD	I_{OH}		75	150	μA	V_{IN} = 0
I/O12 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 12 mA **(24 mA)**
High Output Level	V_{OH}	2.4			V	I_{OH} = -6 mA **(-12mA)**
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{IO} (Note 1)
O12 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 12 mA **(24 mA)**
High Output Level	V_{OH}	2.4			V	I_{OH} = -6 mA **(-12 mA)**
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{IO} (Note 1)
OP12 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 12 mA **(24 mA)**
High Output Level	V_{OH}	2.4			V	I_{OH} = -2 mA **(-4 mA)**
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{IO} (Note 1)
OD20 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 20 mA **(48 mA)**
Output Leakage	I_{OH}	-10		+10	μA	V_{OH} = 0 to V_{IO} (Note 2)
O2 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 2 mA **(4mA)**
High Output Level	V_{OH}	2.4			V	I_{OH} = -1 mA **(-1 mA)**
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{IO} (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4 mA **(8mA)**
High Output Level	V_{OH}	2.4			V	I_{OH} = -2 mA **(-4 mA)**
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{IO} (Note 1)
OD12 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 12 mA **(24 mA)**
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{IO} (Note 1)
OD12P Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 12 mA **(24 mA)**
High Output Level	V_{OH}	2.4			V	I_{OH} = -30 μA **(-30 μA)**
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{IO} (Note 1)
Supply Current Active	I_{CC}			15 **(40)**	mA	All outputs open.
Supply Current Standby	I_{CSBY}			100 **(500)**	μA	Note 3
ChiProtect (SLCT, PE, BUSY, nACK, nERROR)	I_{IL}			±10	μA	Chip in circuit: V_{CC} = 0V V_{IN} = 6V Max.

Note 1: All output leakages are measured with the current pins in high impedance as defined by the PWRGD pin.

Note 2: Output leakage is measured with the low driving output off, either for a high level output or a high impedance state defined by PWRGD.

Note 3: Defined by the device configuration with the PWRGD input low.

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 3.3V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	