Chapter 9

ELECTRICAL CHARACTERISTICS (provisional)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} +0.3	V
Operating temperature	T_A	0 to +70	°C
Storage temperature	T_{STB}	–55 to +150	°C
Power dissipation	p_D	3.0	W

Recommended Operating Conditions

Parameter		Symbol	Condition			Unit
Power supply voltage		V_{CC}	4.75	5.0	5.25	V
Input voltage high	CLK	V_{IH1}	2.8 + V_{CC}	—	V_{CC} + .3	V
Input voltage low		V_{IL1}	–.3	—	.2 + V_{CC}	V
Input voltage high	Other than CLK	V_{IH2}	2.2	—	V_{CC} + .3	V
Input voltage low		V_{IL2}	–.3	—	.8	V
Operating Temperature		T_A	0	+25	+70	°C

DC Characteristics

Parameter	Symbol	Pin	Measurement Condition	Standard Value		Unit
				Min.	Max.	
Input Voltage High	V_{IH1}	CLK		.8 +V_{CC}	V_{CC} +.3	V
Input Voltage Low	V_{IL1}			–.3	.2 +V_{CC}	V
Input Voltage High	V_{IH2}	No CLK		2.2	V_{CC} +.3	V
Input Voltage Low	V_{IL2}			–.3	.8	V
Output Voltage High	V_{OH}	Other than $\overline{DONE}$, $\overline{IRQ}$, and $\overline{XIRQ}$	I_{OH} = –400 mA	2.4	—	V
Output Voltage Low	V_{OL}	$\overline{DONE}$, $\overline{IRQ}$, and $\overline{XIRQ}$	I_{OL} = –3.2 mA	—	.5	V
Input Leakage Circuit	I_{IL}		V_I = 0 to V_{CC}	–10	10	µA
3-state (off) Output Leakage Circuit	I_{IL1}		V_I = 0 to V_{CC}	–10	10	µA
Open Drain (off) Output Leakage Circuit	I_{IL2}	$\overline{DONE}$, $\overline{IRQ}$, and $\overline{XIRQ}$	V_I = 0 to V_{CC}	–10	10	µA
Input Capacitance	C_i		f = 1 MHz	—	20	Pf
Output Capacitance	C_o		f = 1 MHz	—	20	Pf
I/O Capacitance	$C_{I/O}$		f = 1 MHz	—	20	Pf
Power Dissipation	P_d		f = 20 MHz, No load operating frequency	—	1.2	W

AC Characteristics

(V_{CC} = 5 V + 5%, V_{SS} = 0 V, T_A = 0 to 70C

No.	Parameter	Symbol	20 MHz		25 MHz		33 MHz		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
1	Clock Cycle Time	t_c	50	250	40	250	30	250	ns	Figure 9–4
2	Clock High-level Time	$t_{w\,(CH)}$	20	–	17	–	12.5	–	ns	
3	Clock Low-level Time	$t_{w\,(CL)}$	20	–	17	–	12.5	–	ns	
4	Clock Rise Time	$t_{r\,(C)}$	–	5	–	4	–	3	ns	
5	Clock Fall Time	$t_{f\,(C)}$	–	5	–	4	–	3	ns	
6	BAT, A0–29, $\overline{BC}$, $\overline{BLOCK}$ Delay Time	$t_{d\,(CH-A)}$	–	30	–	25	–	20	ns	Figure 9–5
7	BAT, A0–29, $\overline{BC}$, $\overline{BLOCK}$ Holds Time	$t_{h\,(CH-A)}$	0	–	0	–	0	–	ns	
8	BAT, A0–29, $\overline{BC}$, $\overline{BLOCK}$ Float Delay Time (Bus Master)	$t_{d\,(CH-AZ)\,M}$	–	25	–	23	–	20	ns	
9	Read Data Setup Time (Bus Master)	$t_{su\,(RD-CL)\,m}$	7	–	6	–	5	–	ns	
10	Read Data Hold Time (Bus Master)	$t_{h\,(CL-RD)\,m}$	13	–	12	–	10	–	ns	
11	Read Data Hold Time for $\overline{DS}$ Negation	$t_{h\,(DS-RD)\,M}$	0	–	0	–	0	–	ns	
12	Write Data Delay Time (Bus Master)	$t_{d\,(CH-WD)\,M}$	–	30	–	27	–	22	ns	
13	Write Data Hold Time (Bus Master)	$t_{h\,(CH-WD)\,M}$	0	–	0	–	0	–	ns	
14	Write Data Float Delay Time	$t_{d\,(CH-WDZ)\,M}$	–	25	–	23	–	20	ns	
15	$\overline{CSTR}$ Delay Time	$t_{d\,(CH-CST)}$	–	30	–	25	–	20	ns	
16	$\overline{AS}$ Delay Time	$t_{d\,(CL-AS)}$	–	30	–	25	–	20	ns	
17	$\overline{DS}$ Delay Time	$t_{d\,(C-DS)}$	–	30	–	25	–	20	ns	
18	R/$\overline{W}$ Delay Time (Bus Master)	$t_{d\,(CH-RW)\,M}$	–	30	–	25	–	20	ns	
19	R/$\overline{W}$ Hold Time (Bus Master)	$t_{h\,(CH-RW)\,M}$	0	–	0	–	0	–	ns	
20	$\overline{DBEN}$ Delay Time (Bus Master)	$t_{d\,(CH-DE)\,M}$	–	30	–	27	–	22	ns	
21	$\overline{DIN}$ Delay Time (Bus Master)	$t_{d\,(CL-DI)\,M}$	–	30	–	27	–	22	ns	
22	$\overline{DC}$ and $\overline{IORDY}$ Setup Time	$t_{su\,(DC-CH)}$	7	–	6	–	5	–	ns	
23	$\overline{DC}$ and $\overline{IORDY}$ Hold Time for $\overline{DS}$ Negation	$t_{h\,(DC-DC)}$	0	–	0	–	0	–	ns	
24	$\overline{ACK}$ Delay Time	$t_{d\,(C-AK)}$	–	30	–	25	–	20	ns	
25	$\overline{DONE}$ Delay Time (Output)	$t_{d\,(CH-DO)\,O}$	–	30	–	25	–	20	ns	
26	$\overline{DONE}$ Float Delay Time (Output)	$t_{d\,(CH-DOZ)\,O}$	–	25	–	23	–	20	ns	
27	$\overline{DONE}$ Setup Time (Input)	$t_{su\,(DO-CH)\,I}$	7	–	6	–	5	–	ns	
28	$\overline{DONE}$ Hold Time for $\overline{DS}$ Negation	$t_{h\,(DS-DO)\,I}$	0	–	0	–	0	–	ns	
29	$\overline{DONE}$ Setup Time for $\overline{DC}$ Negation	$t_{su\,(DO-DC)\,I}$	10	–	9	–	8	–	ns	
30	$\overline{BERR}$ and $\overline{RERUN}$ Setup Time	$t_{su\,(BR-CL)}$	20	–	18	–	15	–	ns	
31	$\overline{BERR}$ and $\overline{RERUN}$ Hold Time	$t_{h\,(CL-BE)}$	13	–	12	–	10	–	ns	
32	$\overline{HREQ}$ Delay Time	$t_{d\,(CL-HR)}$	–	30	–	25	–	20	ns	
33	$\overline{HACK}$ Setup Time	$t_{su\,(HA-CL)}$	7	–	6	–	5	–	ns	
34	$\overline{ABEN}$, $\overline{AIN}$, $\overline{DBEN}$, $\overline{DIN}$ Valid Delay Time (Bus Master)	$t_{d\,(CH-AEV)\,M}$	–	30	–	27	–	22	ns	

Continued on next page

AC Characteristics (Continued)

(V_{CC} = 5 V + 5%, V_{SS} = 0 V, T_A = 0 to 70C

No.	Parameter	Symbol	20 MHz		25 MHz		33 MHz		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
35	$\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Valid Delay Time (Bus Master)	$t_{d\ (CL-AEZ)\ M}$	–	25	–	23	–	20	ns	Figure 9-6
36	$\overline{ABEN}$, $\overline{AIN}$, $\overline{DBEN}$, $\overline{DIN}$ Float Delay Time (Bus Master)	$t_{d\ (CH-ASV)\ M}$	–	30	–	25	–	20	ns	
37	$\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Float Delay Time (Bus Master)	$t_{d\ (CH-ASZ)\ M}$	–	25	–	23	–	20	ns	
38	$\overline{REQ}$ Setup Time (Burst Mode)	$t_{su\ (CL-RQ)\ B}$	7	–	6	–	5	–	ns	
39	$\overline{CS}$, $\overline{IACK}$ Setup Time	$t_{su\ (CS-CL)}$	7	–	6	–	5	–	ns	Figure 9-7
40	$\overline{ABEN}$, $\overline{AIN}$, $\overline{DBEN}$, $\overline{DIN}$ Valid Delay Time (Bus Slave)	$t_{d\ (CH-AEV)\ S}$	–	30	–	27	–	22	ns	
41	$\overline{ABEN}$, $\overline{AIN}$, $\overline{DBEN}$, $\overline{DIN}$ Float Delay Time (Bus Slave)	$t_{d\ (CH-AEZ)\ S}$	–	25	–	23	–	20	ns	
42	$\overline{ABEN}$ Delay Time (Bus Slave)	$t_{d\ (CH-AE)\ S}$	–	30	–	27	–	22	ns	
43	$\overline{AIN}$ Delay Time (Bus Slave)	$t_{d\ (CL-AI)\ S}$	–	30	–	27	–	22	ns	
44	$\overline{DBEN}$ Delay Time (Bus Slave)	$t_{d\ (CH-DE)\ S}$	–	30	–	30	30	30	ns	
45	$\overline{DBEN}$ Delay Time for $\overline{CS}$, $\overline{IACK}$ Negation	$t_{d\ (CS-DE)}$	–	35	–	27	–	22	ns	
46	Read Data Delay Time (Bus Slave)	$t_{d\ (CH-RD)\ S}$	–	30	–	27	–	22	ns	
47	Data Float Delay Time for $\overline{CS}$, $\overline{IACK}$ Negation	$t_{d\ (CS-RDZ)\ S}$	–	30	–	28	–	25	ns	
48	$\overline{DC}$ Delay Time	$t_{d\ (CH-DC)}$	–	30	–	25	–	20	ns	
49	$\overline{DC}$ Delay Time for $\overline{CS}$, $\overline{IACK}$ Negation	$t_{d\ (CH-DC)}$	–	35	–	32	–	27	ns	
50	$\overline{DC}$ High-level Width	$t_{w\ (DCH)}$	0	–	0	–	0	–	ns	
51	A23 to A29, $\overline{BC}$ Setup Time	$t_{su\ (AD-CH)\ S}$	7	–	6	–	5	–	ns	
52	R/$\overline{W}$ Setup Time	$t_{su\ (RW-CL)\ S}$	7	–	6	–	5	–	ns	
53	$\overline{DIN}$ Delay Time (Slave Bus)	$t_{d\ (CL-DI)\ S}$	–	30	–	27	–	22	ns	Figure 9–8
54	Write Data Setup Time (Bus Slave)	$t_{su\ (WD-CL)\ S}$	7	–	6	–	5	–	ns	
55	Write Data Hold Time (Bus Slave)	$t_{h\ (CL-WD)\ S}$	13	–	12	–	10	–	ns	
56	$\overline{DHREQ}$ Setup Time	$t_{su\ (DR-CL)}$	7	–	6	–	5	–	ns	Figure 9–9
57	$\overline{DHACK}$ Delay Time	$t_{d\ (CL-DA)}$	–	30	–	25	–	20	ns	
58	$\overline{PCL}$ Delay Time (Output)	$t_{d\ (CH-PC)\ O}$	–	30	–	25	–	20	ns	Figure 9–10
59	$\overline{PCL}$ Setup Time (Input)	$t_{su\ (PC-CL)\ I}$	7	–	6	–	5	–	ns	
60	$\overline{IRQ}$ Delay Time (Input)	$t_{d\ (CL-IR)}$	–	30	–	27	–	22	ns	
61	$\overline{IRQ}$ Float Delay Time	$t_{d\ (CL-IRZ)}$	–	25	–	23	–	22	ns	
62	$\overline{REQ}$ Setup Time (Cycle Steal Mode)	$t_{su\ (CL-RQ)}$	7	–	6	–	5	–	ns	Figure 9–11
63	$\overline{REQ}$ Pulse Width (Cycle Steal Mode)	$t_{w\ (RQ)\ C}$	50	–	40	–	30	–	ns	
64	$\overline{REQ}$ Valid Time for $\overline{ACK}$ Assert (Cycle Steal Mode)	$t_{v\ (AK-RQ)\ C}$	0	–	0	–	0	–	ns	

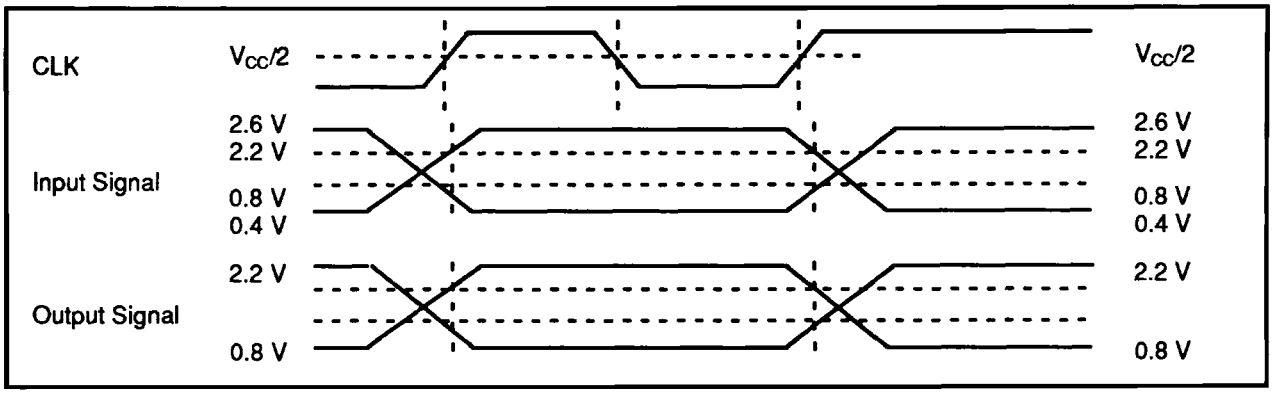

Figure 9–1. Measuring Conditions

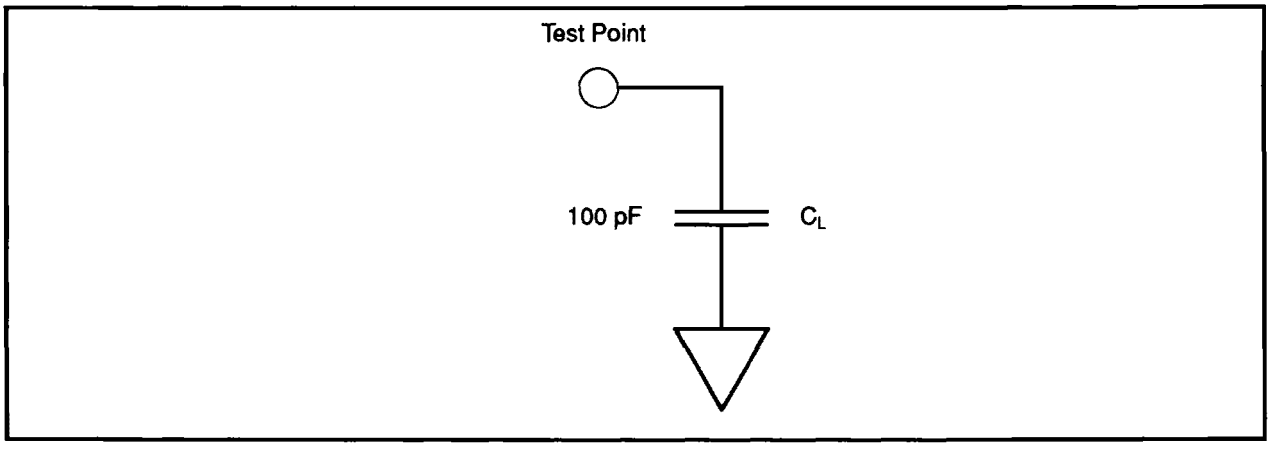

Figure 9–2. Test Load Circuit (all output pins)

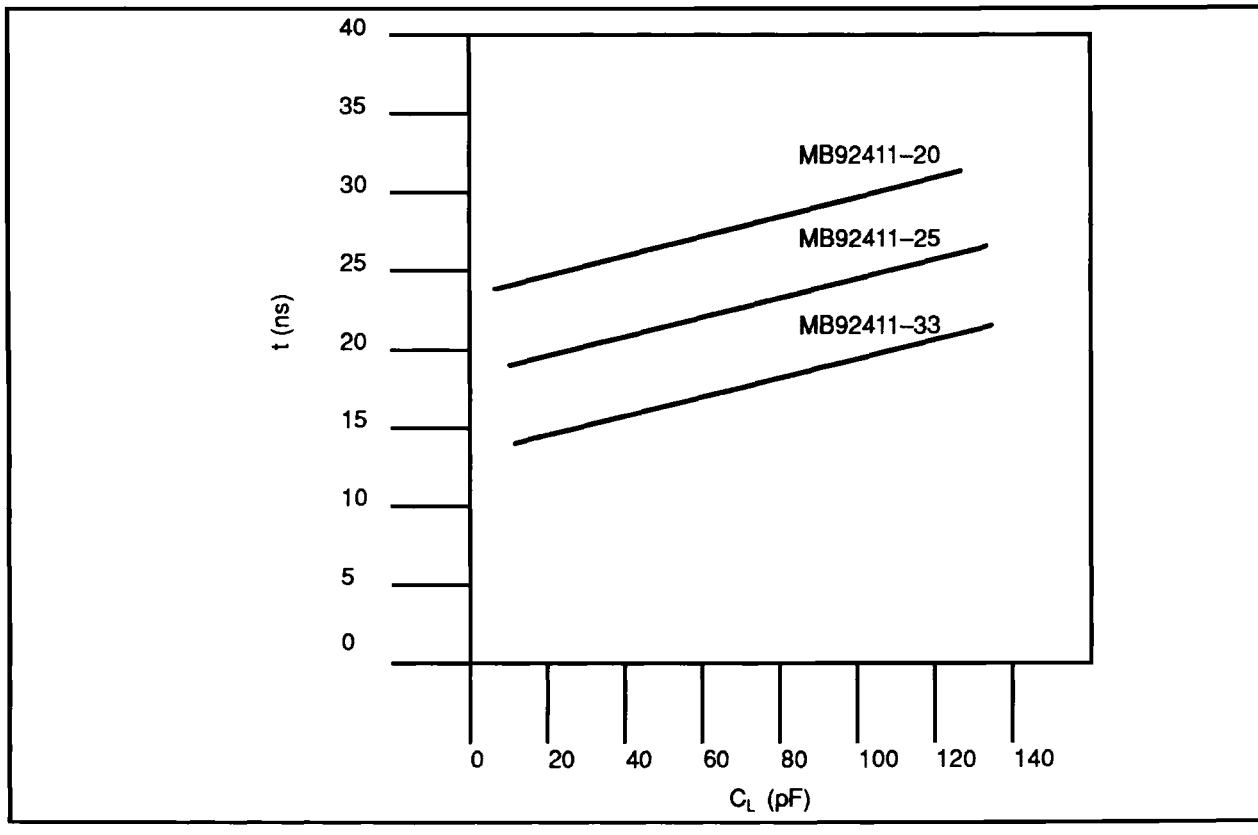

Figure 9–3. Example of Output Delay Load Capacitance for CLK Input (excluding output float delay for CLK input)

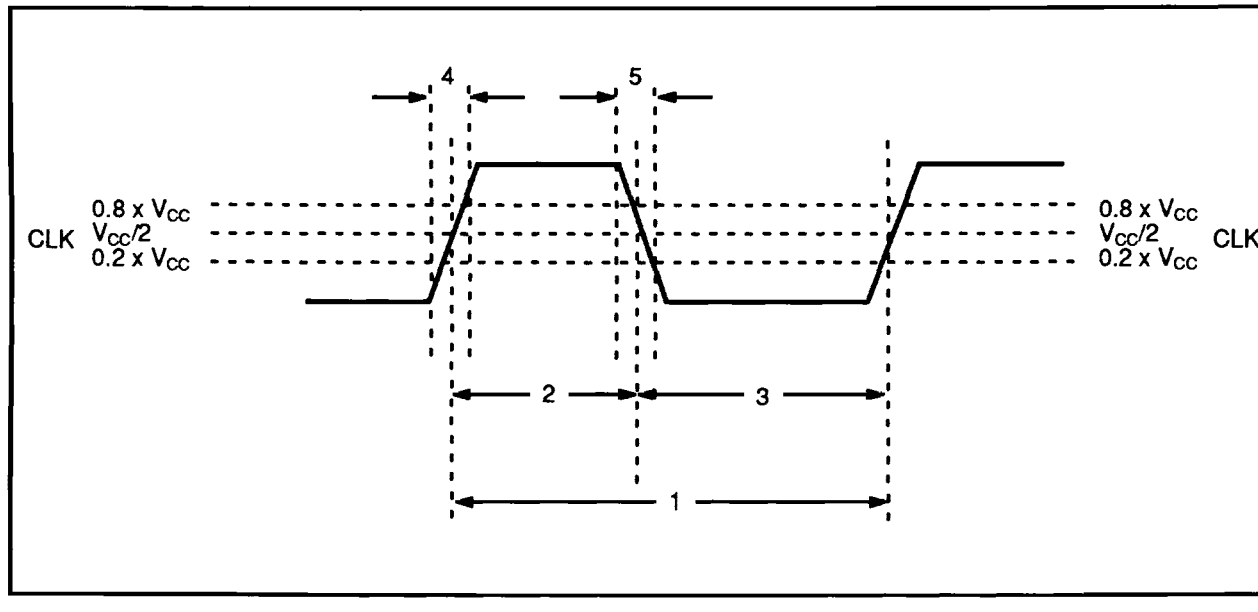

Figure 9–4. Measuring Conditions

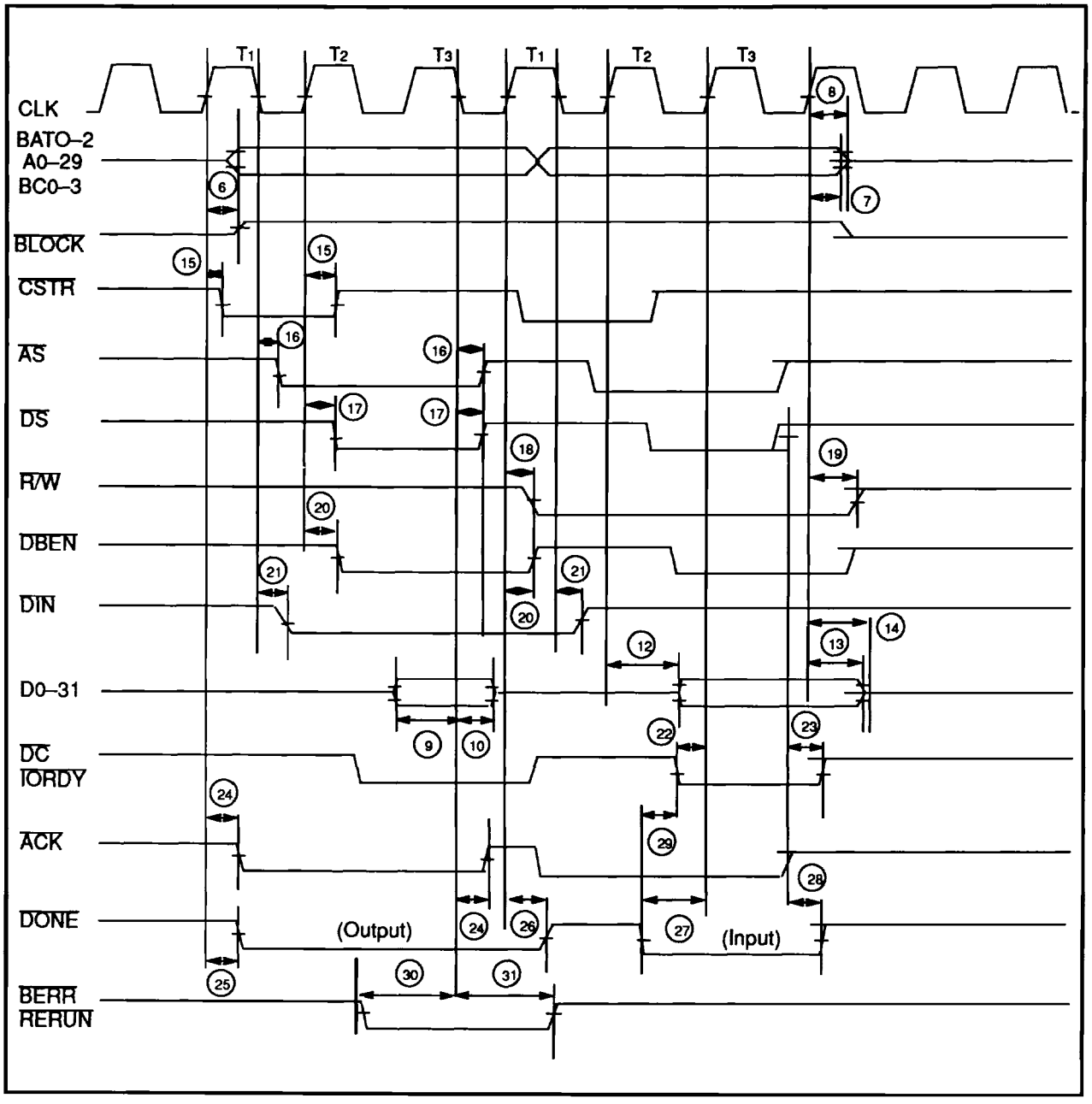

Figure 9–5. Read/Write Cycle

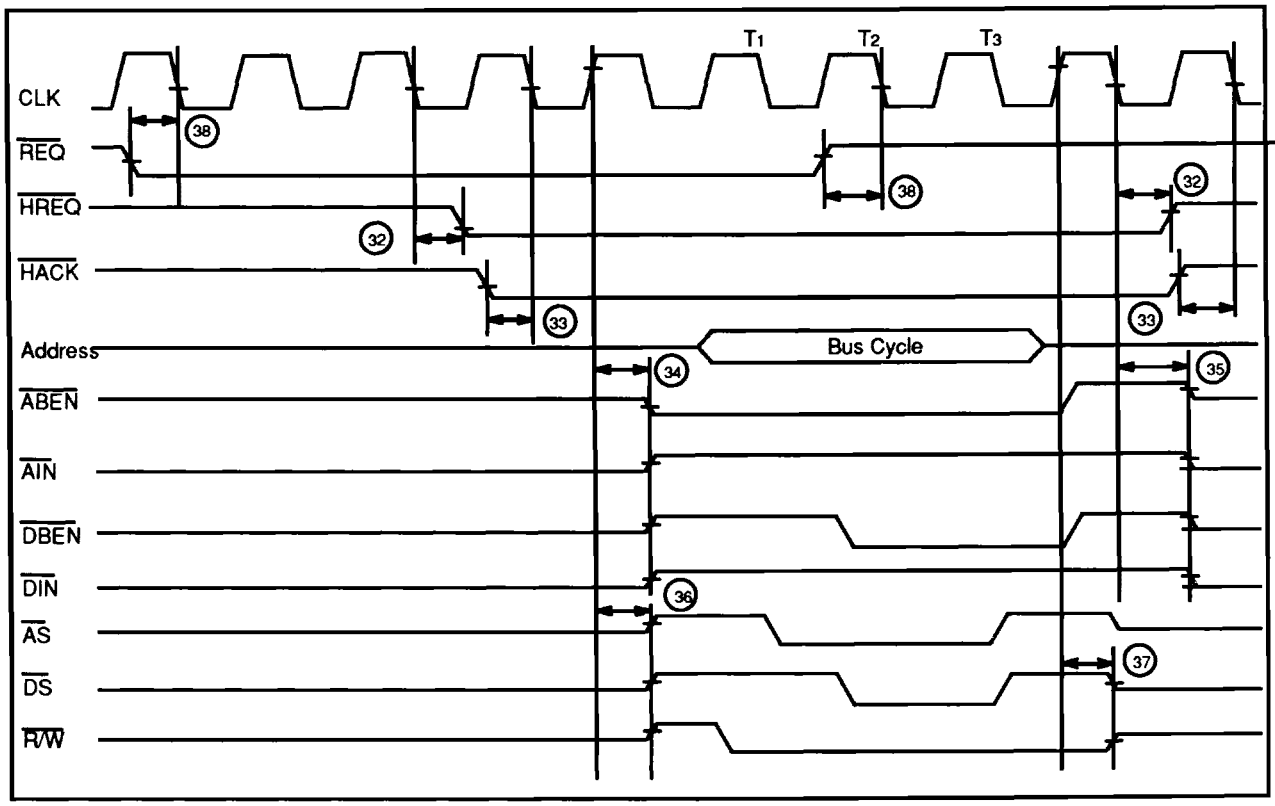

Figure 9–6. Bus Arbitration

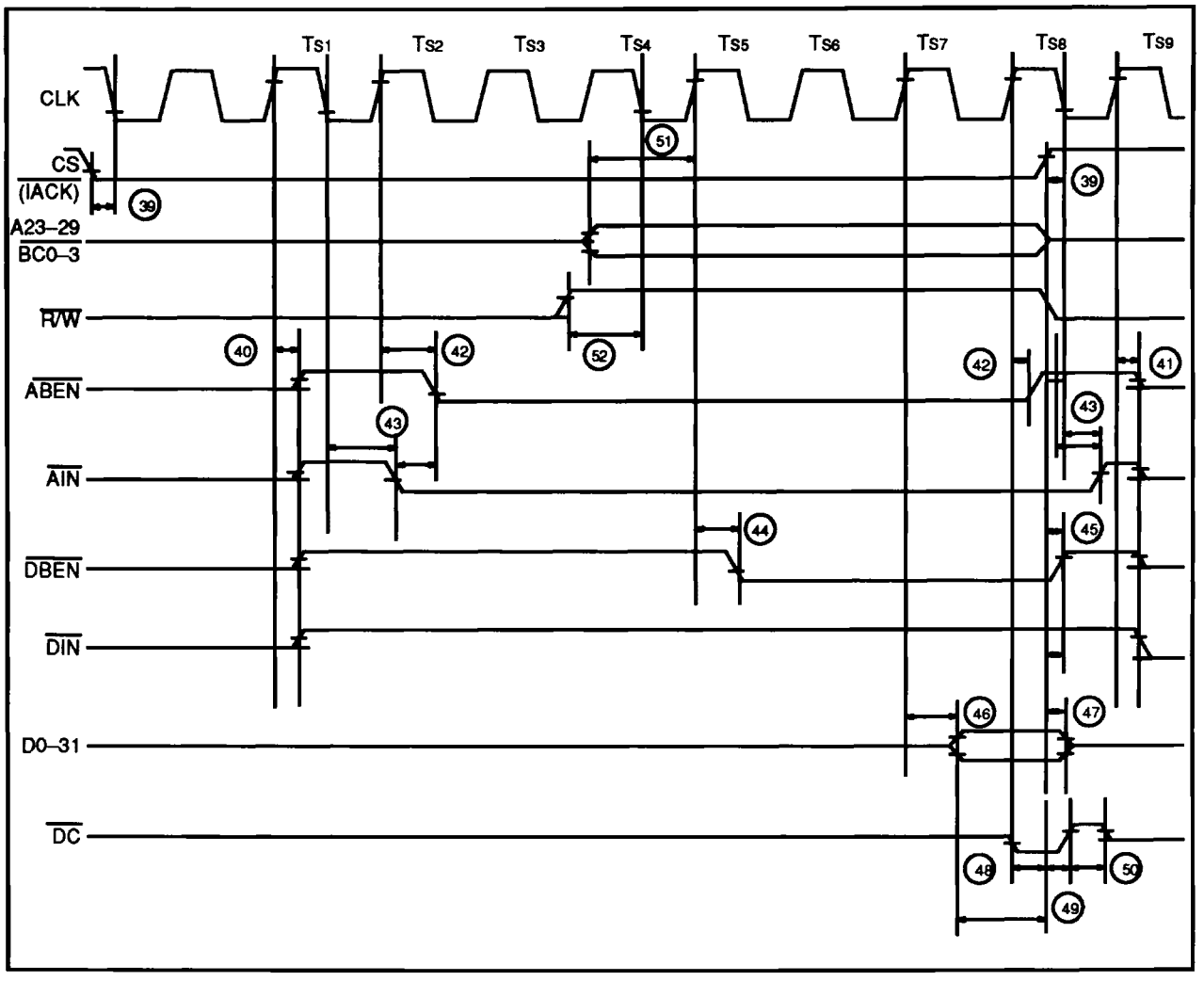

Figure 9–7. Slave Read Cycle

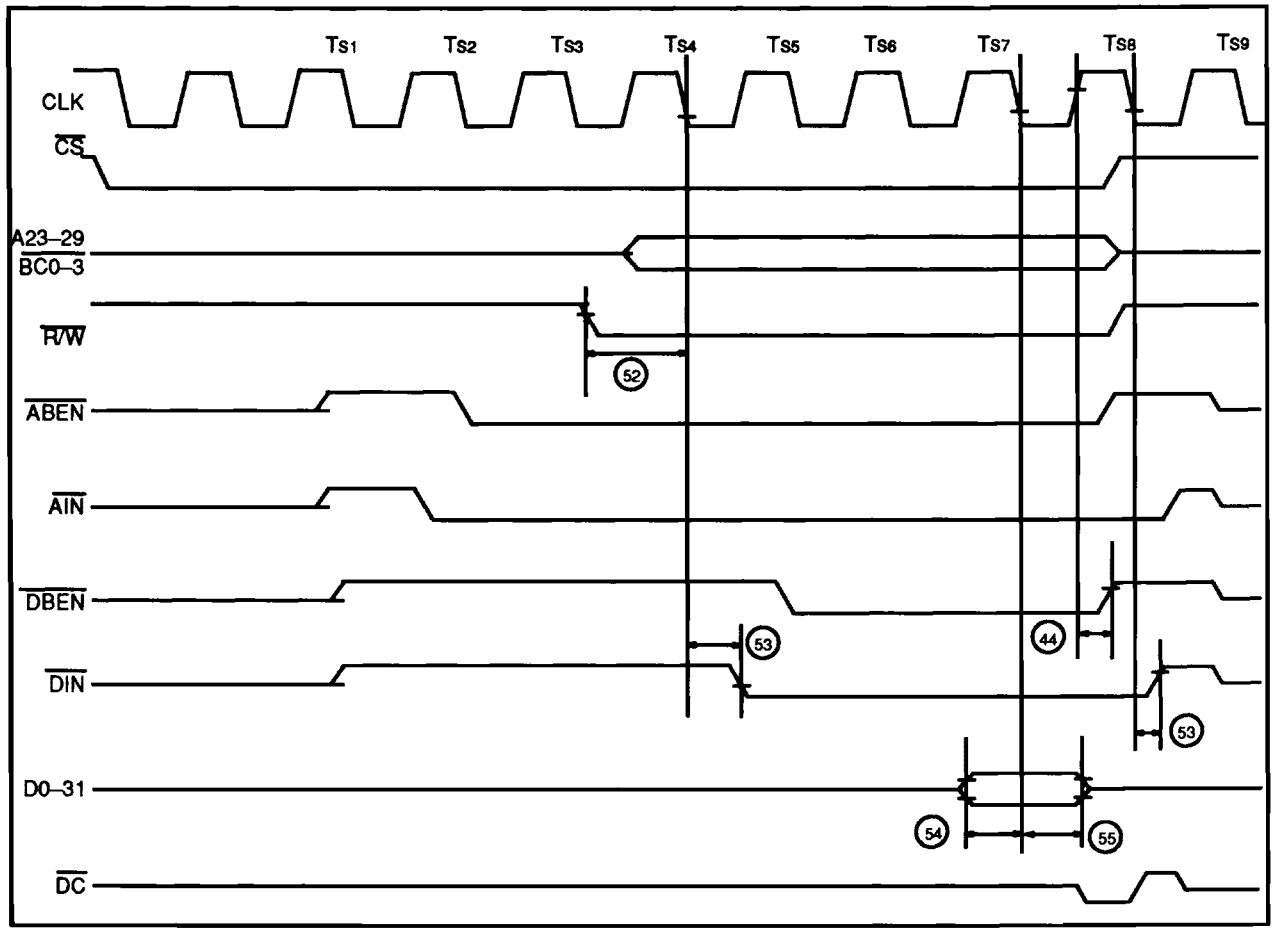

Figure 9–8. Slave Write Cycle

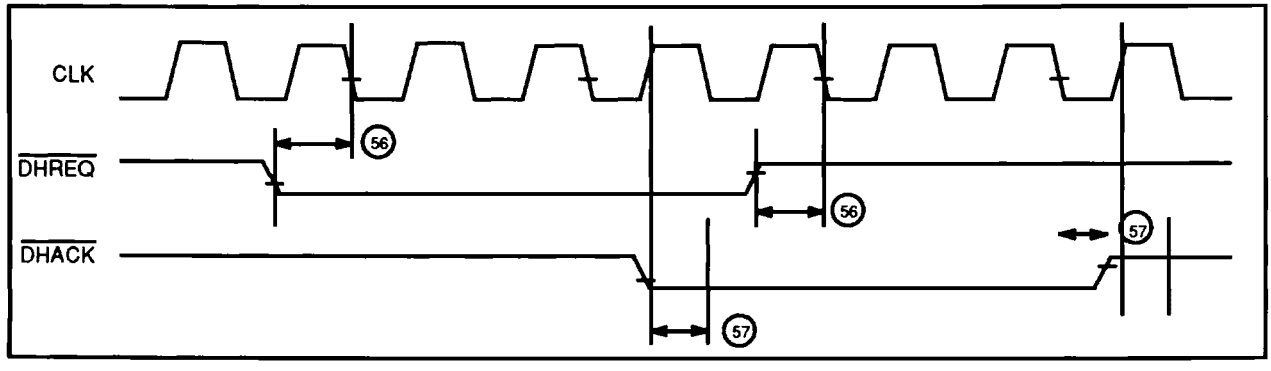

Figure 9–9. Halt Operation

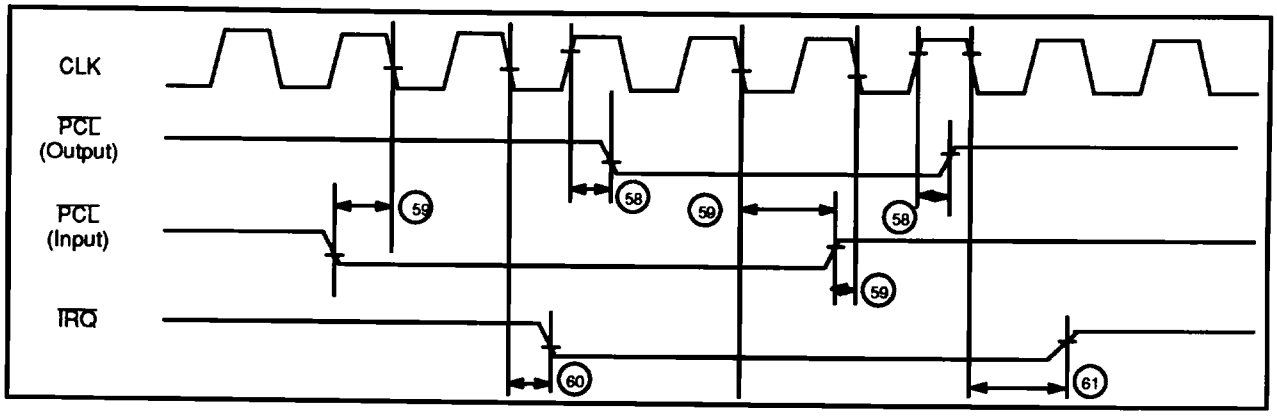

Figure 9–10. PCL and IRQ

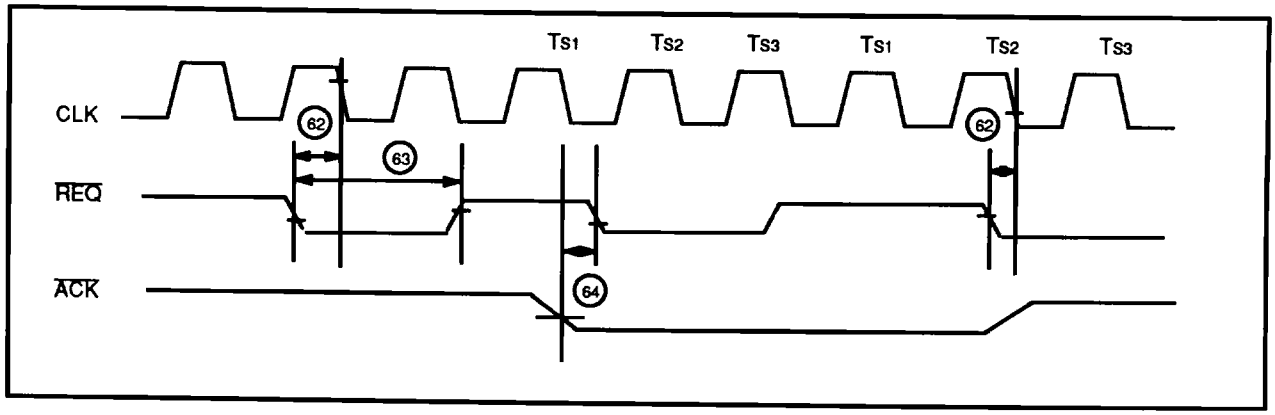

Figure 9–11. REQ # (Cycle Steal Mode)

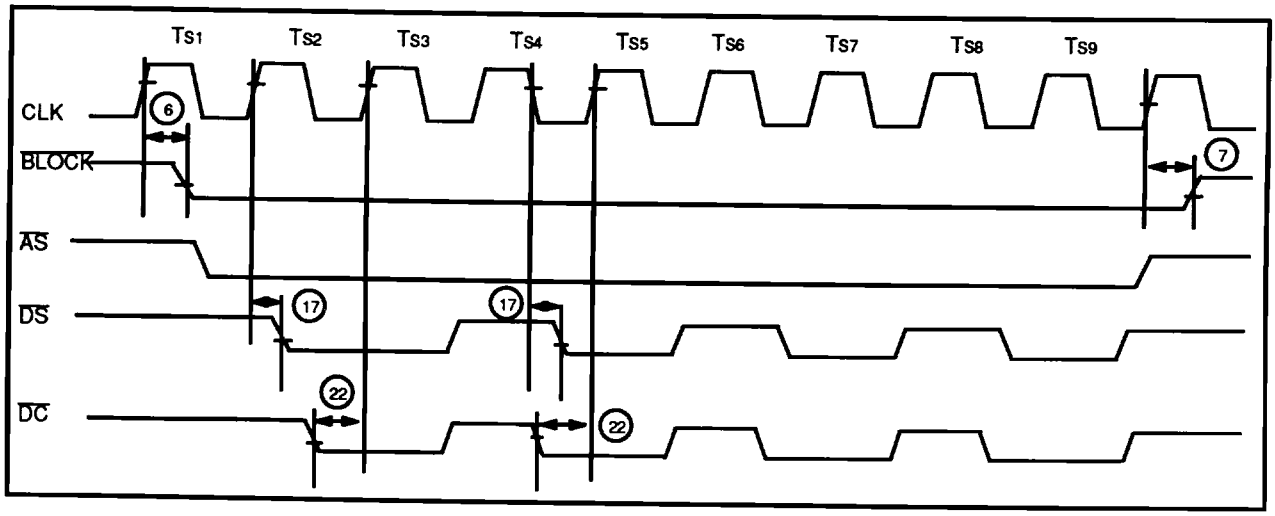

Figure 9–12. Block Transfer