

OKI semiconductor**MSC2312A-XXYS9/KS9****T-46-23-18****1,048,576 BY 9 BIT DYNAMIC RAM MODULE**

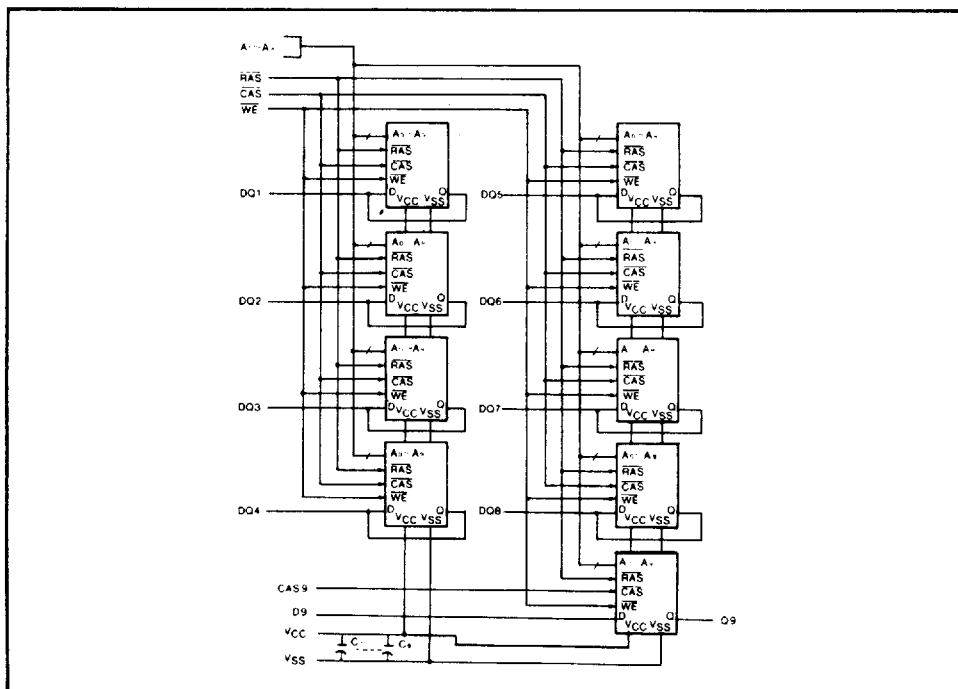
◇ K I SEMICONDUCTOR GROUP

GENERAL DESCRIPTION

The Oki MSC2312A-XXYS9/KS9 is a fully decoded, 1,048,576 words × 9 bit CMOS dynamic random access memory composed of nine 1 Mb DRAMs in SOJ (MSM511000AJS). The mounting of nine SOJs together with nine 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2312A-XXYS9/KS9 are quite same as the original MSM511000A JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

- 1,048,576 word × 9 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 8ms (512 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Separate $\overline{\text{CAS}}$ Control for One Separate Pair of Data-In and Data-Out Lines
- Access Time;
 - 80ns max. (MSC2312A-8A/80YS9/KS9)
 - 100ns max. (MSC2312A-1A/10YS9/KS9)
- Low Power Dissipation;
 - 3713mW max. (MSC2312A-8A/80YS9/KS9)
 - 3218mW max. (MSC2312A-1A/10YS9/KS9)
- Operating Temperature ... 0°C to 70°C

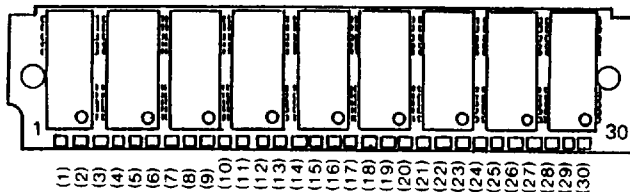
FUNCTIONAL BLOCK DIAGRAM

■ DYNAMIC RAM · MSC2312A-XXYS9/KS9 ■ — ◇ K I SEMICONDUCTOR GROUP

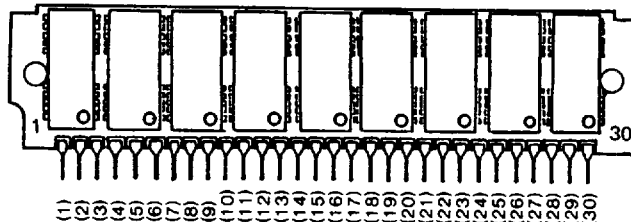
PIN ASSIGNMENT

T-46-23-18

MSC2312AYS9



MSC2312AKS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V _{CC}	11	A4	21	\overline{WE}
2	\overline{CAS}	12	A5	22	V _{SS}
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	Q9
7	A2	17	A8	27	\overline{RAS}
8	A3	18	A9	28	$\overline{CAS9}$
9	V _{SS}	19	NC	29	D9
10	DQ3	20	DQ6	30	V _{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1 to +7	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-1 to +7	V
Operating temperature	T _{opr}	0 to 70	°C
Storage temperature	T _{stg}	-55 to 150	°C
Power dissipation	P _D	9	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

T-46-23-18

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature 0°C to +70°C
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	-1.0	—	0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSC2312A-8AYS9/KS9		MSC2312A-1AYS9/KS9		MSC2312A-8OYS9/KS9		MSC2312A-1OYS9/KS9		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* Average power supply current (RAS, CAS cycling; $t_{RC} = \text{min.}$)	I_{CC1}	—	675	—	585	—	675	—	585	mA
Standby Current* Power supply current (RAS = CAS = V_{IH})	I_{CC2} (TTL)	—	18	—	18	—	18	—	18	mA
	I_{CC2} (MOS)	—	9	—	9	—	9	—	9	mA
Refresh Current 1* Average power supply current (RAS cycling, CAS = V_{IH} ; $t_{RC} = \text{min.}$)	I_{CC3}	—	675	—	585	—	675	—	585	mA
Refresh Current 2* Average power supply current (CAS before RAS; $t_{RC} = \text{min.}$)	I_{CC6}	—	675	—	585	—	675	—	585	mA
Page Mode Current* Average power supply current (RAS = V_{IL} , CAS cycling; $t_{PC} = \text{min.}$)	I_{CC7}	—	495	—	495	—	540	—	495	mA
Input Leakage Current Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, all other pins not under test = 0V)	I_{LI}	-90	90	-90	90	-90	90	-90	90	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{LO}	-10	10	-10	10	-10	10	-10	10	μA
Output Levels Output high voltage ($I_{OH} = -5mA$) Output low voltage ($I_{OL} = 4.2mA$)	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V
	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

4

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A ₀ ~ A ₉)	C _{IN1}	40	70	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	40	75	pF
Data Input/Output Capacitance (DQ)	C _{DQ}	7	20	pF
Input Capacitance ($\overline{\text{CAS9}}$)	C _{IN3}	5	10	pF
Input Capacitance (D9)	C _{IN4}	4	10	pF
Output Capacitance (Q9)	C _{OUT}	4	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Note 1, 2, 3

T-46-23-18

Parameter	Symbol	MSC2312A -8AYS9/KS9		MSC2312A -1AYS9/KS9		MSC2312A -8OYS9/KS9		MSC2312A -1OYS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t _{REF}	—	8	—	8	—	8	—	8	ms	
Random read or write cycle time	t _{RC}	160	—	190	—	160	—	190	—	ns	
Fast page mode cycle time	t _{PC}	55	—	55	—	50	—	55	—	ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}	—	80	—	100	—	80	—	100	ns	4,5,6
Access time from $\overline{\text{CAS}}$	t _{CAC}	—	25	—	30	—	20	—	25	ns	4,5
Access time from column address	t _{AA}	—	40	—	50	—	40	—	50	ns	4,6
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	50	—	50	—	45	—	50	ns	4
Output low impedance time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	0	—	n _s	4
Output buffer turn-off delay	t _{OFF}	0	20	0	20	0	20	0	20	ns	
Transition time	t _T	3	50	3	50	3	50	3	50	ns	3
$\overline{\text{RAS}}$ precharge time	t _{RP}	70	—	80	—	70	—	80	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode cycle only)	t _{RASP}	80	100000	100	100000	80	100000	100	100000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	25	—	30	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ precharge time (Fast page mode cycle only)	t _{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	25	10000	30	10000	20	10000	25	10000	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	80	—	100	—	80	—	100	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	22	55	25	70	25	60	25	75	ns	5
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	20	40	20	50	17	40	20	50	ns	6
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10	—	10	—	10	—	10	—	ns	
Row address set-up time	t _{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t _{RAH}	15	—	15	—	12	—	15	—	ns	
Column address set-up time	t _{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	15	—	20	—	15	—	20	—	ns	
Column address hold time from $\overline{\text{RAS}}$	t _{AR}	60	—	75	—	60	—	75	—	ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	40	—	50	—	40	—	50	—	ns	

■ DYNAMIC RAM • MSC2312A-XXYS9/KS9 ■

O K I SEMICONDUCTOR GROUP

AC CHARACTERISTICS (CONT.)

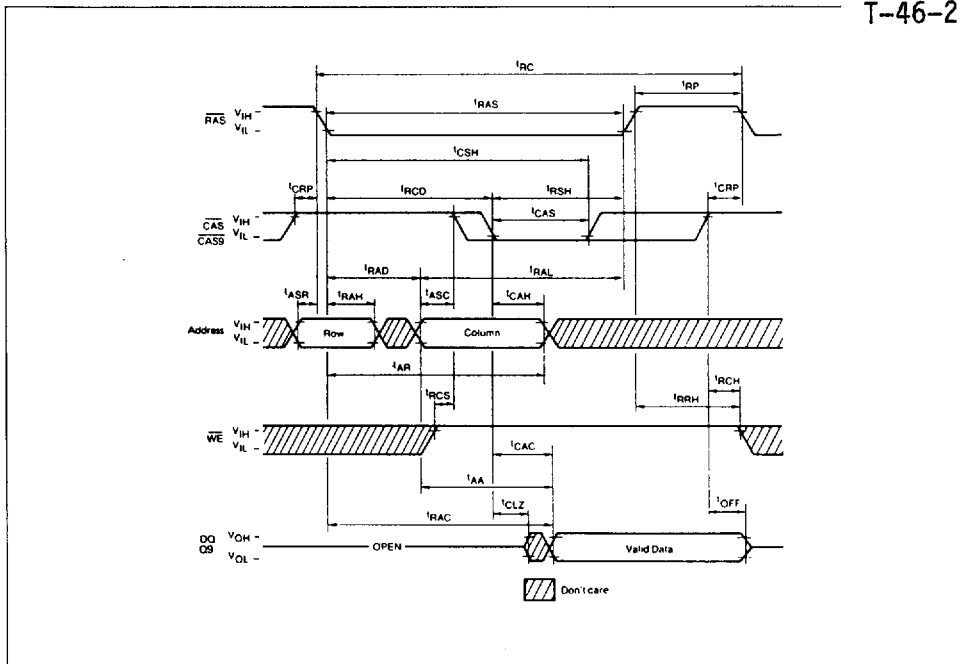
T-46-23-18

Parameter	Symbol	MSC2312A -8AYS9/KS9		MSC2312A -1AYS9/KS9		MSC2312A -80YS9/KS9		MSC2312A -10YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	7
Write command hold time from \overline{RAS}	t_{WCR}	60	—	75	—	60	—	75	—	ns	
Write command set-up time	t_{WCS}	0	—	0	—	0	—	0	—	ns	
Write command hold time	t_{WCH}	15	—	20	—	15	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	15	—	20	—	ns	
Data-in set-up time	t_{DS}	0	—	0	—	0	—	0	—	ns	
Data-in hold time	t_{DH}	15	—	20	—	15	—	20	—	ns	
Data-in hold time from \overline{RAS}	t_{DHR}	60	—	75	—	60	—	75	—	ns	
Read command hold time reference to \overline{RAS}	t_{RRH}	10	—	10	—	10	—	10	—	ns	7
\overline{RAS} to \overline{CAS} set-up time (CAS before \overline{RAS})	t_{CSR}	10	—	10	—	10	—	10	—	ns	
\overline{RAS} to \overline{CAS} hold time (CAS before \overline{RAS})	t_{CHR}	30	—	30	—	30	—	30	—	ns	
\overline{CAS} active delay from \overline{RAS} precharge	t_{RPC}	10	—	10	—	10	—	10	—	ns	
\overline{CAS} precharge time	t_{CPN}	10	—	15	—	10	—	15	—	ns	

- Notes:**
- 1 An initial pause of 100 μ s is required after power-up followed by any 8 \overline{RAS} cycles (Example: \overline{RAS} only) before proper device operation is achieved.
 - 2 The AC characteristics assume at $t_T = 5$ ns.
 - 3 V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 - 4 Measured with a load circuit equivalent to 2TTL + 100 pF.
 - 5 Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC} .
 - 6 Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA} .
 - 7 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

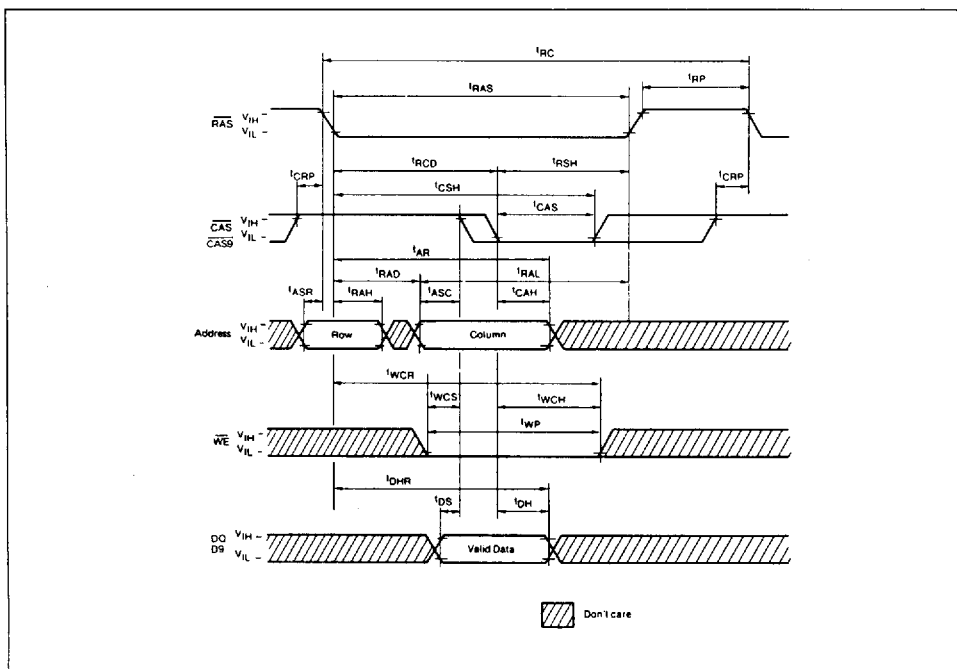
READ CYCLE

T-46-23-18

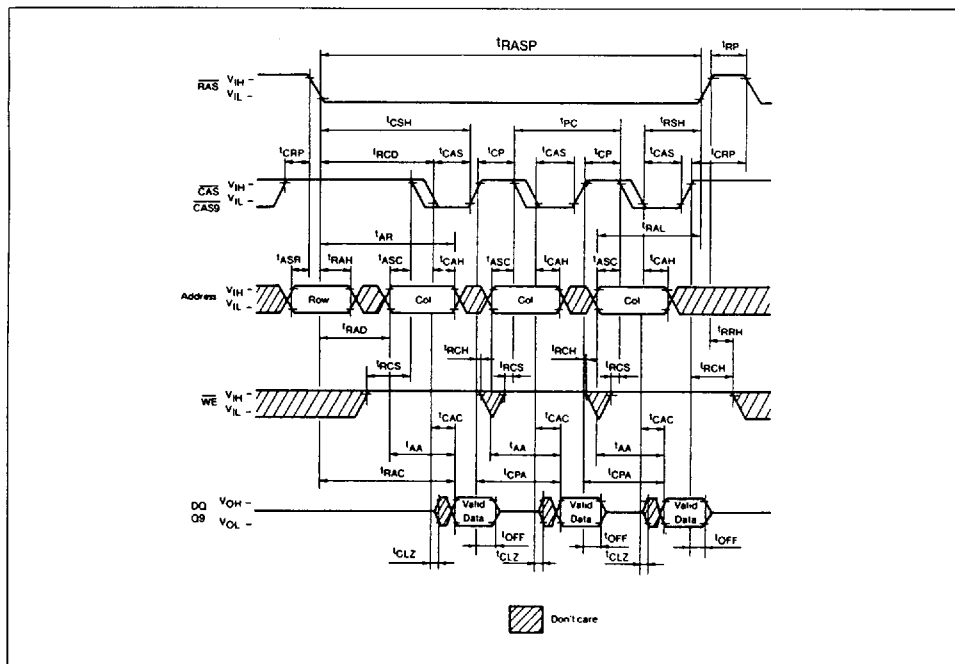


4

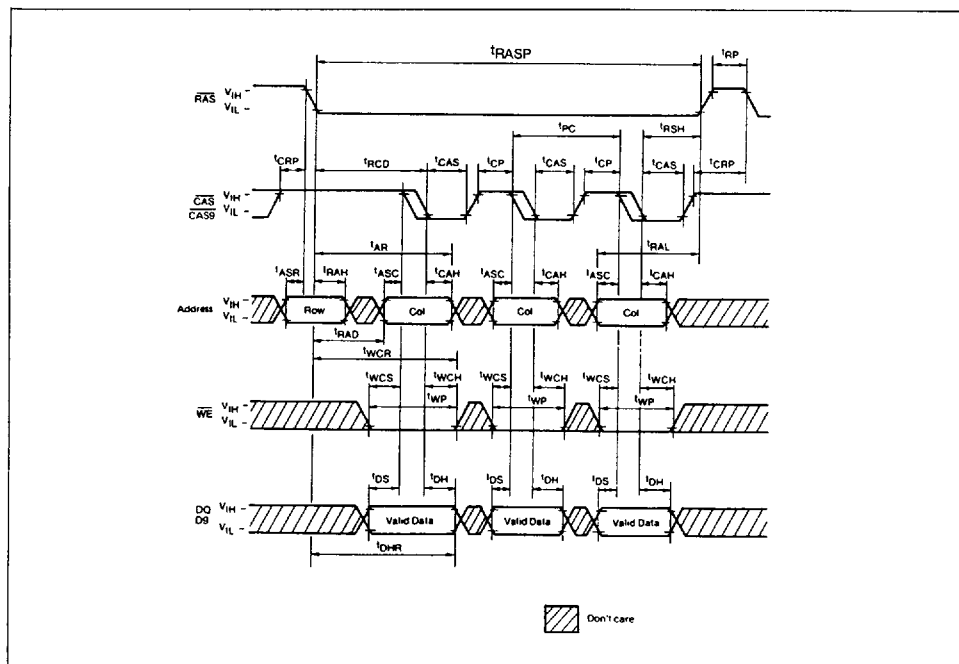
WRITE CYCLE(EARLY WRITE)



FAST PAGE MODE READ CYCLE

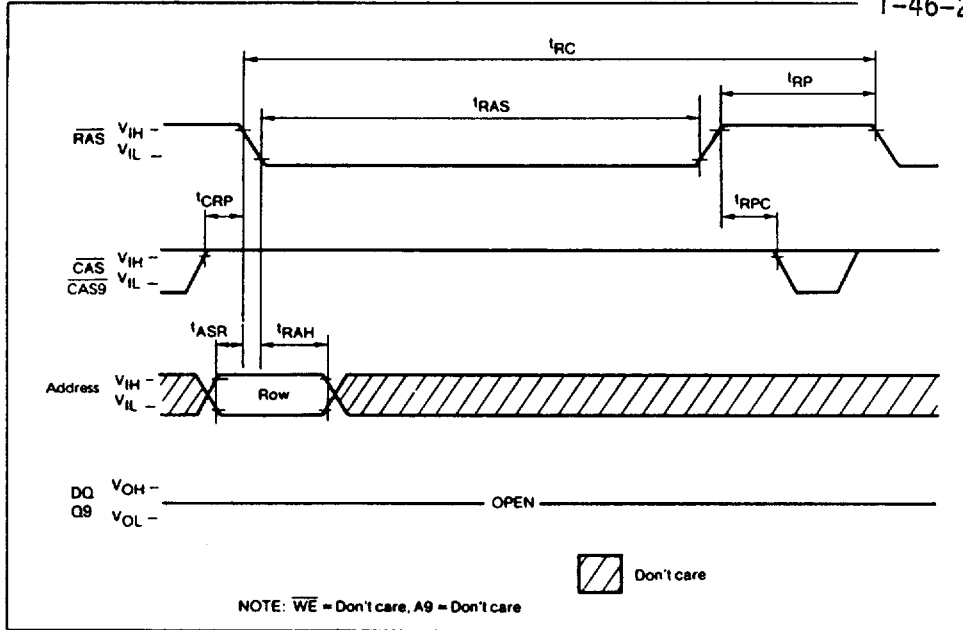


FAST PAGE MODE CYCLE (EARLY WRITE)



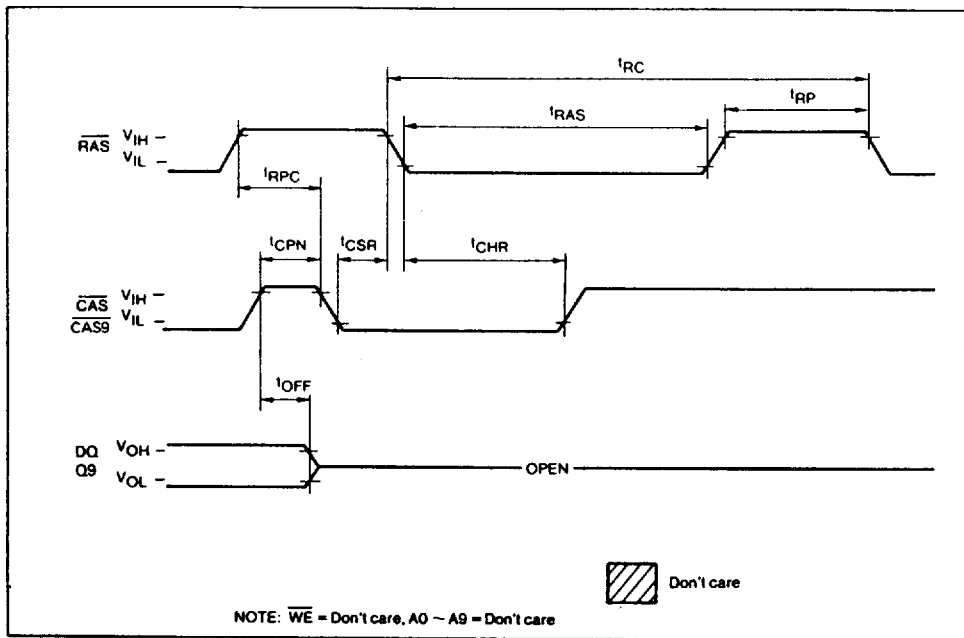
RAS ONLY REFRESH CYCLE

T-46-23-18



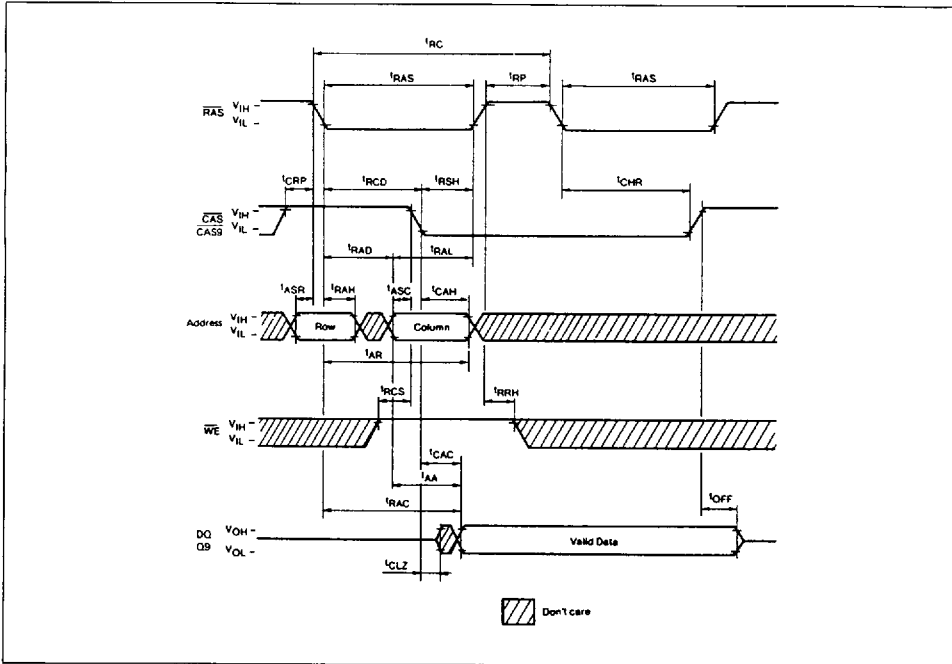
4

CAS BEFORE RAS AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE

T-46-23-18



HIDDEN REFRESH WRITE CYCLE

