Preliminary

Specifications in this data sheet are based on design expectations and on measurements from a limited number of engineering samples. Please contact your local Micro Networks Representative for additional information.

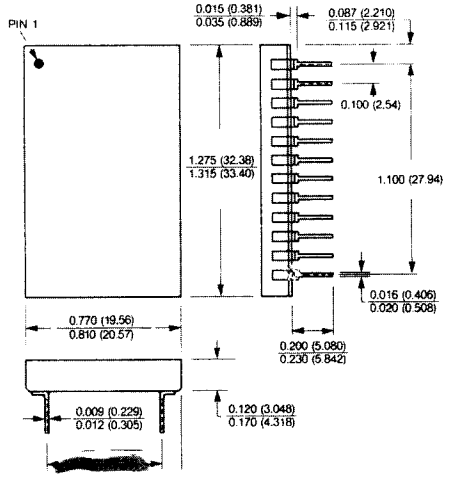
MN050

HIGH-SPEED
TRACK-HOLD
AMPLIFIER

FEATURES

- **120nsec Max Acquisition Time (5V Step to ±0.1%)**
- **±0.01% Max Linearity Error**
- **100psec Max Aperture Jitter**
- **Pin-Programmable Input Buffer Amplifier**
- **20MHz Small Signal Bandwidth**
- **±10μV/μsec Max Droop Rate**
- **ADH-050 Pin and Function Compatible**
- **MIL-STD-883 Screening (Method 5008) Optional**

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN050 is a very high-speed, 12-bit linear, track-hold (sample-hold) amplifier in a small, 24-pin, ceramic DIP. It features fast acquisition time (120nsec max for a 5V step acquired to ±0.1%), wide bandwidth (20MHz typical small-signal bandwidth), low aperture jitter (100psec maximum), and an internal, user-optional, pin-programmable, input buffer amplifier that can be configured as a follower ($G = +1$; input impedance $> 10^7\Omega$), as a differential amplifier ($G = \pm 2, \pm \frac{1}{2}$; differential input impedance = $2k\Omega$), or as a single-ended amplifier ($G = \pm 2, \pm \frac{1}{2}$).

The MN050 has a ±5V input/output range, and its track-hold control line is ECL compatible (logic "1" (track mode) = −0.8V min, logic "0" (hold mode) = −1.8V max). In order to achieve 12-bit (±0.01%FSR) linearity, the MN050 employs a "closed-loop" (feedback) design approach that gives it a gain of −1 (without the input buffer) and a constant pedestal (typically 5mV) that does not vary as a function of input signal level. Feedthrough attenuation in the hold mode is typically 80dB. Output droop rate is typically ±0.1μV/μsec.

The MN050 is pin compatible with the ADH-050 but offers considerable performance improvements in the areas of input-output voltage range, input impedance, track-mode offset, pedestal, aperture jitter (100psec vs. 500 psec), droop rate and power consumption.

The MN050's throughput has been optimized for 10-12 bit applications. For high-speed 12-13 bit applications, the MN376 and MN377 fully specify acquisition time (200nsec and 100nsec respectively) and track-to-hold settling time to ±0.01% accuracy.

The MN050 is available fully specified for either 0°C to 70°C (case) or −55°C to +125°C (case) operation. For military/aerospace applications, the MN050H/B is fully screened to MIL-STD-883, Method 5008.

MN050

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MN050 HIGH-SPEED TRACK-HOLD AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C (case)
Specified Temperature Range:	
MN050	0°C to +70°C (case)
MN050H, MN050H/B	−55°C to +125°C (case)
Storage Temperature Range	−65°C to +150°C
+15V Supply (+Vcc, Pin 12)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 9)	+0.5 to −18 Volts
−5.2V Supply (−Vdd, Pin 5)	+0.5 to −7 Volts
−1.3V Reference (−Vbb, Pin 8)	+0.5 to −3 Volts
Direct Analog Input Voltage (Pin 24)	±15 Volts
Buffer Input Voltage (Pins 19, 21, 22, 23)	±15 Volts
Digital Input Voltage (Pin 3)	+0.5 to −7 Volts

ORDERING INFORMATION

PART NUMBER — **MN050H/B**

Standard device is specified for 0°C to +70°C (case) operation. Add "H" suffix for specified −55°C to +125°C (case) operation.

Add "/B" for 100% screening according to Method 5008 of MIL-STD-883.

SPECIFICATIONS (T_A = +25°C, $\pm V_{cc}$ = ±15V, $-V_{dd}$ = −5.2V and $-V_{bb}$ = −1.3V unless otherwise indicated).

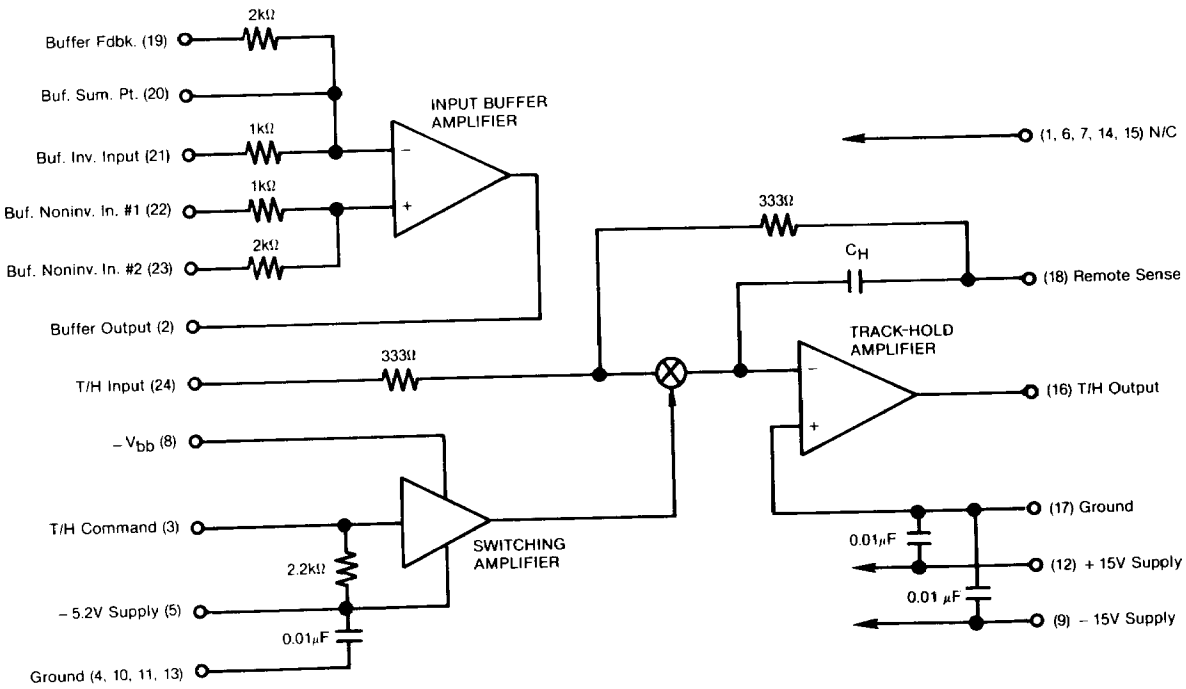
	MIN.	TYP.	MAX.	UNITS
ANALOG INPUTS				
Without Buffer: Input Voltage Range	±5	±6		Volts
Input Resistance		333		Ω
Input Capacitance			15	pF
With Buffer as Follower: Input Impedance	10^7			Ω
Input Bias Current		±100	±250	nA
Output Voltage Range	±5			Volts
With Buffer as Differential Amplifier:				
Input Voltage Range	±2.5			Volts
Common Mode Range		±10		Volts
Differential Input Impedance		2000 // 15		Ω // pF
With Buffer as Single-Ended Amplifier:				
Input Voltage Range (Gain = ±2)	±2.5			Volts
Input Voltage Range (Gain = ±½)	±10			Volts
Input Impedance (Gain = −2)		1000 // 15		Ω // pF
ANALOG OUTPUT				
Output Voltage Range	±5			Volts
Output Current: Buffer Amplifier	±15			mA
T/H Amplifier	±10			mA
Output Impedance (T/H Amplifier)		0.02	0.1	Ω
Maximum Capacitive Load (T/H Amplifier)		50		pF
DIGITAL INPUTS				
Logic Levels: Logic "1" (Track Mode)	−0.8			Volts
Logic "0" (Hold Mode)			−1.8	Volts
Logic Loading: Logic "1" (−0.8 Volts)		−2.0		mA
Logic "0" (−1.8 Volts)		−1.5		mA
TRANSFER CHARACTERISTICS (Note 2)				
Gain: Buffer (Pin-programmable)		+1, ±½, ±2		V/V
T/H Amplifier		−1		V/V
Gain Accuracy (Note 3): Initial (+25°C)		±0.05	±0.1	%
Drift		±2	±5	ppm/°C
Gain Linearity Error: T/H Amplifier (−55°C to +110°C)		±0.002	±0.01	%FSR
Buffer Amplifier Initial (+25°C)		±0.002		%FSR
Buffer Amplifier Drift		±1	±2	ppm of FSR/°C
T/H Amplifier Output Offset (Track Mode): Initial (+25°C)		±3	±10	mA
Drift		±50	±120	µV/°C
Buffer Amplifier Offset (RTI): Initial (+25°C)		±1	±3	mV
Dirft		±20	±50	µV/°C
T/H Pedestal: Initial (+25°C)		±5	±20	mV
Drift		±10	±25	µV/°C

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Acquisition Time: 5V Step to ±0.1% (±5mV)		100	120	nsec
2V Step to ±0.1% (±2mV)		90	100	nsec
Track-to-Hold Transient: Height (Peak-to-Peak)		200		mV
Settling Time (to ±2mV)			100	nsec
Settling Time (Step Response) to ±2mV:				
Buffer Amplifier			500	nsec
T/H Amplifier in Track Mode		70	100	nsec
Aperture Delay Time			5	nsec
Aperture Jitter			100	psec
Small Signal Bandwidth:				
Buffer Amplifier (Follower)		5		MHz
T/H Amplifier in Track Mode		20		MHz
Output Slew Rate: Buffer Amplifier		60		V/μsec
T/H Amplifier		200		V/μsec
Feedthrough Attenuation (Hold Mode, ±2.5V 10kHz Input)	60	80		dB
Droop Rate: Initial (+25°C)		±0.1	±10	μV/μsec
Over Temperature		(Note 4)		
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±15V Supplies	±14.25	±15	±15.75	Volts
−5.2V Supply	−5.5	−5.2	−4.9	Volts
Power Supply Rejection (±15V Supplies): Buffer Amplifier		±0.1		mV/V
T/H Amplifier		±1	±5	mV/V
Current Drains: +15V Supply		45	60	mA
−15V Supply		45	60	mA
−5.2V Supply		15	25	mA
−1.3V Supply		1.8	2.5	mA
Power Consumption		1400	1900	mW

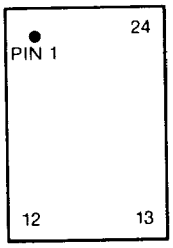
SPECIFICATION NOTES:

1. The MN050 buffer and T/H amplifiers are output short circuit protected to ground for approximately 1 minute. Shorts to either supply will result in destruction. Under normal operating conditions, output currents should not exceed guaranteed minimums.
2. FSR stands for Full Scale Range and is equivalent to 10 Volts for the MN050.
3. Specifications apply for either the input-buffer or T/H amplifier.
4. Doubles every 10°C.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	N/C	24	T/H Input
2	Buffer Output	23	Buffer Noninverting Input #2
3	T/H Command	22	Buffer Noninverting Input #1
4	Ground	21	Buffer Inverting Input
5	−5.2V Supply	20	Buffer Summing Point
6	N/C	19	Buffer Feedback
7	N/C	18	T/H Remote Sense (FDBK)
8	$-V_{bb}$	17	Ground
9	−15V Supply	16	T/H Output
10	Ground	15	N/C
11	Ground	14	N/C
12	+15V Supply	13	Ground

APPLICATIONS INFORMATION

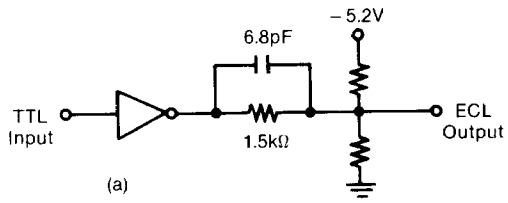
DESCRIPTION OF OPERATION—The MN050 consists of a track-hold (sample-hold) amplifier and an independent, user-optional, pin-programmable input buffer amplifier in a single package. The track-hold amplifier (T/H) has a gain of −1 and an ECL compatible track-hold command line. The buffer amplifier may be bypassed (the T/H has a direct input resistance of 333Ω) or configured as a follower, a differential amplifier, or a single-ended amplifier.

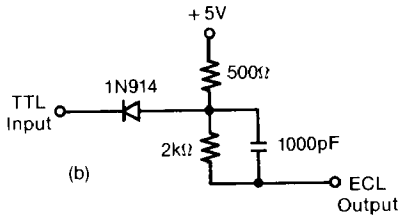
With an ECL logic "1" (−0.8V minimum) applied to pin 3 (T/H Command), the MN050 will be in the tracking (signal acquisition) mode, and its output will track its input. In this mode, the MN050 operates as an inverting, gain of 1 amplifier and gain accuracy, gain linearity, track-mode offset, slew rate and small signal bandwidth specifications apply. The application of an ECL logic "0" (−1.8V maximum) to pin 3 drives the MN050 into the hold mode holding the output voltage constant at the value that existed when the hold command was applied. In the hold mode, output droop rate and feedthrough attenuation specifications apply. Application of a logic "1" at this point drives the MN050 back into the tracking (sampling) mode. Acquisition time refers to the time it takes the output of the T/H, at this point, to catch up to its new input and settle to within some specified accuracy of the input.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified performance from the MN050. The unit's 4 Digital Ground pins (pins 4, 10, 11 and 13) and its single Analog Ground pin (pin 17) must all be tied to system ground lines. If your system employs separate analog and digital ground returns, the MN050's digital ground pins should be connected to system digital ground and its analog ground pin should be connected to system analog ground, preferably through a large analog ground plane beneath the package. If your system does not have separate digital and analog grounds, all five of the MN050's ground pins should be tied together as close to the unit as possible and all connected to analog ground. Again, the preferred connection is a large ground plane beneath the package.

Power supply connections should be short and direct. The MN050 contains internal 0.01μF ceramic bypass capacitors on each supply line. In critical applications, additional external 0.1μF to 1μF tantalum bypass capacitors may be required.

TRACK-HOLD COMMAND INPUT—An ECL logic "1" (−0.8V minimum) applied to pin 3 puts the MN050 into the track mode; an ECL logic "0" (−1.8V maximum) puts the MN050 into the hold mode. To ensure correct operation, the −1.3V (−Vbb) applied to pin 8 should come from the same −5.2V ($-V_{dd}$) logic supply driving the MN050. Some ECL circuits, such as the 10115 differential line receiver, provide their own V_{bb} reference generator, and this can be used as the $-V_{bb}$ reference for the MN050. If control signals are TTL compatible, a TTL to ECL translator (10124) must be used or an appropriate translator circuit devised as shown below. Circuit B below consumes less power than Circuit A but also requires a +5V supply.





INPUT BUFFER AMPLIFIER—The user-optional input buffer amplifier may be configured in a number of ways as shown in the following diagrams. The follower configuration (G = +1) provides an input impedance greater than 10MΩ and an input bias current guaranteed not to exceed ±250nA. This configuration is useful in high-speed, multiplexed, data acquisition applications.

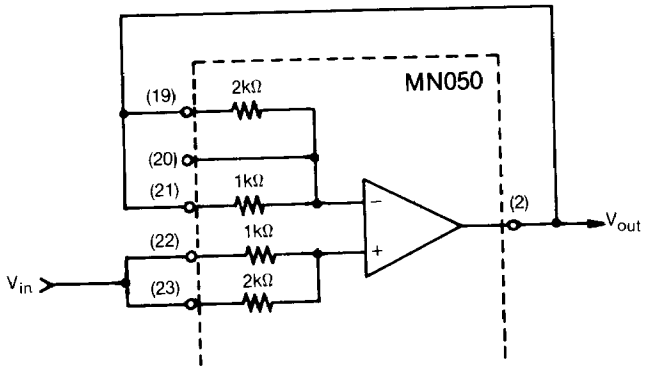


Figure 1. Buffer amplifier connected as follower. $V_{in} = \pm 5V$, $G = +1$, $Z_{in} > 10^7\Omega$.

In the differential amplifier mode, gain can be set to 2 (shown in the diagram) with a differential input impedance of 2kΩ or reduced to ½ (with a differential input impedance of 4kΩ) by interchanging pins 19 and 21. In this configuration, the common mode voltage range is ± 10V and CMRR is XXdB.

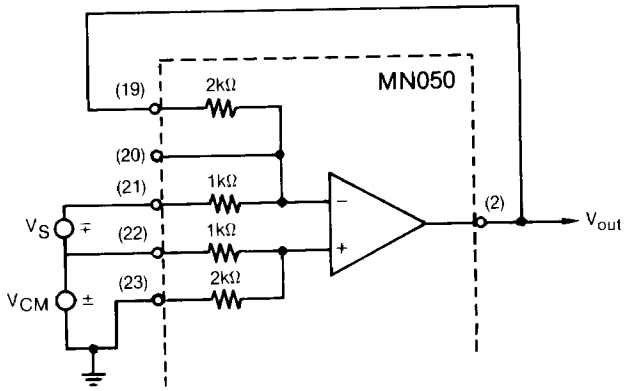


Figure 2. Buffer amplifier connected as differential amplifier. $V_S = \pm 2.5V$, $V_{CM} = \pm 10V$, $G = 2$, differential input impedance = 2kΩ.

In the single-ended amplifier mode, gain can be +2, −2, + ½ or − ½, depending on configuration. The diagram shows gains of + 2 (input applied to pin 22, pin 21 grounded, input resistance = 3kΩ) and − 2 (input applied to pin 21, pin 22 grounded, input resistance = 1kΩ). By interchanging pins 19 and 21 or pins 22 and 23, gains of + ½ and − ½ are achieved.

The versatile pinout of the MN050's internal buffer makes numerous configurations, other than those just discussed, possible. If external gain-setting resistors are used, they should be metal-film types with absolute T.C.'s less than 100ppm/°C, and the user should realize that tracking mismatches between internal and external resistors will increase gain drift with temperature. The thin-film resistors internal to the MN050 have excellent tracking characteristics and will typically keep buffer-amplifier gain drift below ± 2ppm/°C.

If necessary, a buffer-amplifier feedback capacitor may be connected between pins 19 and 20 or 2 and 20. This will reduce the bandwidth of the buffer and may be useful in reducing the input analog signal noise level. If the buffer is used to drive loads other than the MN050's internal T/H, this capacitor may be necessary for stability.

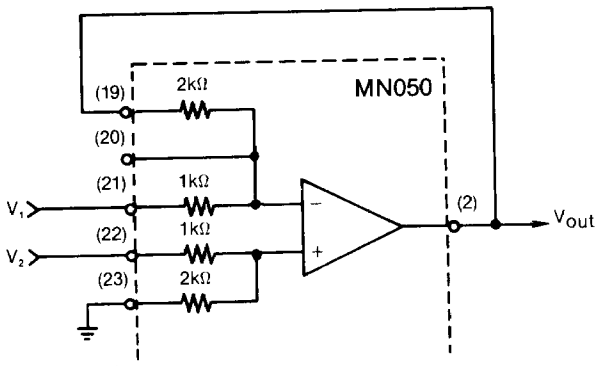


Figure 3. Buffer amplifier connected as single ended amplifier. V_1 or $V_2 = \pm 2.5V$, $V_{out}/V_1 = -2$, $V_{out}/V_2 = +2$, pin 21 impedance = 1kΩ, pin 22 impedance = 3kΩ.

ANALOG AND REMOTE SENSE—As shown in the block diagram, the MN050's output feedback loop has been left open, and in normal operation, pin 18 (Remote Sense) should be connected to pin 16 (Output). In applications in which the MN050's load is remotely located, the remote sense output can be tied directly to the load to eliminate the effects of unwanted series resistance in the output line. Care should be taken not to extend the remote sense connection for more than 2 inches or a loss of speed and/or an instability may result.

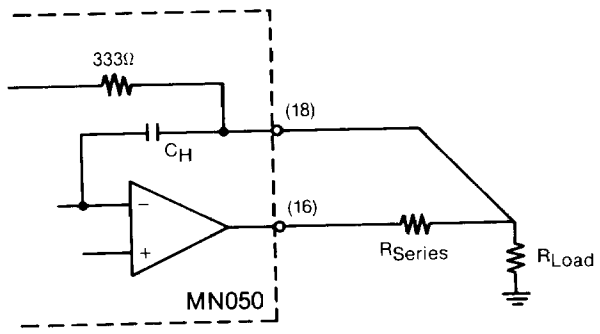


Figure 4. The Remote Sense output can be used to reduce the effect of unwanted series resistance in the output connection.