

### DESCRIPTION

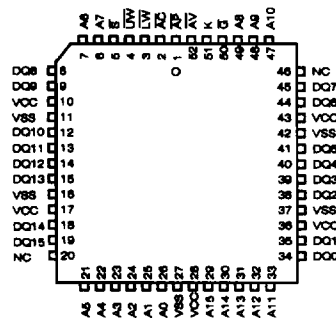
This device integrates high-speed 64Kx16 SRAM core, address registers, data input registers, a 2-bit burst address counter and pipelined output. All synchronous inputs pass through registers controlled by a positive-edge triggered clock(K).

The device is ideally suited for 486/Pentium system by including all necessary timing and control logic on a chip. Any external address latches, counters, or other timing and control logic are not necessary.

### FEATURES

- Single 5V±5% power supply
- 6ns/9ns/12ns access times from clock
- Support up to 75MHz System Operation
- Optimized for use with Intel 486/Pentium secondary cache applications (Interleaved burst sequence and Linear burst sequence)
- Registered data-out for pipelined read
- Byte writable using separate upper/lower byte write input controls
- Write Pass-through functionality
- On-chip burst address counter
- On-chip clocked input and output registers
- 3-state buffered output with asynchronous output enable control
- Standard 52-lead PLCC package with JEDEC pinout

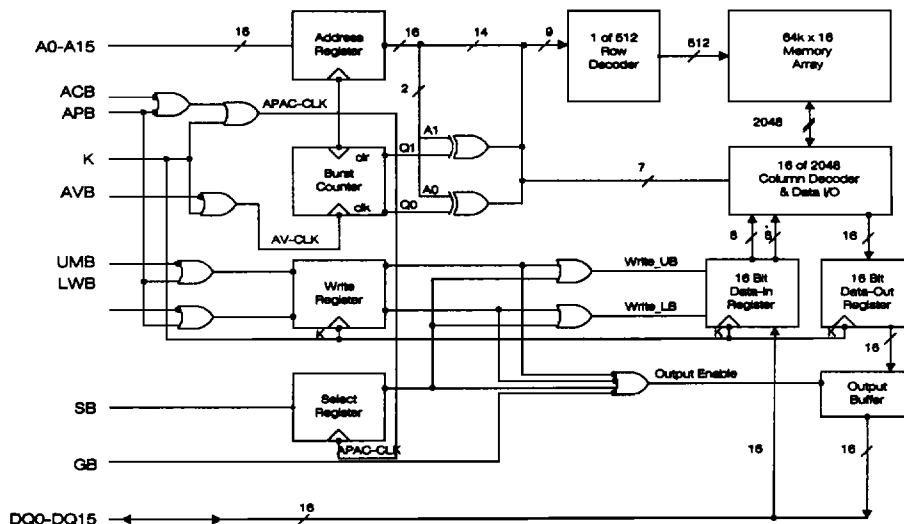
### PIN CONNECTION



### PART NUMBER EXAMPLES

Part No.	Burst Sequence
HY6716100	Interleaved
HY6716101	Linear

### FUNCTION BLOCK DIAGRAM



**PIN DESCRIPTIONS**

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
K	51	Input	Clock. This signal is used to synchronize the device with the system timing. It registers the Addresses, Data inputs, Byte Write Enables and Chip Enable. It may clear or increment the burst counter depending on the state of APB, ACB and AVB.
A0-An	6, 7, 21, 22, 23, 24, 25, 26, 29, 30, 31, 32, 33, 47, 48, 49	Input	Synchronous Address. The addresses are registered at rising edge of the clock.
SB	5	Input	Chip Select. A synchronous control input used to enable(LOW state) and disable(HIGH state) the device. This input is sampled and registered only when a new base address cycle is initiated.
UWB/ LWB	3, 4	Input	Upper and Lower Byte Write Enable. Synchronous control input registered by rising edge of the clock. A LOW state allows data to be written into the device, and a HIGH state initiates a read cycle. UWB controls upper byte(DQ8-15) and LWB controls lower byte(DQ0-7).
APB	1	Input	Address Status from Processor. A synchronous control input registered by rising edge of the clock. A LOW state interrupts the burst sequence and loads in a new address. The device will read out the data at new address. This input over-rides ACB and UWB/LWB.
ACB	2	Input	Address Status from Cache Controller. A synchronous control input registered by rising edge of the clock. When this input is at LOW state and APB is HIGH state, burst sequence is interrupted and new addresses are loaded into the device. The device will perform a read or write cycle with new addresses.
AVB	52	Input	Burst Address Advance. A synchronous control input registered by rising edge of the clock. When this input is at LOW state, the burst counter increments at rising clock edge. A HIGH state will insert wait states into the burst sequence. The burst addresses will wrap around to the initial state after burst counter completed a burst sequence.
GB	50	Input	Output Enable. An asynchronous control input. A LOW state will enable the DQs and a HIGH state will tri-state the DQs.
DQ0-n	8, 9, 12, 13, 14, 15, 18, 19, 34, 35, 38, 39, 40, 41, 44, 45	Input/ Output	Data Input/Outputs. A bi-directional common I/O data pins. GB controls the pins when the device is outputting the data(read cycle) . At write cycle, input data are registered at rising edge of the clock.
Vcc	28	Supply	Positive Power Supply: +5.0V±5%
Vss	27	Supply	Negative Power Supply and Ground Return.
VccQ	10, 17, 36, 43	Supply	Isolated Output Buffer Supply: +5.0V±5%
VssQ	11, 16, 37, 42	Supply	Isolated Output Buffer Ground: GND
NC	20, 46	Supply	No Connection

**TRUTH TABLE**

OPERATION	ADD.	SB	LWB	UWB	APB	ACB	AVB	K	GB	DQ
Deselected, Outputs High Z	X	H	X	X	X	L	X	L-H	X	Hi-Z
Output Disabled, Outputs High Z	X	X	X	X	X	X	X	X	H	Hi-Z
Register New Base Address, Read from Base Address During Next Cycle	NBA	L	X	X	L	X	X	L-H	L	VQ
Register New Base Address, Read from Base Address During Next Cycle	NBA	L	H	H	H	L	X	L-H	L	VQ
Increment Burst Address, Read from Incremented Address During Next Cycle	X	X	H	H	H	H	L	L-H	L	VQ
Read, Non-Incremented Burst Address : Wait-State	X	X	H	H	H	H	H	L-H	L	VQ
Register New Base Address, Write Both Bytes at Base Address	NBA	L	L	L	H	L	X	L-H	X	VD
Register New Base Address, Write Only the Lower Byte at Base Address	NBA	L	L	H	H	L	X	L-H	X	VD
Register New Base Address, Write Only the Upper Byte at Base Address	NBA	L	H	L	H	L	X	L-H	X	VD
Increment Burst Address, Write Both Bytes at Incremented Address	X	X	L	L	H	H	L	L-H	X	VD
Increment Burst Address, Write Only Lower Byte at Incremented Address	X	X	L	H	H	H	L	L-H	X	VD
Increment Burst Address, Write Only Upper Byte at Incremented Address	X	X	H	L	H	H	L	L-H	X	VD
Write Both Bytes, Non-Incremented Burst Address : Wait-State	X	X	L	L	H	H	H	L-H	X	VD
Lower Byte Write, Non-Incremented Burst Address : Wait-State	X	X	L	H	H	H	H	L-H	X	VD
Upper Byte Write, Non-Incremented Burst Address : Wait-State	X	X	H	L	H	H	H	L-H	X	VD

**NOTE :**

All inputs except GB must meet set-up and hold times on the rising edge(LOW to HIGH) of K. The burst counter is cleared or incremented by the rising edge of K combined with the control inputs APB, ACB and AVB.

Hi-Z = High Impedance  
 VQ = Valid Data Output  
 VD = Valid Data Input  
 NBA = New Base Address

X = Don't Care : Input  
 Changing : Output  
 L = Low  
 H = High

**INTERLEAVED BURST SEQUENCE TABLE**

Note that in every case the sequence starts with the initial address, then complements the RAM LSB, then complements both, and finally complements the RAM 2nd LSB. It is only when application-specific address weights are assigned that the sequence appears to differ.

APPLICATION TYPE	SEQUENCE 0	SEQUENCE 1	SEQUENCE 2	SEQUENCE 3
'486 Application :				
Initial	00	04	08	0C
First in Burst	04	00	0C	08
Second in Burst	08	0C	00	04
Third in Burst	0C	08	04	00
Pentium Application :				
Initial	00	08	10	18
First in Burst	08	00	18	10
Second in Burst	10	18	00	08
Third in Burst	18	10	08	00
Arbitrary Application :				
Initial	RAM A1 A0	RAM A1 A0	RAM A1 A0	RAM A1 A0
First in Burst	RAM A1 A0B	RAM A1 A0B	RAM A1 A0B	RAM A1 A0B
Second in Burst	RAM A1B A0	RAM A1B A0	RAM A1B A0	RAM A1B A0
Third in Burst	RAM A1B A0B	RAM A1B A0B	RAM A1B A0B	RAM A1B A0B

**LINEAR BURST SEQUENCE TABLE**

	SEQUENCE 0	SEQUENCE 1	SEQUENCE 2	SEQUENCE 3
Initial	RAM A1B A0B	RAM A1B A0	RAM A1 A0B	RAM A1 A0
First in Burst	RAM A1B A0	RAM A1 A0B	RAM A1 A0	RAM A1B A0B
Second in Burst	RAM A1 A0B	RAM A1 A0	RAM A1B A0B	RAM A1B A0
Third in Burst	RAM A1 A0	RAM A1B A0B	RAM A1B A0	RAM A1 A0B

**ABSOLUTE MAXIMUM RATINGS**

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in the excess of those given in the operation sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	SYMBOL	MIN	MAX	UNIT
Storage Temperature	TSTG	-55	125	°C
Junction Temperature	Tc	...	125	°C
Case Temperature Under Bias	...	-10	85	°C
VCC Potential to VSS	...	-0.5	6	V
Input Voltage(dc)	...	-0.5	Vcc+0.5	V

**RECOMMENDED OPERATING CONDITIONS**

Recommended Operating Conditions are defined as the range of operating conditions over which the device performance meets or exceeds the specified DC characteristics.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Supply	Vcc	4.75	5.25	V
Supply Return, Reference Level	VSS	0.0	0.0	V
Input Low Voltage Level	VIL	-0.5	0.8	V
Input High Voltage Level	VIH	2.2	Vcc+0.5	V
Case Temperature	Tc	0	70	°C

**ELECTRICAL CHARACTERISTIC**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Input Voltage : High Low	V <sub>IH</sub>	...	2.2	...	V <sub>CC</sub> +0.5	V	
	V <sub>IL</sub>	...	-0.5	...	0.8	V	
Output Voltage : High Low	V <sub>OH</sub>	I <sub>OH</sub> =-4.0mA	2.4	...	...	V	
	V <sub>OL</sub>	I <sub>OL</sub> =8.0mA	...	...	0.4	V	
Input Leakage Current	I <sub>L1</sub>	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-2	...	2	μA	
Output Leakage Current	I <sub>L0</sub>	G <sub>B</sub> ≥ V <sub>CC</sub> -0.2, 0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>	-2	...	2	μA	
Power Supply Current : Operating	I <sub>CC</sub>	Device selected, all inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> , V <sub>CC</sub> =MAX, cycle ≥ 1KC min, outputs open.	13ns	...	...	250	mA
			15ns	...	...	225	mA
			20ns	...	...	180	mA
CMOS Standby	I <sub>sb1</sub>	Device deselected; S̄ ≥ V <sub>CC</sub> -0.2, AC ≤ V <sub>SS</sub> +0.2, all inputs ≤ V <sub>SS</sub> +0.2 or ≥ V <sub>CC</sub> -0.2, all inputs static, V <sub>CC</sub> =MAX, f <sub>CLK</sub> =0.	...	...	3	mA	
	I <sub>sb2</sub>	Device deselected; S̄ ≥ V <sub>CC</sub> -0.2, AC ≤ V <sub>SS</sub> +0.2, all inputs ≤ V <sub>SS</sub> +0.2 or ≥ V <sub>CC</sub> -0.2, all inputs static, V <sub>CC</sub> =MAX, cycle time ≥ 1KC min.	...	...	80	mA	
	I <sub>sb3</sub>	Device deselected; S̄ ≥ V <sub>IH</sub> , AC ≤ V <sub>IL</sub> , all inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> , all inputs static, V <sub>CC</sub> =MAX, f <sub>CLK</sub> =0	...	...	20	mA	
Short Circuit Output Current	I <sub>OS</sub>	-	...	...	50	mA	

**TIMING CHARACTERISTICS**

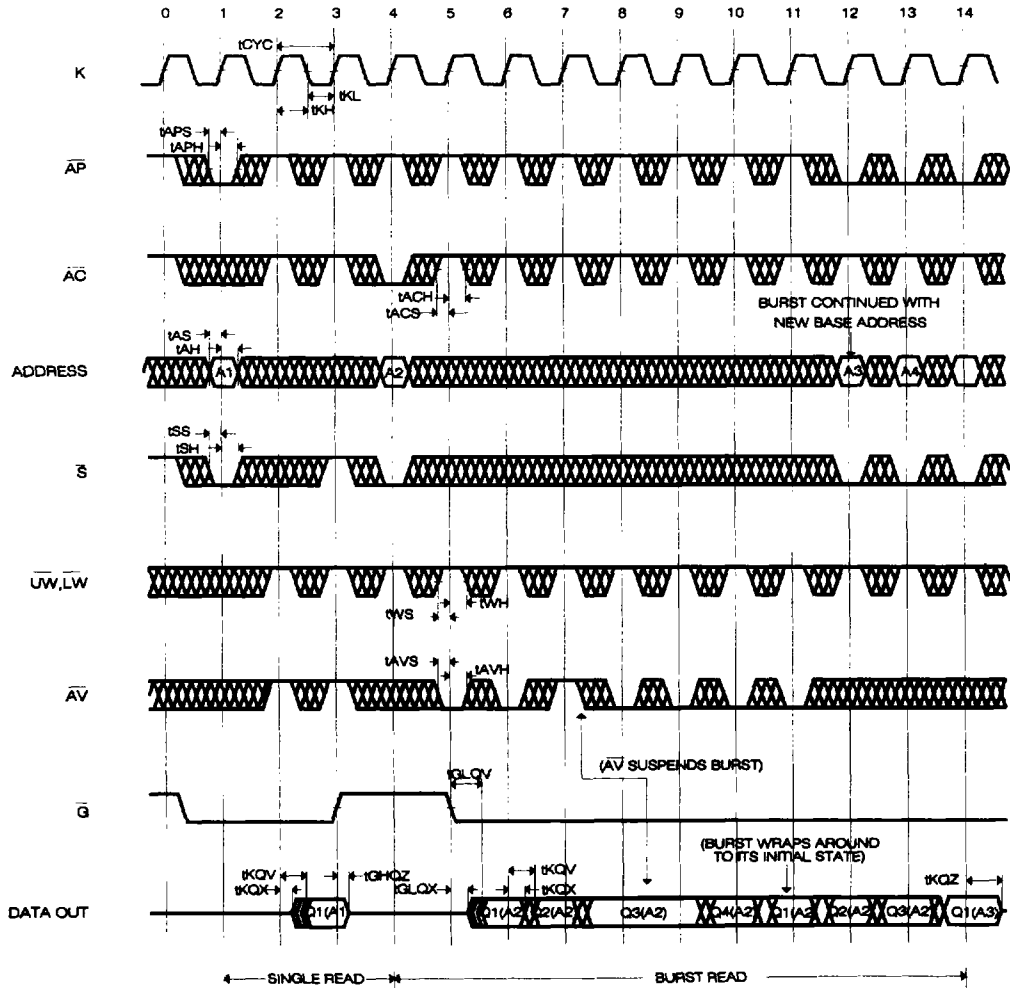
SYMBOL	'486/'P5 Local Bus Rate	50MHz		67MHz		75MHz		Unit
	Cache RAM	12ns		9ns		6ns		
	Parameter	Min	Max	Min	Max	Min	Max	
tcyc	Cycle Time	20	...	15	...	13	...	ns
tkqv	Access Time from Clock	...	12	...	9	...	6	ns
tis	Input Setup Time	3	...	2.0	...	2.0	...	ns
tAS	Address							
tSS	Select							
tAPS	Address Status - $\mu$ P							
tACS	Address Status - Controller							
tAVS	Address Advance							
tWS	Write Enables(LWB, UWB)							
tDS	Data In							
tIH	Input Hold Time	3	...	2.0	...	2.0	...	ns
tAH	Address							
tSH	Select							
tAPH	Address Status - $\mu$ P							
tACH	Address Status - Controller							
tAVH	Address Advance							
tWH	Write Enables (LWB, UWB)							
tDH	Data In							
tkH	Clock High Pulse Width	7	...	5.5	...	4.5	...	ns
tkL	Clock Low Pulse Width	7	...	5.5	...	4.5	...	ns
tGLQX	Output Enable to Output Active	3	...	2	...	1	...	ns
tGLQV	Output Enable Time	...	7	...	6	...	6	ns
tGHQZ	Output Disable Time	...	7	...	6	...	6	ns
tkQX	Output Change from Clock & Output Enable from Clock	4	...	3	...	2	...	ns
tkQZ	Output Disable from Clock	...	10	...	8	...	7	ns

**NOTE :**

1. Switching measurements are from 1.5V levels on the inputs to 1.5V levels on the outputs, except for enable and disable times.
2. Enable and disable time measurements are from 1.5V levels on the inputs to change of 0.1V in the output levels.
3. See figure AC TEST LOAD A. for output load.
4. Input levels for switching measurements are 0V to 3.0V.
5. Input rise and fall times for switching measurements are  $\leq 2.0$ ns(20% to 80%).
6. This unit is measured using output loading as specified in figure AC TEST LOAD B.

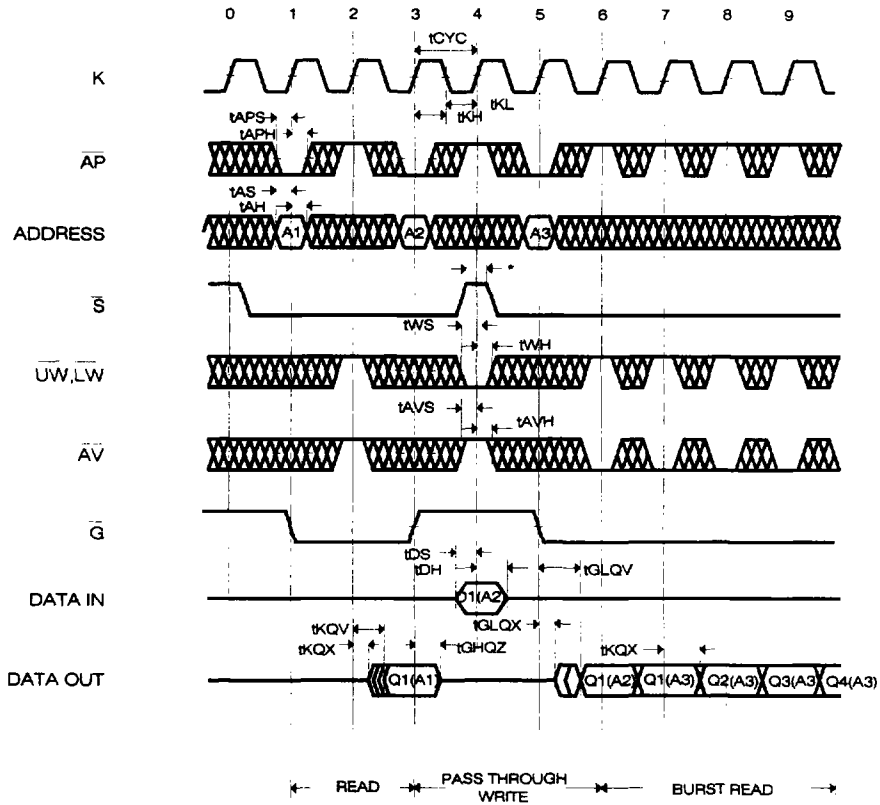
**TIMING DIAGRAM**

**READ CYCLE**



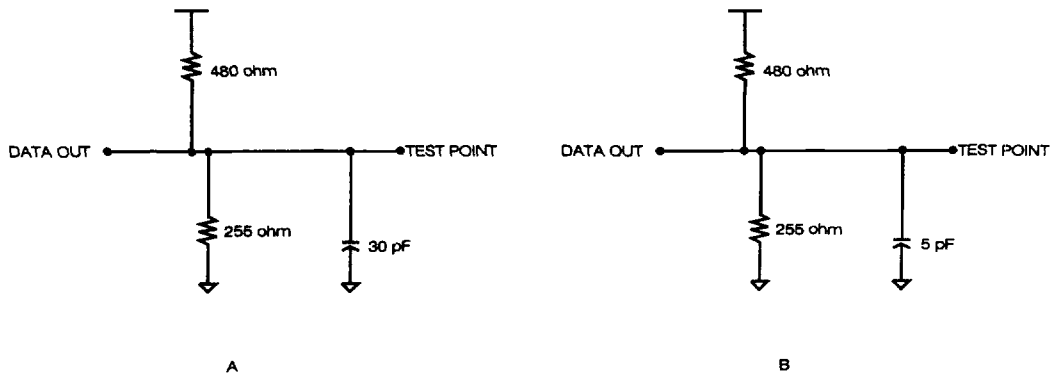


**READ AND WRITE**

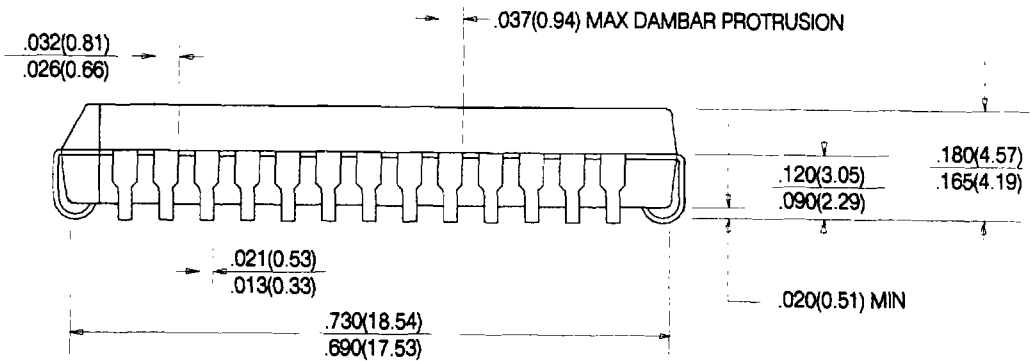
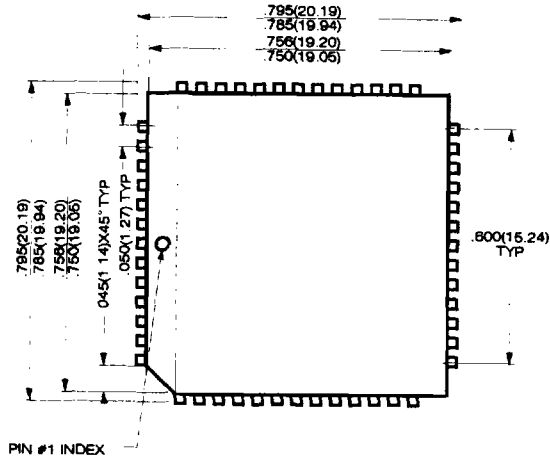


\*The state of S at 4 is ignored due to address A2 being registered one cycle earlier.

**AC TEST LOAD**



**PACKAGE INFORMATION**



**ORDERING INFORMATION**

<b>PART NO.</b>	<b>SPEED(ns)</b>	<b>FEATURES</b>	<b>PACKAGE</b>
HY6716100C	6/9/12	Pipelined (Interleaved)	52pin PLCC
HY6716101C	6/9/12	Pipelined (Linear)	52pin PLCC