National Semiconductor

100391
Low Power Single Supply Hex TTL-to-ECL Translator

General Description

The 100391 is a hex translator for converting TTL logic levels to F100K ECL logic levels. The unique feature of this translator, is the ability to do this translation using only one +5V supply. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. A common enable (E), when low, holds all inverting outputs HIGH and all non-inverting inputs LOW.

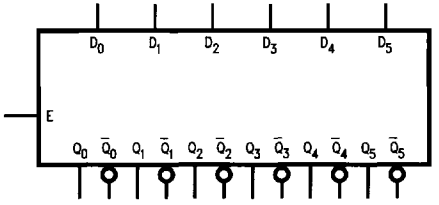
The 100391 is ideal for those mixed ECL/TTL applications which only have a +5V supply available. When used in the differential mode, the 100391, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems.

Features

- Operates from a single +5V supply
- Differential ECL outputs
- 2000V ESD protection
- Companion chip to 100390 hex ECL-to-TTL translator

Ordering Code: See Section 6

Logic Symbol



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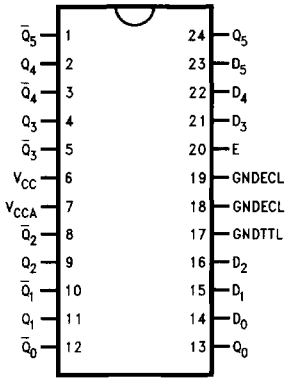
Pin Names	Description
D_0–D_5	Data Inputs (TTL)
Q_0–Q_5	Data Outputs (PECL)
$\overline{Q}_0$–$\overline{Q}_5$	Inverting Data Outputs (PECL)
E	Enable Input (TTL)

Connection Diagrams

24-Pin DIP and SOIC



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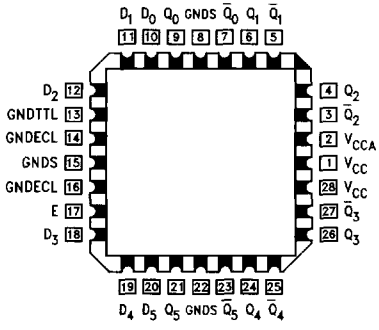
28-Pin PCC



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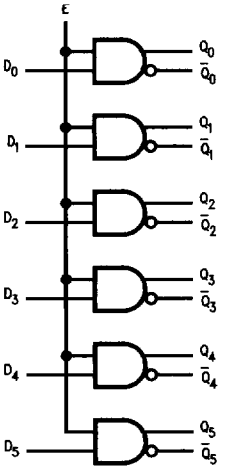
Logic Diagram



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Truth Table

Inputs		Outputs	
D_n	E	Q_n	$\overline{Q}_n$
H	H	H	L
L	H	L	H
H	L	L	H
L	L	L	H

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
ECL Output Current (DC Output HIGH)	−50 mA
TTL Input Voltage (Note 3)	−0.5V to +7.0V
TTL Input Current (Note 3)	−30 mA to +5.0 mA
ESD (Last Passing Voltage) (Min) (Note 2)	2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{CC})	4.5V to 5.5V
Commercial	

Commercial Version

TTL-to-ECL DC Electrical Characteristics V_{CC} = +5.0V ±10%, GND = 0V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	V_{CC} − 1025	V_{CC} − 955	V_{CC} − 870	mV	V_{IN} = $V_{IH\ (max)}$ or $V_{IL\ (min)}$ Loading with 50Ω to V_{CC} − 2V
V_{OL}	Output LOW Voltage	V_{CC} − 1890	V_{CC} − 1705	V_{CC} − 1620	mV	
V_{OHC}	Output HIGH Voltage Corner Point High	V_{CC} −1035			mV	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$ Loading with 50Ω to V_{CC} − 2V
V_{OLC}	Output LOW Voltage Corner Point Low			V_{CC} − 1610	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			10	μA	V_{IN} = +2.7V
	Breakdown Test			20	μA	V_{IN} = +5.5V
I_{IL}	Input LOW Current D_n E	−0.8 −4.2			mA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{CC}	V_{CC} Supply Current	32		69	mA	Inputs Open

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP Package AC Electrical Characteristics

V_{CC} = 5.0V ±10%

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	1.40	0.35	1.30	0.40	1.30	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.40	1.50	0.45	1.40	0.50	1.40	ns	*Figures 1, 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.70	0.35	1.70	0.35	1.70	ns	*Figures 1, 2*

SOIC and PCC Package AC Electrical Characteristics

V_{CC} = 5.0V ±10%

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	1.40	0.35	1.30	0.40	1.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.40	1.50	0.45	1.40	0.50	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.70	0.35	1.70	0.35	1.70	ns	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		750		750		750	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		700		700		700	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		450		450		450	ps	PCC Only (Note 1)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		525		525		525	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design

Industrial Version

DC Electrical Characteristics

V_{CC} = +5.0V ±10%, GND = 0V (Note 1)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	V_{CC} − 1085	V_{CC} − 870	V_{CC} − 1025	V_{CC} − 870	mV	V_{IN} = $V_{IH\ (max)}$ or $V_{IL\ (min)}$
V_{OL}	Output LOW Voltage	V_{CC} − 1890	V_{CC} − 1575	V_{CC} − 1890	V_{CC} − 1620	mV	Loading with 50Ω to V_{CC} − 2V
V_{OHC}	Output HIGH Voltage Corner Point High	V_{CC} − 1095		V_{CC} − 1035		mV	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$ Loading with 50Ω to V_{CC} − 2V
V_{OLC}	Output LOW Voltage Corner Point High		V_{CC} − 1565		V_{CC} − 1610	mV	
V_{IH}	Input HIGH Voltage	2.0	5.0	2.0	5.0	V	
V_{IL}	Input LOW Voltage	0	0.8	0	0.8	V	
I_{IH}	Input HIGH Current		10		10	μA	V_{IN} = +2.7V
	Breakdown Test		20		20	μA	V_{IN} = +5.5V
I_{IL}	Input LOW Current D_n E	 −0.8 −4.2		 −0.8 −4.2		mA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2		−1.2		V	I_{IN} = −18 mA
I_{CC}	V_{CC} Supply Current	29	69	29	69	mA	Inputs Open

PCC AC Electrical Characteristics

V_{CC} = +5.0V ±10%, GND = 0V

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.20	1.50	0.35	1.30	0.40	1.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.35	1.60	0.45	1.40	0.50	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.70	0.35	1.70	0.35	1.70	ns	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Military Version-Preliminary

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	V_{CC} − 1025	V_{CC} − 870	mV	0°C to +125°C	V_{IN} = $V_{IH\ (max)}$ or $V_{IL\ (min)}$	Loading with 50Ω to V_{CC} − 2.0V	1, 2, 3
		V_{CC} − 1085	V_{CC} − 870	mV	−55°C			
V_{OL}	Output LOW Voltage	V_{CC} − 1830	V_{CC} − 1620	mV	0°C to +125°C			
		V_{CC} − 1830	V_{CC} − 1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	V_{CC} − 1035		mV	0°C to +125°C	V_{IN} = $V_{IH\ (min)}$ or $V_{IL\ (max)}$	Loading with 50Ω to V_{CC} − 2.0V	1, 2, 3
		V_{CC} − 1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		V_{CC} − 1610	mV	0°C to +125°C			
			V_{CC} − 1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	2.0		V	−55°C to +125°C			1, 2, 3, 4
V_{IL}	Input LOW Voltage		0.8	V	−55°C to +125°C			1, 2, 3, 4
I_{IH}	Input HIGH Current		70	μA	−55°C to 125°C	V_{IN} = +2.7V		1, 2, 3
I_{IL}	Input LOW Current	−1.0		mA	−55°C to +125°C	V_{IN} = +0.5V		1, 2, 3
V_{FCD}	Input Clamp Diode Voltage	−1.2		V	−55°C to +125°C	I_{IN} = −18 mA		1, 2, 3
I_{CC}	V_{CC} Supply Current	20	70	mA	−55°C to +125°C	Inputs Open		1, 2, 3

AC Electrical Characteristics V_{CC} = +5.0 ± 10%, GND = 0V

Symbol	Parameter	T = −55°C		T = +25°C		T = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.40	2.50	0.50	2.10	0.50	2.10	ns	Figures 1, 2	1, 2, 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	2.00	0.30	2.00	0.30	2.00	ns	Figures 1, 2	1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold termperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C and +125°C, Subgroups 1, 2, 3, 7 and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C and +125°C, Subgroups A1, 2, 3, 7 and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Switching Waveforms

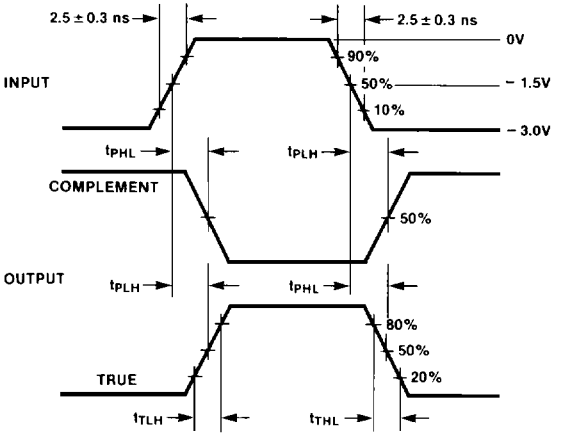

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FIGURE 1. Propagation Delay and Transition Times

Test Circuit

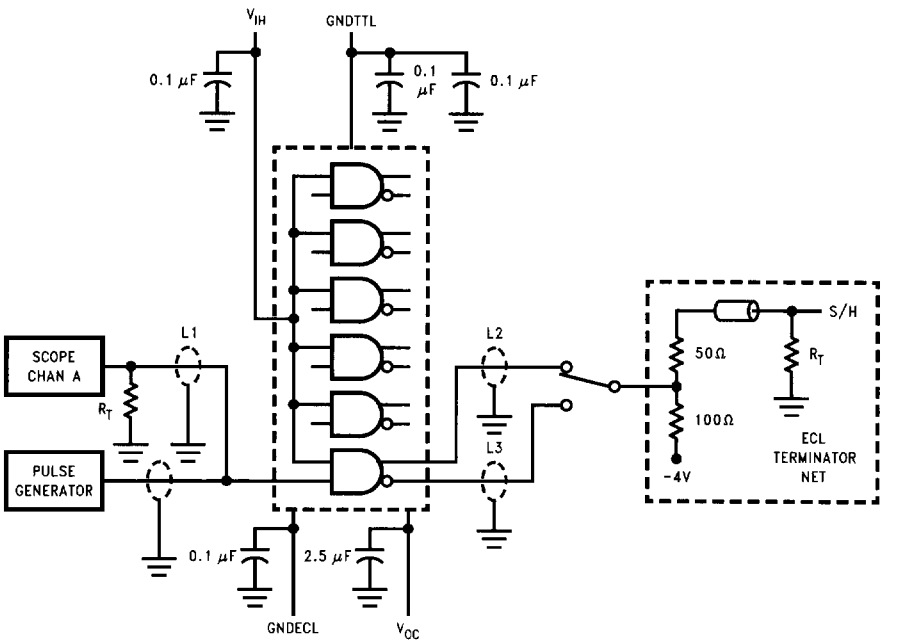

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FIGURE 2. AC Test Circuit

Notes:

$V_{CC} = V_{CCA} = +2V$, GNDECL = GNDTTL = 3.0V
$V_{IH} = 0V$, $V_{IL} = -3V$
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF