

40-Channel Symmetric Row Driver

Ordering Information

Device	Package Options			
	80-Lead Ceramic Gullwing	64-Lead 3-Sided Plastic Gullwing	Die in waffle pack	80-Lead Ceramic Gullwing (MIL-STD-883 Processed*)
HV7224	HV7224DG	HV7224PG	HV7224X	RBHV7224DG
HV7324	–	–	HV7324X**	–

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

** Refer to die specification section for dimensions.

Features

- Processed with HVCMOS® technology
- Symmetric row drive (reduces latent imaging in ACTFEL displays)
- Output voltage up to 240V
- Low-power level shifting
- Source/Sink current 70mA (min.)
- Shift Register Speed 3MHz
- Pin-programmable shift direction (DIR, SHIFT)
- Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD} ¹	-0.5V to +7V	
Supply voltage, V_{PP}	-0.5V to +260V	
Logic input levels	-0.5V to $V_{DD} + 0.5V$	
Continuous total power dissipation ²	Ceramic	1500mW
	Plastic	1200mW
Operating temperature range	Industrial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range	-65°C to +150°C	
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C	

Notes: 1. All voltages are referenced to GND.
2. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV72 and HV73 are low-voltage serial to high-voltage parallel converters with push-pull outputs. They are especially suitable for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays.

When the data reset pin (DR_{IO}) is at logic high, it will reset all the outputs of the internal shift register to zero. At the same time, the output of the shift register will start shifting a logic high from the least significant bit to the most significant bit. The DR_{IO} can be triggered at any time. The DIR and SHIFT pins control the direction of data shift through the device. When DIR is at logic high, DR_{OA} is the input and DR_{OB} is the output. When DIR is grounded, DR_{IOB} is the input and the DR_{IOA} is the output. See the Output Sequence Operation Table for output sequence. The \overline{POL} and \overline{OE} pins perform the polarity select and output enable function respectively. Data is loaded on the low to high transition of the clock. A logic high will cause the output to swing to V_{PP} if \overline{POL} is high, or to GND if \overline{POL} is low. All outputs will be in High-Z state if \overline{OE} is at logic high. Data output buffers are provided for cascading devices.

The HV73 has the same electrical characteristics as the HV72. The HV73 is designed and layout for flip chip assembly and is available only in die form.

Electrical Characteristics

(over recommended operating conditions of $V_{DD} = 5V$, $V_{PP} = 240V$, and $T_A = 25^\circ C$ unless noted)

DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		10	mA	$f_{CLK} = 3MHz$
I_{PP}	High voltage supply current		2.0	mA	Outputs low or High-Z
			4.0	mA	One Output High ¹
I_{DDQ}	Quiescent V_{DD} supply current		100	μA	All $V_{IN} = GND$ or V_{DD}
V_{OH}	High-level output	HV _{OUT}	190	V	$I_O = -70mA (-50mA)^2$
		Data out	4.5	V	$I_O = -100\mu A$
V_{OL}	Low-level output	HV _{OUT}	50	V	$I_O = 70mA (50mA)^2$
		Data out	0.5	V	$I_O = 100\mu A$
I_{IH}	High-level logic input current		1	μA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		-1	μA	$V_{IL} = 0V$

Notes:

1. Only one output can be turned on at a time.
2. Over military temperature range.

AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		3	MHz	
$t_{W(H/L)}$	Pulse width - clock high or low	150		ns	
t_{SUD}	Data set-up time before clock rises	50		ns	
t_{HD}	Data hold time after clock rises	50		ns	
t_{SUC}	HV _{OUT} delay from clock rises (Hi-Z to H or L)		1	μs	$C_L = 330pF // R_L = 10k\Omega$
t_{SUE}	HV _{OUT} delay from $\overline{\text{Output Enable}}$ falls		600	ns	$C_L = 330pF // R_L = 10k\Omega$
t_{HC}	HV _{OUT} delay from clock rises (H or L to Hi-Z)		2	μs	$C_L = 330pF // R_L = 10k\Omega$
t_{HE}	HV _{OUT} delay from $\overline{\text{Output Enable}}$ rises		600	ns	$C_L = 330pF // R_L = 10k\Omega$
t_{DHL}^*	Delay time clock to data output falls		250	ns	$C_L = 15pF$
t_{DLH}^*	Delay time clock to data output rises		250	ns	$C_L = 15pF$
t_{ONF}	HV _{OUT} fall time		2	μs	$C_L = 330pF // R_L = 10k\Omega$
t_{ONR}	HV _{OUT} rise time		2	μs	$C_L = 330pF // R_L = 10k\Omega$
t_{POW}	$\overline{\text{POL}}$ pulse width	3		μs	
t_{OEW}	$\overline{\text{Output Enable}}$ pulse width	3		μs	
	Slew rate, V_{PP} or GND		45	V/ μs	One active output driving 4.7nF load

* The delay is measured from the trailing edge of the clock but the data is triggered by the rising edge of the clock. There is an internal delay for the data output which is equal to t_{WH} . Therefore the delay is measured from the trailing edge of the clock.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	
V_{DD}	Logic supply voltage	4.5	5.5	V	
V_{PP}	High voltage supply [†]	0	240	V	
V_{IH}	High-level input voltage	$0.7 V_{DD}$	V_{DD}	V	
V_{IL}	Low-level input voltage	0	$0.2V_{DD}$	V	
f_{CLK}	Clock frequency		3	MHz	
I_O	High voltage output current		± 70	mA	
T_A	Operating free-air temperature	Industrial	-40	+85	°C
		Military Hi-Rel (RB)	-55	+125	°C
I_{OD}	Allowable pulse current through output diode		300	mA	

Notes:

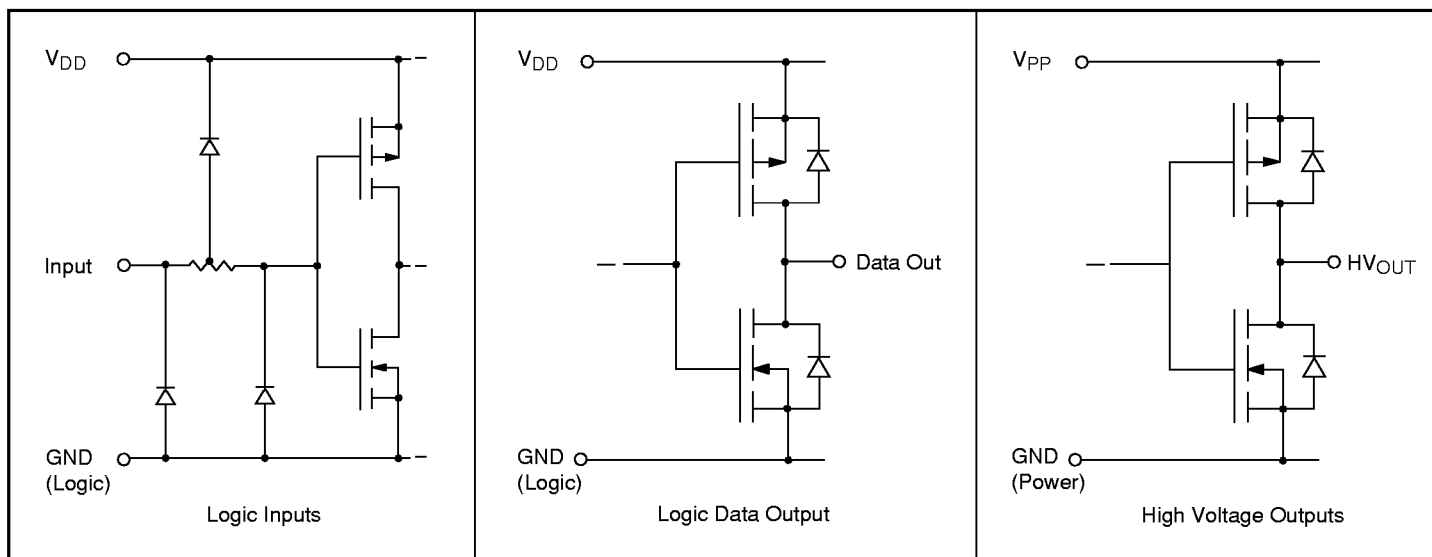
[†] Output will not switch at $V_{PP} = 0V$.

Power-up sequence should be the following:

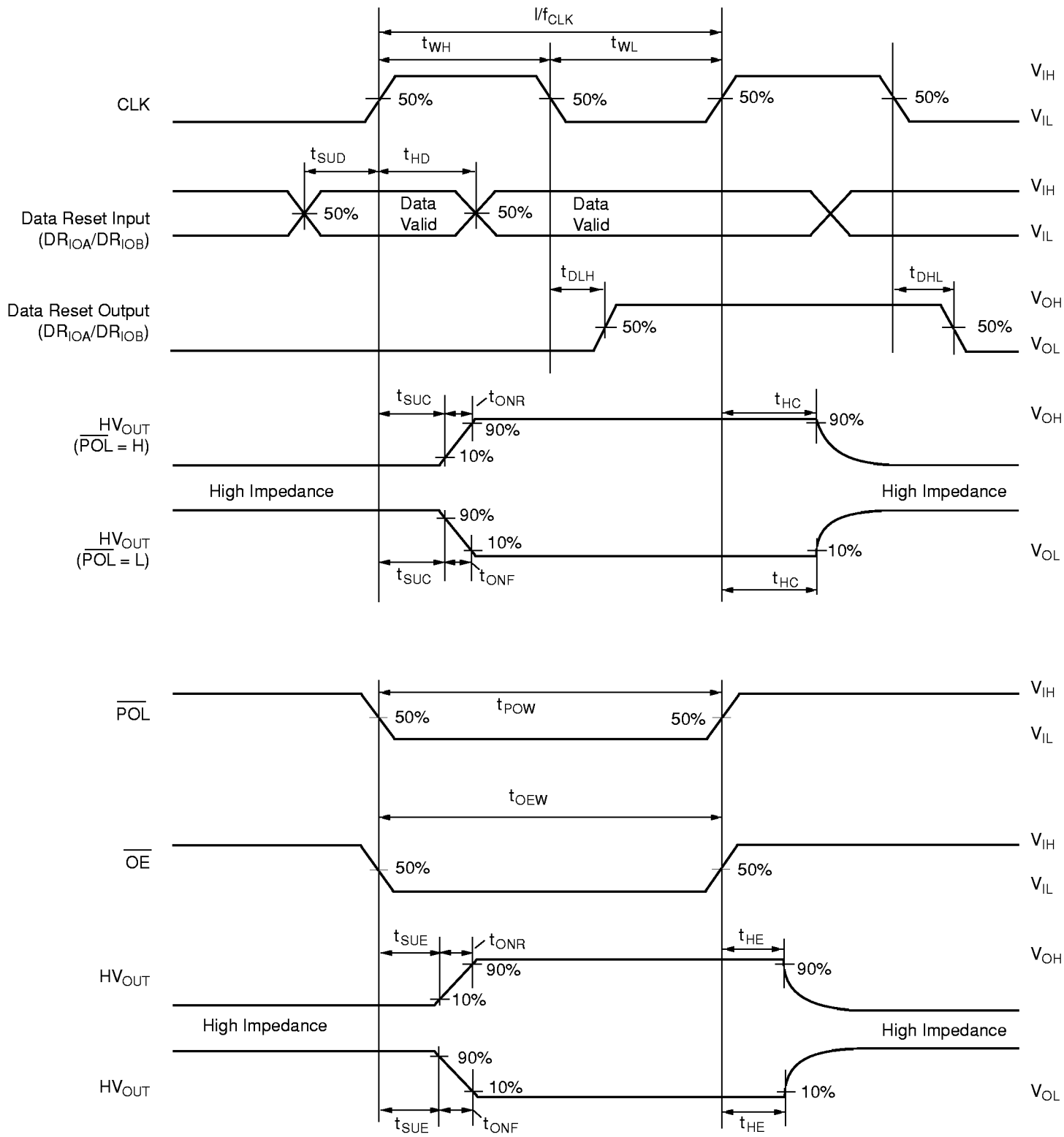
1. Connect ground.
2. Apply V_{DD} .
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP} .

Power-down sequence should be the reverse of the above.

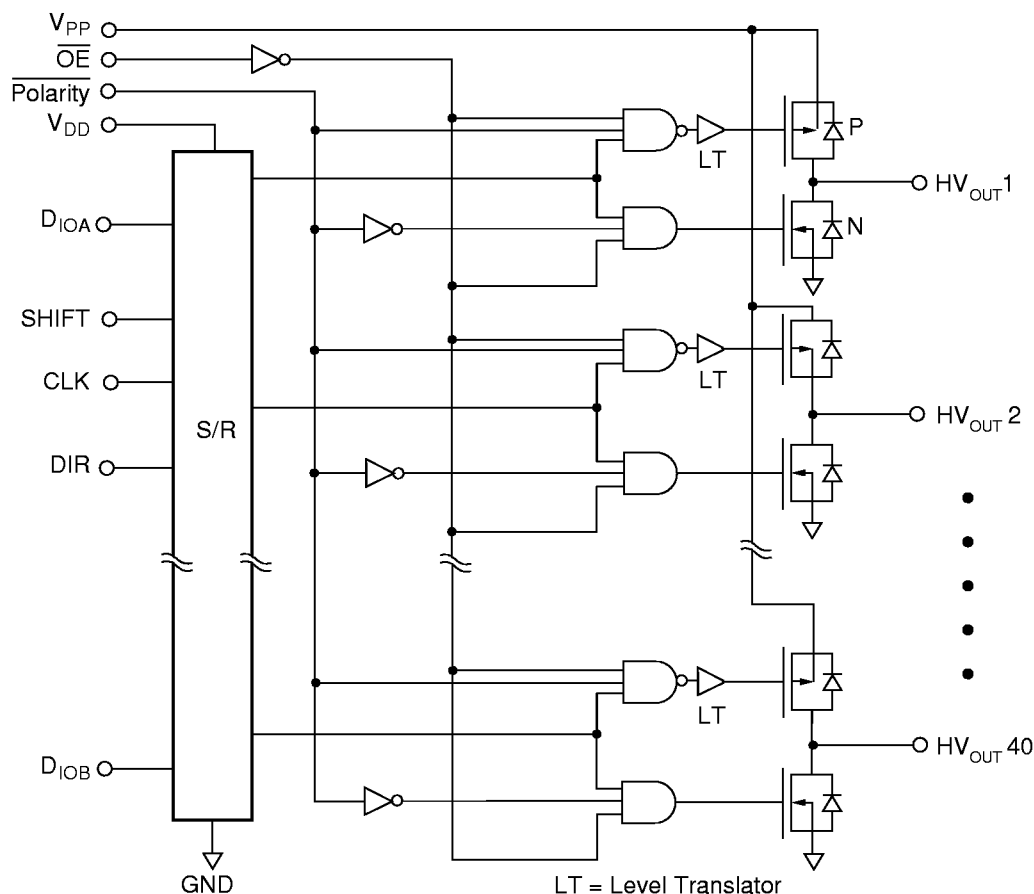
Input and Output Equivalent Circuits


12

Switching Waveforms



Functional Block Diagram



Function Table

I/O Relations	Inputs					HV Outputs
	CLK	DIR	S/R Data	POL	OE	
O/P HIGH	X	X	H	H	L	H
O/P OFF	X	X	L	X	L	HIGH-Z
O/P LOW	X	X	H	L	L	L
O/P OFF	X	X	X	X	H	All O/P HIGH-Z

Notes:

H = logic high level, L = logic low level, X = irrelevant

Output Sequence Operation Table

DIR	Shift	Data Reset In	Data Reset Out	HV_OUT# Sequence	Direction*	Option (See pin-out on P. 12-146)
L	L	DR _{IOB}	DR _{IOA} ¹	40 → 1	↺	A
H	L	DR _{IOA}	DR _{IOB} ²	1 → 40	↻	A
L	H	DR _{IOB}	DR _{IOA} ¹	20 → 1 → 40 → 21	↺	B
H	H	DR _{IOA}	DR _{IOB} ²	21 → 40 → 1 → 20	↻	B

* Reference to package outline or chip layout drawing.

1. DR_{IOA} is DR_{IOB} delayed by 40 clock pulses.

2. DR_{IOB} is DR_{IOA} delayed by 40 clock pulses.



Pin Configurations

HV72

Option A:

Pin	Function	Pin	Function
1	HV _{OUT} 1/40	33	NC
2	HV _{OUT} 2/39	34	DR _{IOB}
3	HV _{OUT} 3/38	35	\overline{OE}
4	HV _{OUT} 4/37	36	NC
5	HV _{OUT} 5/36	37	\overline{POL}
6	HV _{OUT} 6/35	38	NC
7	HV _{OUT} 7/34	39	V _{DD}
8	HV _{OUT} 8/33	40	NC
9	HV _{OUT} 9/32	41	GND (Logic)
10	HV _{OUT} 10/31	42	GND (Power)
11	HV _{OUT} 11/30	43	NC
12	HV _{OUT} 12/29	44	V _{PP}
13	HV _{OUT} 13/28	45	HV _{OUT} 21/20
14	HV _{OUT} 14/27	46	HV _{OUT} 22/19
15	HV _{OUT} 15/26	47	HV _{OUT} 23/18
16	HV _{OUT} 16/25	48	HV _{OUT} 24/17
17	HV _{OUT} 17/24	49	HV _{OUT} 25/16
18	HV _{OUT} 18/23	50	HV _{OUT} 26/15
19	HV _{OUT} 19/22	51	HV _{OUT} 27/14
20	HV _{OUT} 20/21	52	HV _{OUT} 28/13
21	V _{PP}	53	HV _{OUT} 29/12
22	NC	54	HV _{OUT} 30/11
23	GND (Power)	55	HV _{OUT} 31/10
24	GND (Logic)	56	HV _{OUT} 32/9
25	DIR	57	HV _{OUT} 33/8
26	V _{DD}	58	HV _{OUT} 34/7
27	CLK	59	HV _{OUT} 35/6
28	NC	60	HV _{OUT} 36/5
29	SHIFT	61	HV _{OUT} 37/4
30	NC	62	HV _{OUT} 38/3
31	DR _{IOA}	63	HV _{OUT} 39/2
32	NC	64	HV _{OUT} 40/1

Note: Pin designation for DIR H/L, SHIFT = L.
 Example: For DIR = H, pin 1 is HV_{OUT}1.
 For DIR = L, pin 1 is HV_{OUT}40.
 Pins 65–80 are NC (ceramic only).

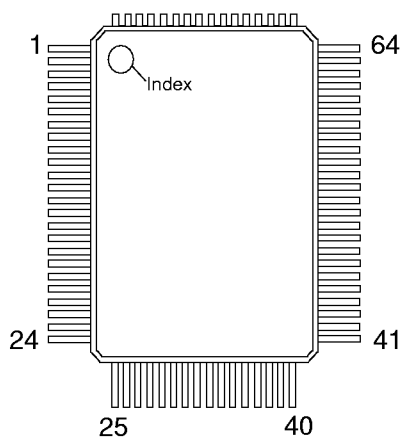
HV72

Option B:

Pin	Function	Pin	Function
1	HV _{OUT} 20/21	33	NC
2	HV _{OUT} 19/22	34	DR _{IOB}
3	HV _{OUT} 18/23	35	\overline{OE}
4	HV _{OUT} 17/24	36	NC
5	HV _{OUT} 16/25	37	\overline{POL}
6	HV _{OUT} 15/26	38	NC
7	HV _{OUT} 14/27	39	V _{DD}
8	HV _{OUT} 13/28	40	NC
9	HV _{OUT} 12/29	41	GND (Logic)
10	HV _{OUT} 11/30	42	GND (Power)
11	HV _{OUT} 10/31	43	NC
12	HV _{OUT} 9/32	44	V _{PP}
13	HV _{OUT} 8/33	45	HV _{OUT} 40/1
14	HV _{OUT} 7/34	46	HV _{OUT} 39/2
15	HV _{OUT} 6/35	47	HV _{OUT} 38/3
16	HV _{OUT} 5/36	48	HV _{OUT} 37/4
17	HV _{OUT} 4/37	49	HV _{OUT} 36/5
18	HV _{OUT} 3/38	50	HV _{OUT} 35/6
19	HV _{OUT} 2/39	51	HV _{OUT} 34/7
20	HV _{OUT} 1/40	52	HV _{OUT} 33/8
21	V _{PP}	53	HV _{OUT} 32/9
22	NC	54	HV _{OUT} 31/10
23	GND (Power)	55	HV _{OUT} 30/11
24	GND (Logic)	56	HV _{OUT} 29/12
25	DIR	57	HV _{OUT} 28/13
26	V _{DD}	58	HV _{OUT} 27/14
27	CLK	59	HV _{OUT} 26/15
28	NC	60	HV _{OUT} 25/16
29	SHIFT	61	HV _{OUT} 24/17
30	NC	62	HV _{OUT} 23/18
31	DR _{IOA}	63	HV _{OUT} 22/19
32	NC	64	HV _{OUT} 21/20

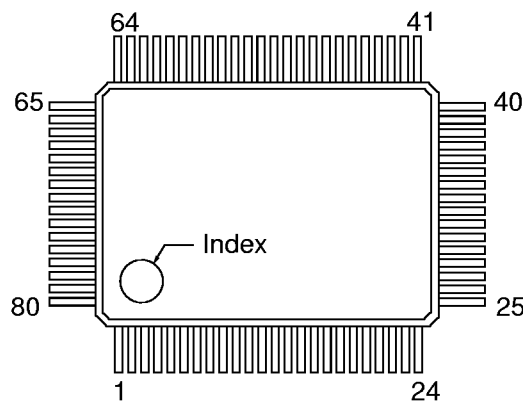
Note: Pin designation for DIR L/H, SHIFT = H.
 Example: For DIR = L, pin 1 is HV_{OUT}20.
 For DIR = H, pin 1 is HV_{OUT}21.
 Pins 65–80 are NC (ceramic only).

Package Outline



top view

3-sided Plastic 64-pin Gullwing Package



top view

80-pin Ceramic Gullwing Package