

# KS54HCTLS 843/844 KS74HCTLS

## 9-Bit Bus Interface D-Type Latches with 3-State Outputs

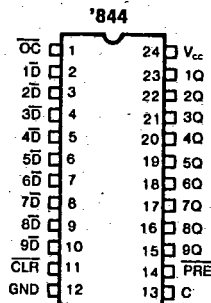
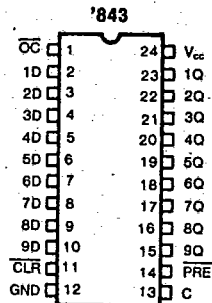
T-46-07-05

### Preliminary Specifications

#### FEATURES

- Bus-Structured Pinout
- Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High Impedance
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

#### PIN CONFIGURATIONS



#### DESCRIPTION

These 9-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

The nine latches are transparent D-type. The '843 has noninverting data (D) inputs and the '844 has inverting  $\bar{D}$  inputs.

A buffered output control ( $\overline{OC}$ ) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ( $\overline{OC}$ ) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### FUNCTION TABLES

'843

INPUTS					OUTPUT
PRE	CLR	$\overline{OC}$	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	$Q_0$
X	X	H	X	X	Z

'844

INPUTS					OUTPUT
PRE	CLR	$\overline{OC}$	C	$\bar{D}$	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	$Q_0$
X	X	H	X	X	Z

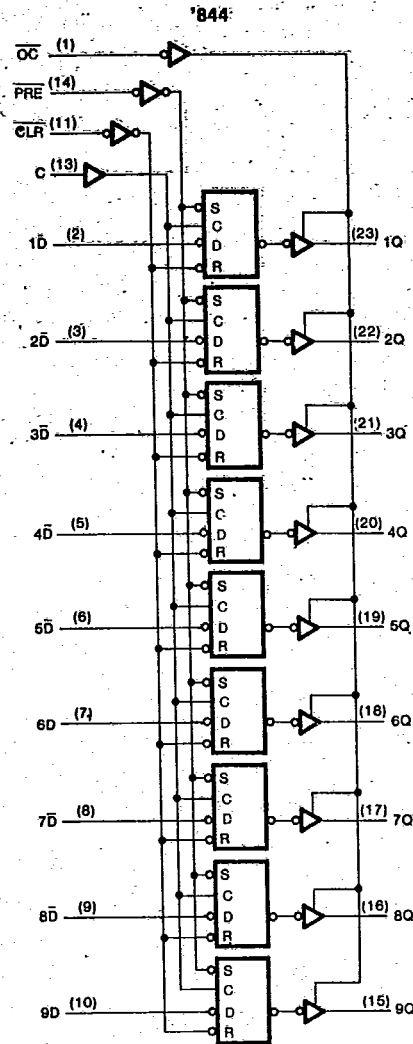
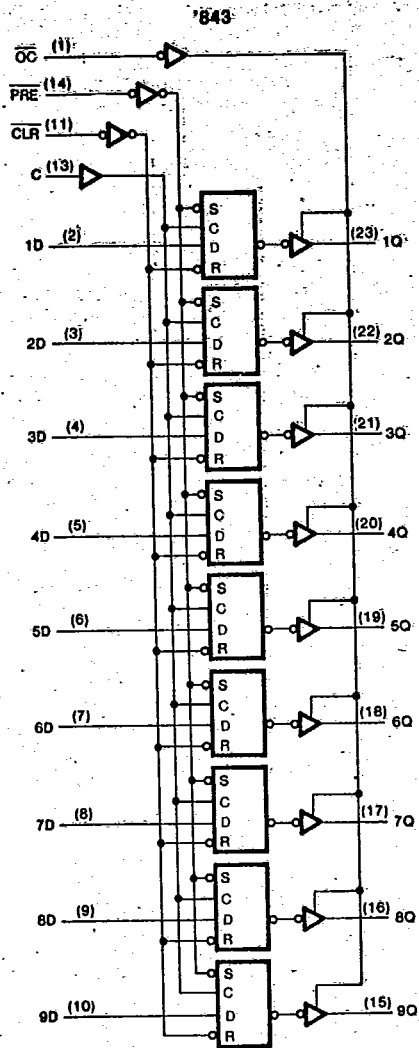
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KS54HCTLS 843/844  
KS74HCTLS

9-Bit Bus Interface D-Type  
Latches with 3-State Outputs

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LOGIC DIAGRAMS



**KS54HCTL5 843/844**  
**KS74HCTL5**

**9-Bit Bus Interface D-Type Latches with 3-State Outputs**

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**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C  
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTL5: -40°C to +85°C  
 KS54HCTL5: -55°C to +125°C

Input Rise & Fall Times,  $t_r, t_f$  . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_s = 25^\circ C$			Unit	
			Typ	KS74HCTL5 $T_a = -40^\circ C$ to $+85^\circ C$	KS54HCTL5 $T_a = -55^\circ C$ to $+125^\circ C$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT} = V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT} = 0\mu A$		2.7	2.9	3.0	mA

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**KS54HCTLS**  
**KS74HCTLS**
**843/844**
**9-Bit Bus Interface D-Type**  
**Latches with 3-State Outputs**

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTLS843, HCTLS844)

Characteristic	Symbol	Conditions†	$T_s = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_s = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_s = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Maximum Propagation Delay, to	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	18	24	30	36	ns		
			21	27	35	42			
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	18	24	30	36	ns		
			21	27	35	42			
Maximum Propagation Delay, C to any Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21	28	35	42	ns		
			24	31	40	48			
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21	28	35	42	ns		
			24	31	40	48			
Maximum Propagation Delay, PRE to Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	23	30	38	46	ns		
Maximum Propagation Delay, CLR to Q	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	23	30	38	46	ns		
			26	33	43	52			
Maximum Output Enable Time, $\overline{OC}$ to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	18	24	30	36	ns	
			$C_L = 150\text{pF}$	21	27	35	42		
	$t_{PZL}$		$C_L = 50\text{pF}$	18	24	30	36		
			$C_L = 150\text{pF}$	21	27	35	42		
Maximum Output Disable Time, $\overline{OC}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	18	24	30	36	ns		
	$t_{PLZ}$	$C_L = 50\text{pF}$	18	24	30	36			
Minimum Pulse Width, C High	$t_w$		15	20	25	30	ns		
Minimum Setup Time, Data after $C\downarrow$	$t_{su}$		12	16	20	24	ns		
Minimum Hold Time, Data before $C\downarrow$	$t_h$		6	8	10	12	ns		
Maximum Input Capacitance	$C_{IN}$		5				pF		
Maximum Output Capacitance	$C_{OUT}$		10				pF		
Power Dissipation Capacitance (per stage)	$C_{PD}$	$\overline{OC} = V_{CC}$	5				pF		
		$\overline{OC} = \text{GND}$	30						

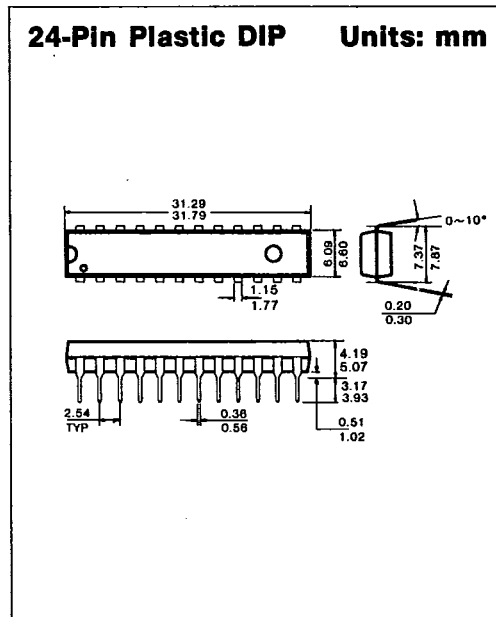
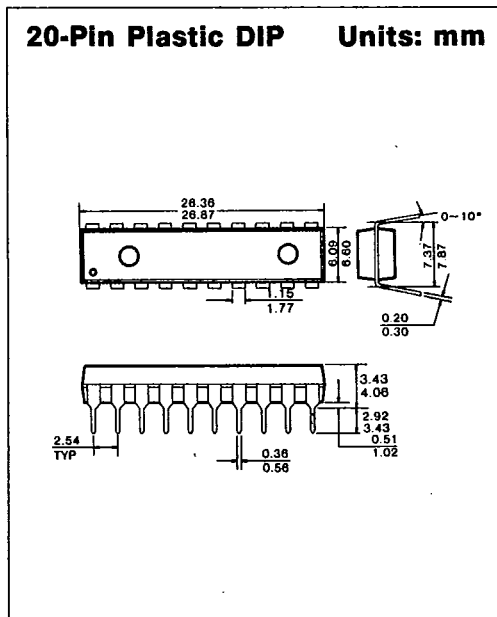
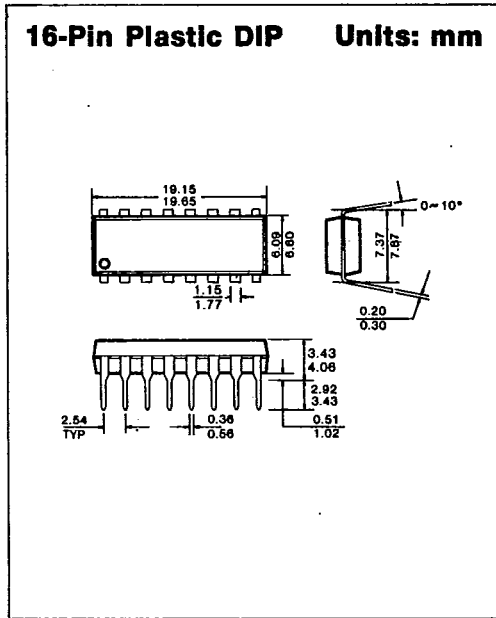
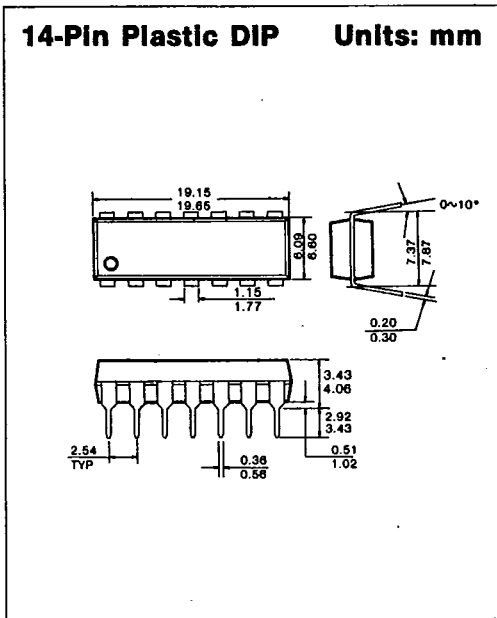
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

† For AC switching test circuits and timing waveforms see section 2.

**PACKAGE DIMENSIONS**

T-90-20

**1. PLASTIC PACKAGES**



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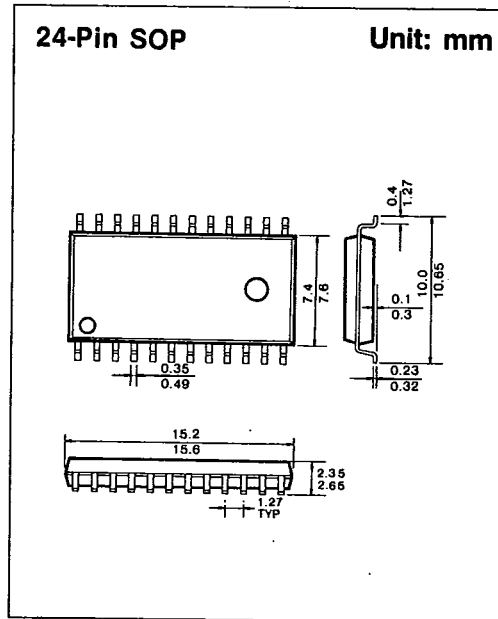
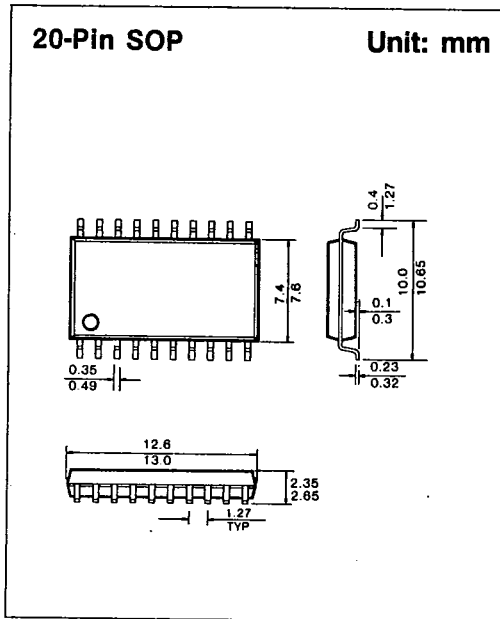
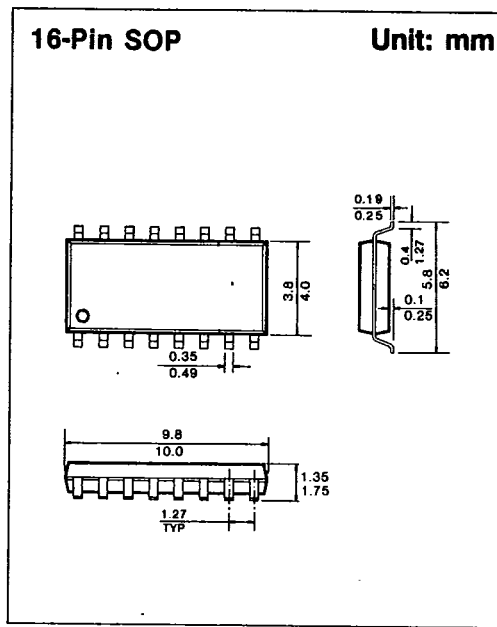
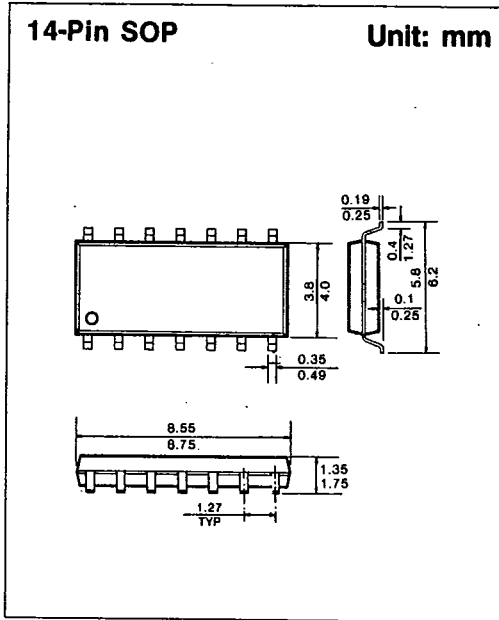
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**PACKAGE DIMENSIONS**

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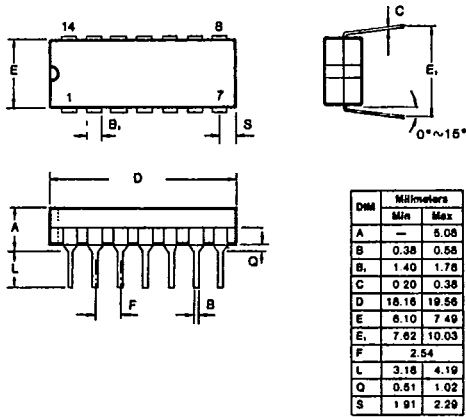


**PACKAGE DIMENSIONS**

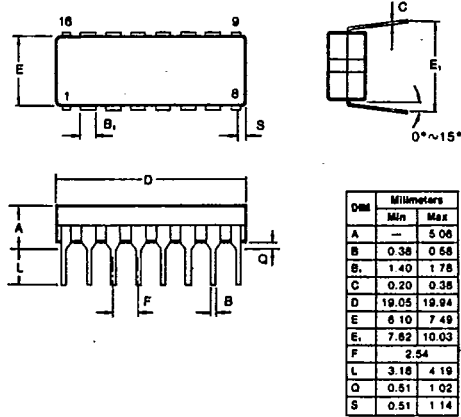
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**2. CERAMIC PACKAGES**

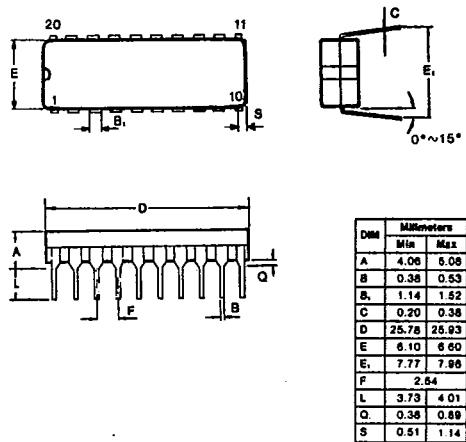
**14-Pin Ceramic DIP Units: mm**



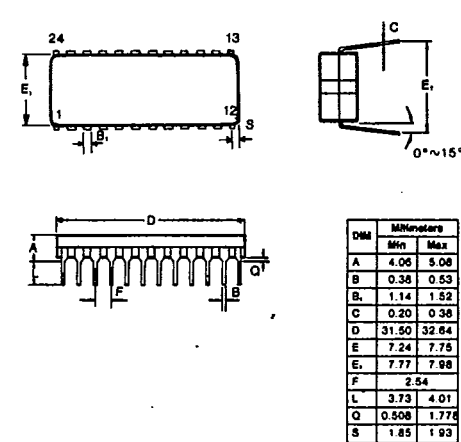
**16-Pin Ceramic DIP Units: mm**



**20-Pin Ceramic DIP Units: mm**



**24-Pin Ceramic DIP Units: mm**



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