

Product name MG7050HAN 100.000000MHz 2ACJAA

Product Number / Ordering code X1M0004310007xx

Please refer to the 10.Packing information about xx (last 2 digits)

Output waveform HCSL

Pb free / Complies with EU RoHS directive

Reference weight Typ. 163 mg

1. Absolute maximum ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	Vcc-GND	-0.5	-	40	V	-
Storage temperature	T_stg	-55	-	125	°C	Storage as single product
Input voltage	Vin	-0.5	-	Vcc+0.5	V	-

2. Specifications(characteristics)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f0		100.0000		MHz	2 output
Supply voltage	Vcc	2.97	3.3	3.63	V	-
Operating temperature	T_use	0	-	70	°C	-
Frequency tolerance	f_tol	-50	-	50	x10 ⁻⁶	T_use
Current consumption	Icc	-	60	90	mA	2-output OE=Vcc
Stand-by current	I_std	-	-	-	mA	-
Disable current	I_dis	-	12	25.0	mA	OE = GND
Symmetry	SYM	45	-	55	%	At output crossing point
Output voltage(HCSL)	VOH	0.66	-	0.85	V	-
	VOL	-0.15	-	0.15	V	-
Crossing voltage	VCR	0.25	-	0.55	V	-
Output load condition(LVDS)	L_HCSL	-	50	-	Ω	ZSEL = High
	Rs	-	33	-	Ω	ZSEL = High
	CL	-	2	-	pF	-
Input voltage	VIH	70%Vcc	-	-		OE and ZSEL terminals
	VIL	-	-	30%Vcc		
Rise time	t _r	1	-	4	V/ns	-0.15 V and 0.15 V of differential output
Fall time	t _f	1	-	4	V/ns	-0.15 V and 0.15 V of differential output
Start-up time	t_str	-	-	10	ms	Time at minimum supply voltage to be 0s
Jitter	t _{DJ}	-	-	N/A	ps	Deterministic Jitter
	T _{RJ}	-	-	N/A	ps	Random Jitter
	t _{RMS}	-	-	N/A	ps	σ(RMS of total distribution)
	t _{p-p}	-	-	N/A	ps	Peak to Peak
	t _{acc}	-	-	N/A	ps	Accumulated jitter
Phase jitter	t _{PJ}	-	0.16	0.3	ps	Offset Frequency: 12 kHz to 20 MHz
Phase noise	L(f)	-	-	-	dBc/Hz	Offset:1 Hz
		-	-61.8	-	dBc/Hz	Offset:10 Hz
		-	-90.9	-	dBc/Hz	Offset:100 Hz
		-	-120.5	-	dBc/Hz	Offset:1 kHz
		-	-148.0	-	dBc/Hz	Offset:10 kHz
		-	-153.4	-	dBc/Hz	Offset:100 kHz
-	-155.5	-	dBc/Hz	Offset:1 MHz		
Skew	t_skew	-	-	50	ps	ZSEL = H
Frequency aging	f_age	-	-	-	x10 ⁻⁶ /Year	Included in Frequency tolerance 10 years
		-	-	-		-

3. Test circuit

1) Measurement condition

(1) Oscilloscope

- Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).
- Probe ground should be placed closely from test point and lead length should be as short as possible.

(2) By-pass capacitor 1 (approx. 0.01 μF to 0.1 μF) places closely between Vcc and GND.

(3) By-pass capacitor 2 (approx. 10 μF) places closely between power supply terminals on the board.

(4) Output line length L is estimated as follows

$$L = \frac{0.1c}{f_o \sqrt{0.475\epsilon_r + 0.67}}$$

ϵ_r : Relative dielectric constant of the board

f_o : Output frequency

c : Velocity of light in a vacuum

(5) Use the current meter whose internal impedance value is small.

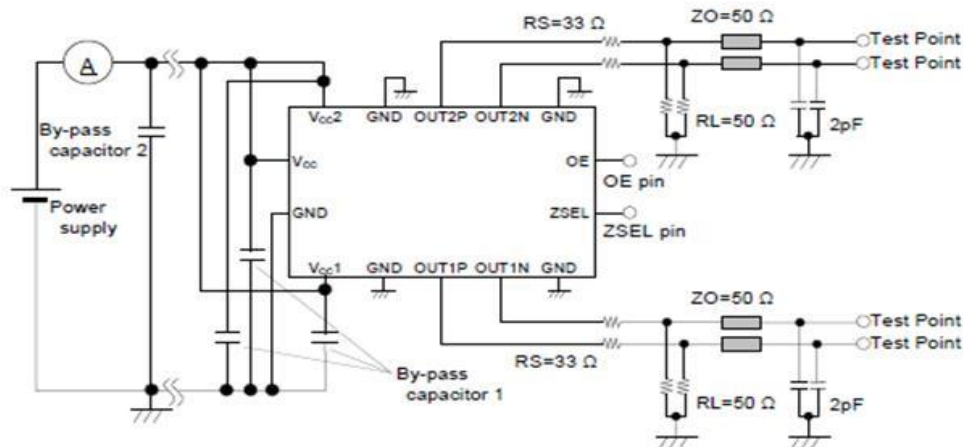
(6) Power supply

- Start up time (0 V \rightarrow 90 %Vcc) of power source should be more than 150 μs and slew rate should be less than 19.8 mV/ μs .
- Impedance of power supply should be as low as possible.

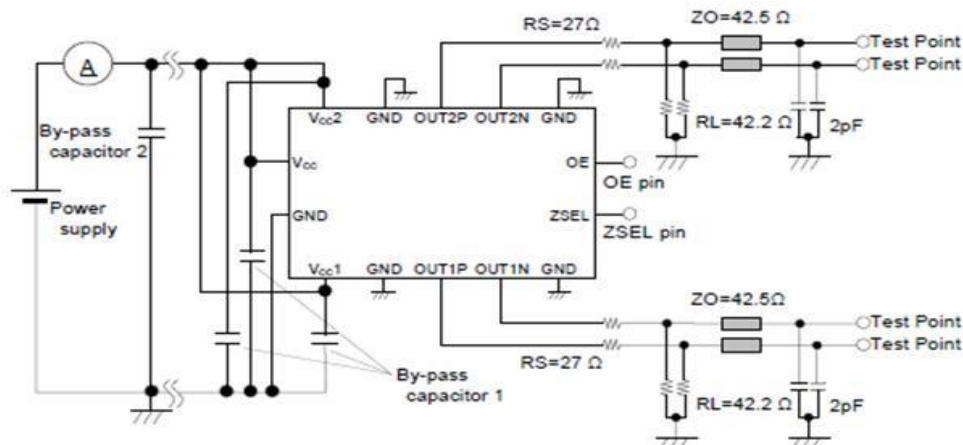
2) 2 output type

(1) To observe waveform and current

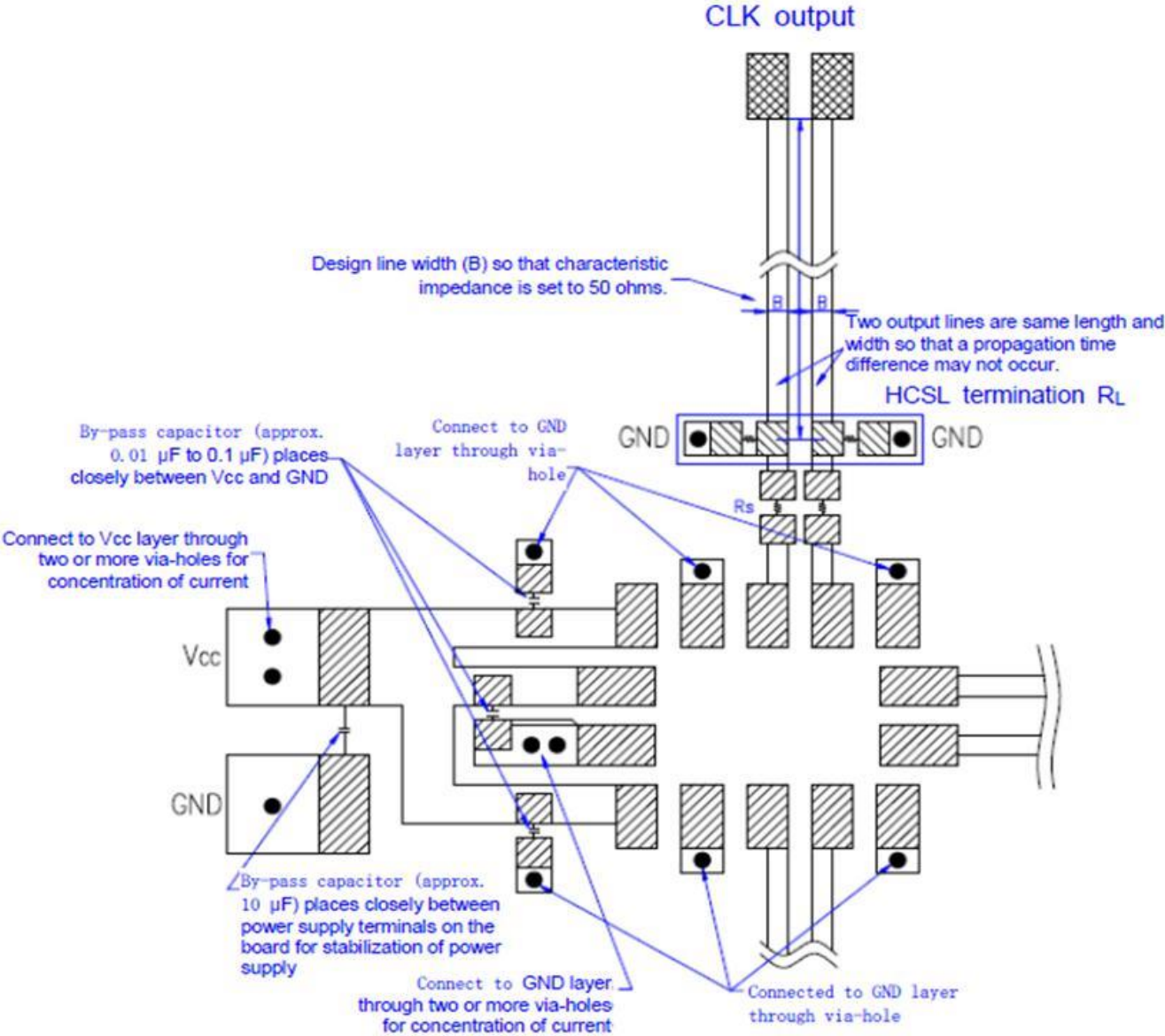
• Case of ZSEL=H ($R_S=33\ \Omega$ / $R_L=50\ \Omega$ / $Z_0=50\ \Omega$)



• Case of ZSEL=L ($R_S=27\ \Omega$ / $R_L=42.2\ \Omega$ / $Z_0=42.5\ \Omega$)



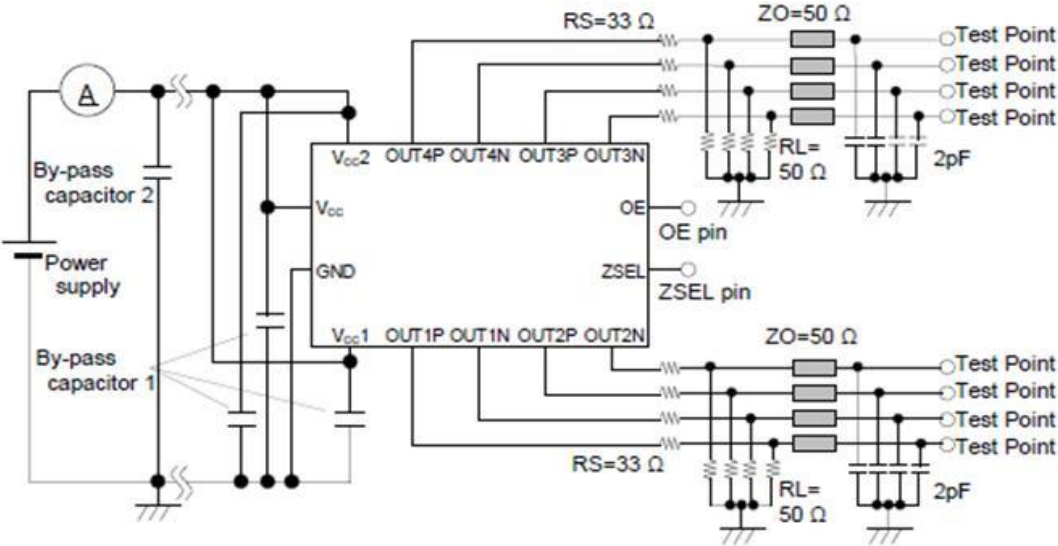
(2)PCB layout (multilayers, with Vcc and GND layer inside)



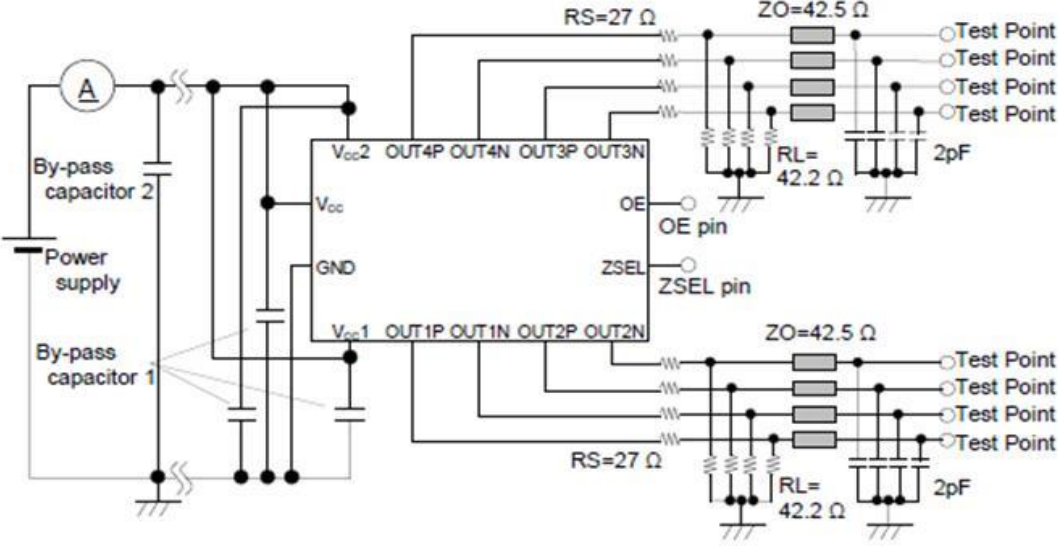
3) 4 output type

(1) To observe waveform and current

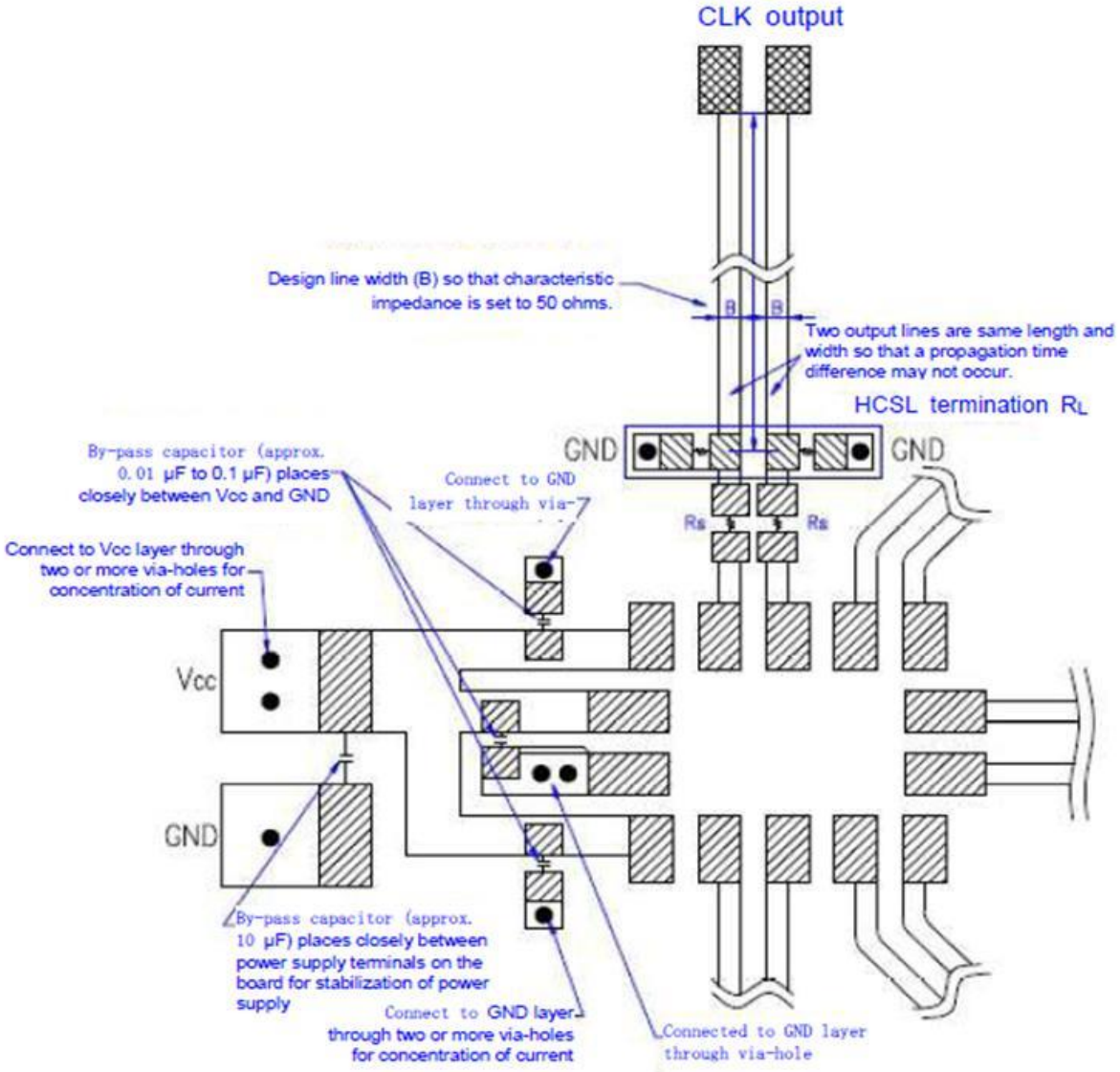
• Case of ZSEL=H ($R_S=33\Omega/R_L=50\Omega/ZO=50\Omega$)



• Case of ZSEL=H ($R_S=27\Omega/R_L=42.2\Omega/ZO=42.5\Omega$)

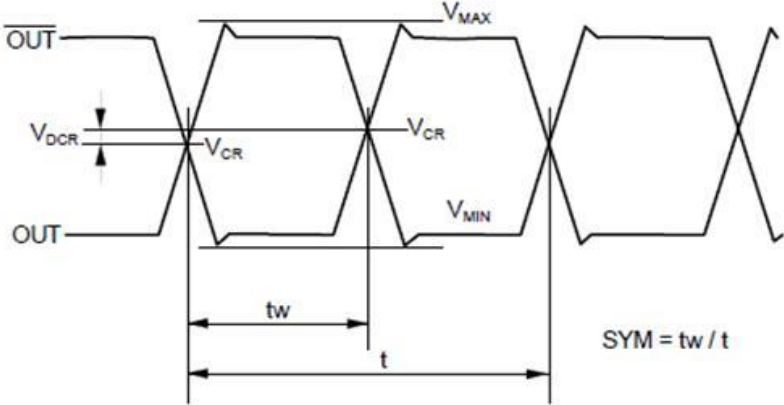


(2)PCB layout (multilayers, with Vcc and GND layer inside)

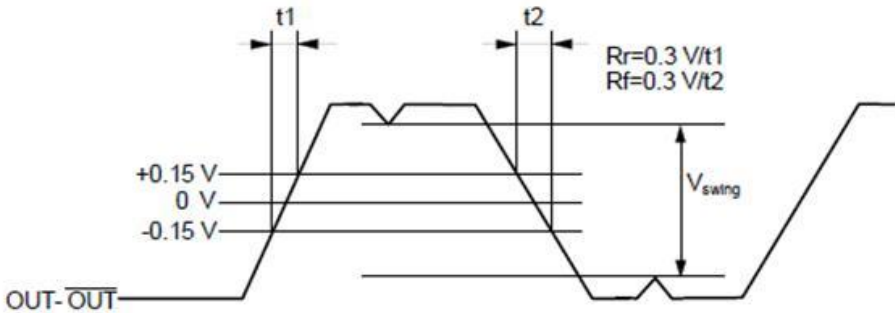


4. Timing chart

Each output waveform (OUT*P and OUT*N)

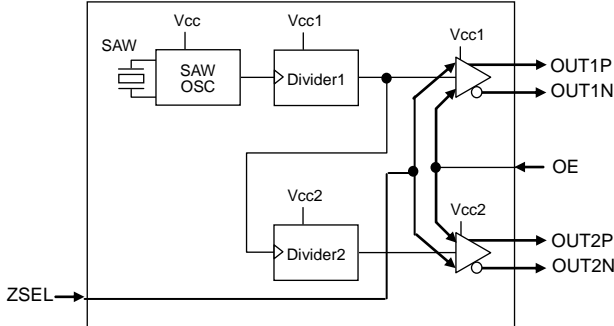


Differential output waveform (OUT*P - OUT*N)

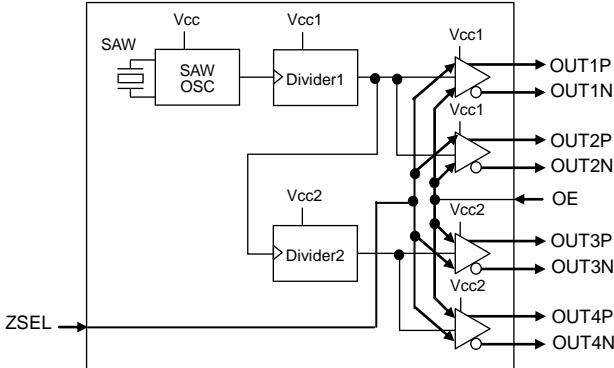


5. Block diagram

2 outputs



4 outputs



6. FSEL function

		Output line	HCSL load	Shunt resistor
		Differential Zo	L_HCSL	Rs
ZSEL	H	100 Ω	50 Ω	33 Ω
	L	85 Ω	42.2 Ω	27 Ω

7.External dimensions

(Unit: mm)

OE pin = "H" : Specified frequency output.
 OE pin = "L" : Output is high impedance
 #14 is connected to the cover.

Pin	Connections	
	2-outputs	4-outputs
1	Vcc1	
2	GND	OUT1P
3	OUT1P	OUT1N
4	OUT1N	OUT2P
5	GND	OUT2N
6	FSEL	
7	OE	
8	GND	OUT3N
9	OUT2N	OUT3P
10	OUT2P	OUT4N
11	GND	OUT4P
12	Vcc2	
13	Vcc	
14	GND	

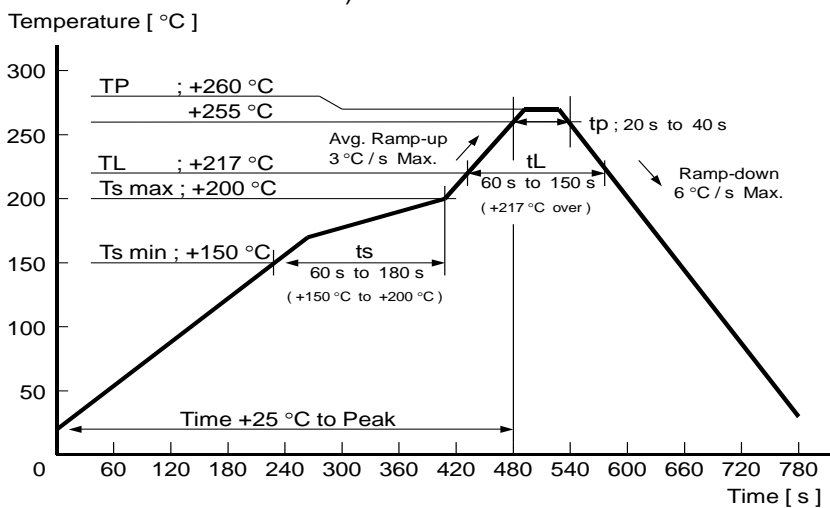
8.Footprint(Recommended)

(Unit: mm)

To maintain stable operation, provide a 0.01 μF to 0.1 μF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between V_{CC}, V_{CC1}, V_{CC2} - GND).

9.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.01)



10.Packing information

[1] Product number last 2 digits code(xx) description The recommended code is "00"

X1M0004310007xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	00	1000pcs / Reel
12	250pcs / Reel		

[2] Taping specification

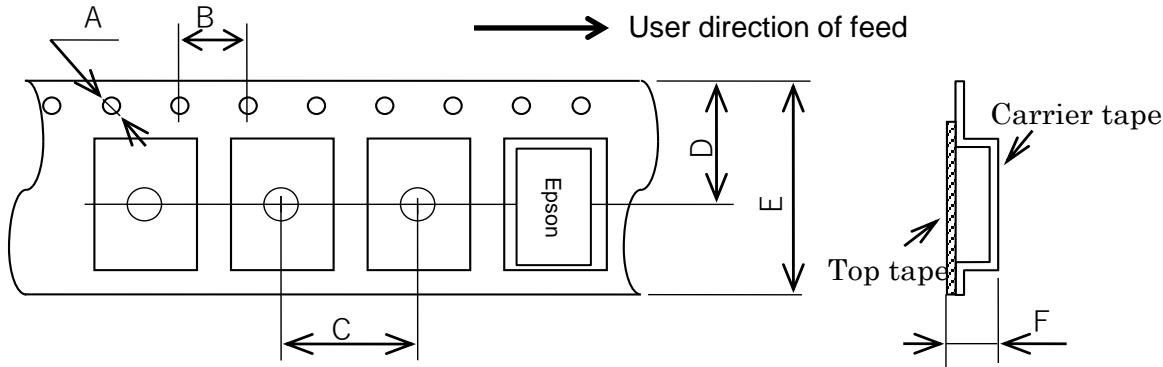
Subject to EIA-481 & IEC-60286

(1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm

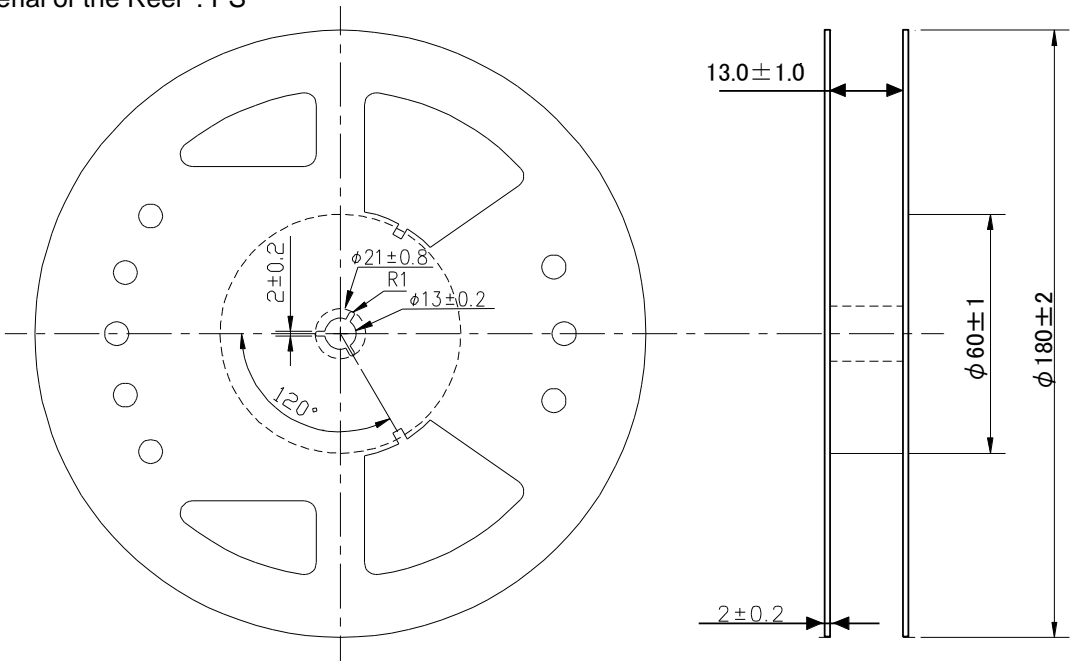


Symbol	A	B	C	D	E	F
Value	$\Phi 1.5$	4	8	9.25	16	2.3

(2) Reel dimensions

Center material : PS

Material of the Reel : PS



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