LM556-MIL Dual Timer

1 Features

- Direct Replacement for SE556/NE556
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Replaces Two 555 Timers
- Adjustable Duty Cycle
- Output Can Source or Sink 200 mA
- Output and Supply TTL-Compatible
- Temperature Stability Better Than 0.005% per °C
- Normally On and Normally Off Output

2 Applications

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Linear Ramp Generator

3 Description

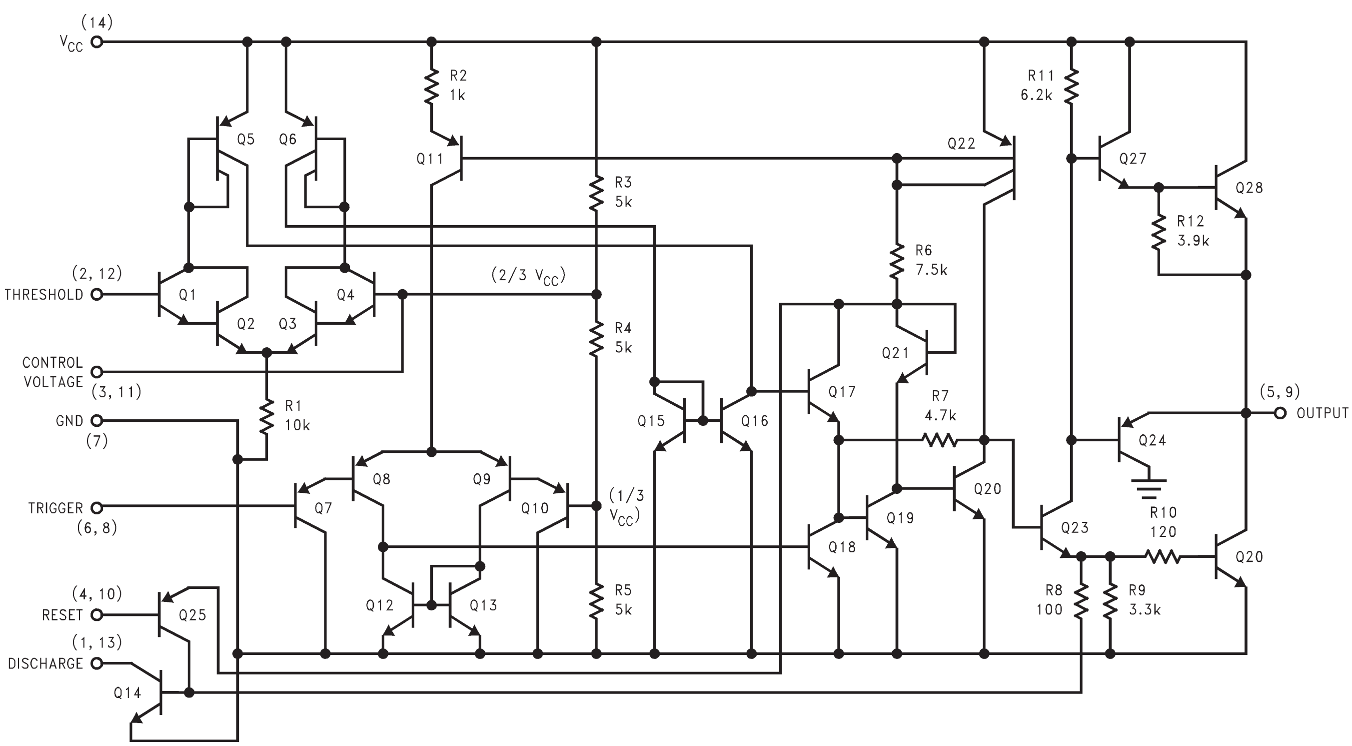
The LM556-MIL dual-timing circuit is a highly-stable controller capable of producing accurate time delays or oscillation. The LM556-MIL device is a dual-timing version of the LM555 device. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other, sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM556-MIL	SOIC (14)	3.91 mm × 8.65 mm
	PDIP (14)	6.35 mm × 19.177 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic Diagram



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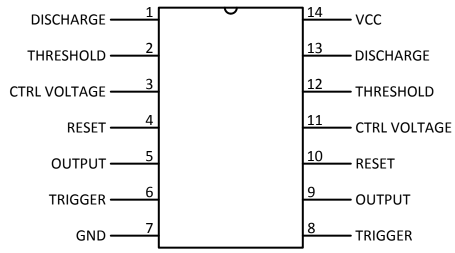
4 Revision History

DATE	REVISION	NOTES
June 2017	*	Initial release.

5 Pin Configuration and Functions

D or NFF Package
14-Pin SOIC or PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL VOLTAGE (Timer 0)	3	I	Controls the threshold and trigger levels. It determines the pulse width of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform.
CONTROL VOLTAGE (Timer 1)	11	I	Controls the threshold and trigger levels. It determines the pulse width of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform.
DISCHARGE (Timer 0)	1	I	Open collector output which discharges a capacitor between intervals (in phase with output). It toggles the output from high to low when voltage reaches 2/3 of supply voltage.
DISCHARGE (Timer 1)	13	I	Open collector output which discharges a capacitor between intervals (in phase with output). It toggles the output from high to low when voltage reaches 2/3 of supply voltage.
GND	7	O	Ground reference voltage
OUTPUT (Timer 0)	5	O	Output driven waveform
OUTPUT (Timer 1)	9	O	Output driven waveform
RESET (Timer 0)	4	I	Negative pulse applied to this pin to disable or reset the timer. When not used for reset purposes, it should be connected to Vcc to avoid false triggering.
RESET (Timer 1)	10	I	Negative pulse applied to this pin to disable or reset the timer. When not used for reset purposes, it should be connected to Vcc to avoid false triggering.
THRESHOLD (Timer 0)	2	I	Compares the voltage applied to the terminal with a reference voltage of 2/3 V_{CC}. The amplitude of voltage applied to this terminal is responsible for the set state of the flip-flop.
TRIGGER (Timer 0)	6	I	Responsible for transition of the flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin.
THRESHOLD (Timer 1)	12	I	Compares the voltage applied to the terminal with a reference voltage of 2/3 V_{CC}. The amplitude of voltage applied to this terminal is responsible for the set state of the flip-flop.
TRIGGER (Timer 1)	8	I	Responsible for transition of the flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin.
VCC	14	I	Supply voltage with respect to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

		MIN	MAX	UNIT
Supply voltage			18	V
Power dissipation[3]	LM556CM		410	mW
	LM556CN		1620	
Operating temperature, LM556C		0	70	°C
Soldering information	PDIP package soldering (10 seconds)		260	°C
	SOIC package vapor phase (60 seconds)		215	
	SOIC package infrared (15 seconds)		220	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(3) For operating at elevated temperatures the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 77°C/W (Plastic Dip), and 110°C/W (SO-14 Narrow).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	16	V
T_A	Operating free-air temperature	0	70	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM56-MIL D (SOIC) 14 PINS	LM556-MIL NFF (PDIP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.3	48.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.8	34.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.6	27.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.7	19.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.4	27.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, V_{CC} = 5 V to 15 V, unless otherwise specified

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply voltage				4.5		16	V
Supply current (each timer section)		V_{CC} = 5 V, R_L = ¥			3	6	mA
		V_{CC} = 15 V, R_L = ¥ (low state)(1)			10	14	
Timing error, monostable	Initial accuracy	R_A = 1 k to 100 kΩ, C = 0.1 μF(2)			0.75%		ppm/°C
	Drift with temperature				50		
	Accuracy over temperature				1.5%		
	Drift with supply				0.1		%/V
Timing error, astable	Initial accuracy	R_A, R_B = 1 k to 100 kΩ, C = 0.1 μF(2)			2.25%		
	Drift with temperature				150		ppm/°C
	Accuracy over temperature				3%		
	Drift with supply				0.30		%/V
Trigger voltage		V_{CC} = 15 V		4.5	5	5.5	V
		V_{CC} = 5 V		1.25	1.67	2	
Trigger current					0.2	1	µA
Reset voltage				0.4	0.5	1	V
Reset current					0.1	0.6	mA
Threshold current		V_{TH} = V-control(3)			0.03	0.1	µA
		V_{TH} = 11.2 V				250	nA
Control voltage level and threshold voltage		V_{CC} = 15 V		9	10	11	V
		V_{CC} = 5 V		2.6	3.33	4	
Pin 1, 13 leakage output high					1	100	nA
Pin 1, 13 sat output low(4)		V_{CC} = 15 V, I = 15 mA			180	300	mV
		V_{CC} = 4.5 V, I = 4.5 mA			80	200	
Output voltage drop (low)		V_{CC} = 15 V	I_{SINK} = 10 mA		0.1	0.25	V
			I_{SINK} = 50 mA		0.4	0.75	
			I_{SINK} = 100 mA		2	2.75	
			I_{SINK} = 200 mA		2.5		
		V_{CC} = 5 V, I_{SINK} = 5 mA			0.25	0.35	
Output voltage drop (high)		I_{SOURCE} = 200 mA, V_{CC} = 15 V			12.5		V
		I_{SOURCE} = 100 mA, V_{CC} = 15 V		12.75	13.3		
		V_{CC} = 5 V		2.75	3.3		
Rise time of output					100		ns
Fall time of output					100		ns
Matching characteristics	Initial timing accuracy	See (5)			0.1%	2%	ppm/°C
	Timing drift with temperature				±10		
	Drift with supply voltage				0.2	0.5	%/V

(1) Supply current when output high typically 1 mA less at V_{CC} = 5 V.
(2) Tested at V_{CC} = 5 V and V_{CC} = 15 V.
(3) This will determine the maximum value of R_A + R_B for 15-V operation. The maximum total (R_A + R_B) is 20 MΩ.
(4) No protection against excessive pin 1, 13 current is necessary providing the package dissipation rating will not be exceeded.
(5) Matching characteristics refer to the difference between performance characteristics of each timer section.

6.6 Typical Characteristics

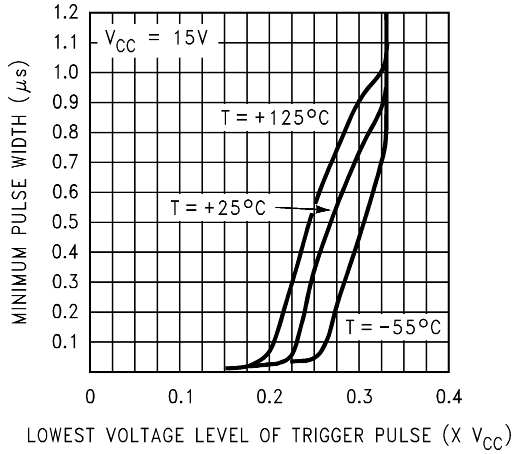


Figure 1. Minimum Pulse Width Required for Triggering

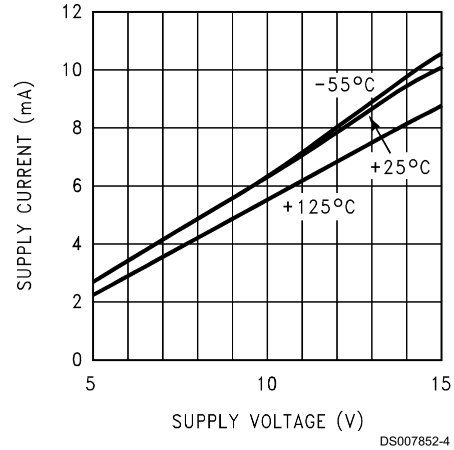


Figure 2. Supply Current vs Supply Voltage (Each Section)

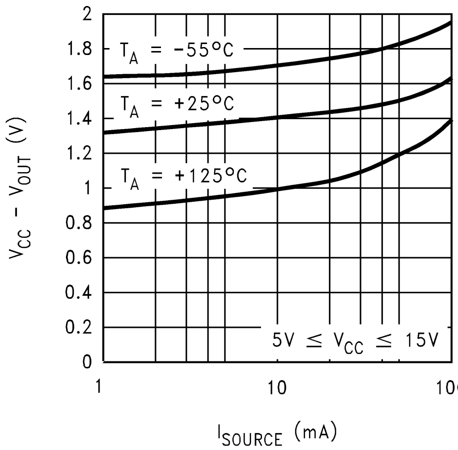


Figure 3. High Output Voltage vs Output Source Current

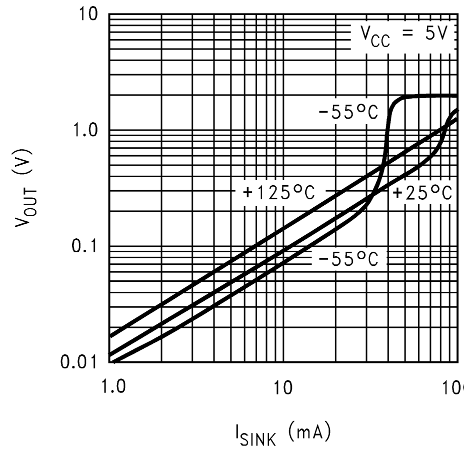


Figure 4. Low Output Voltage vs Output Sink Current

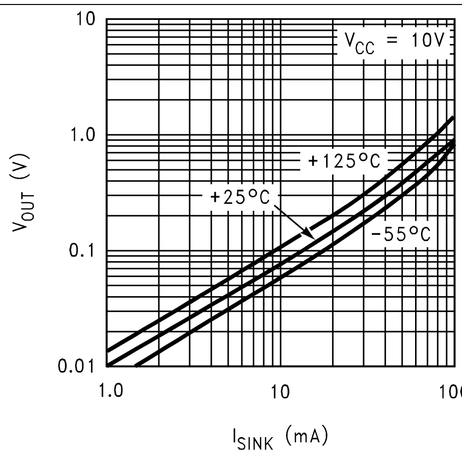


Figure 5. Low Output Voltage vs Output Sink Current

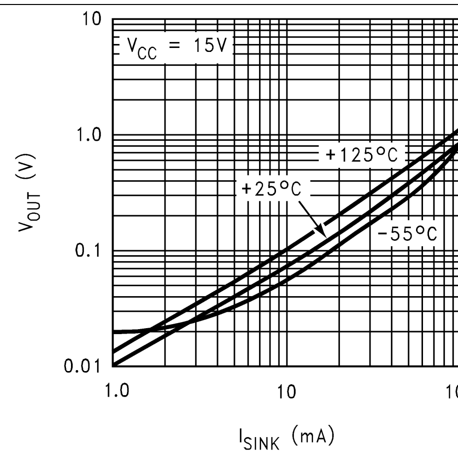


Figure 6. Low Output Voltage vs Output Sink Current

Typical Characteristics (continued)

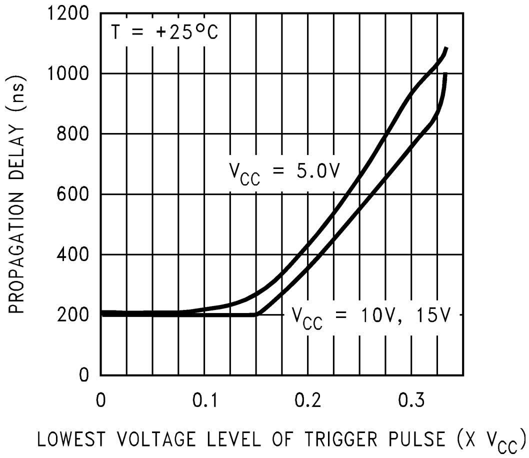


Figure 7. Output Propagation Delay vs Voltage Level of Trigger Pulse

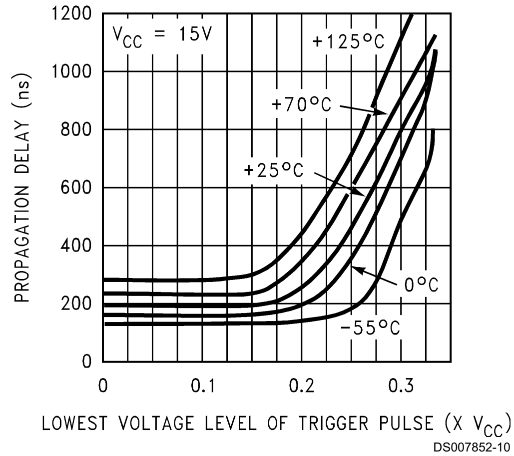


Figure 8. Output Propagation Delay vs Voltage Level of Trigger Pulse

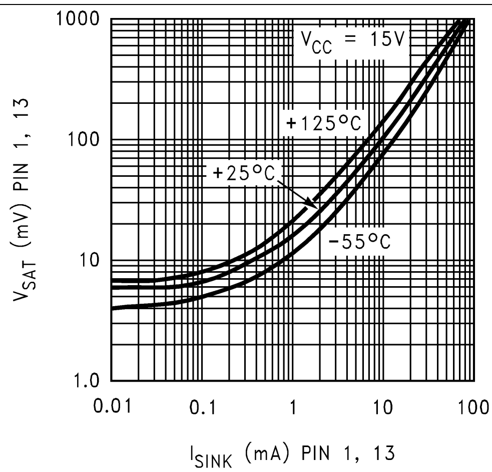


Figure 9. Discharge Transistor (Pin 1, 13) Voltage vs Sink Current

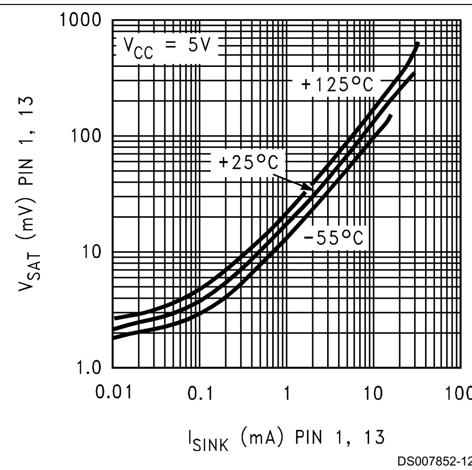


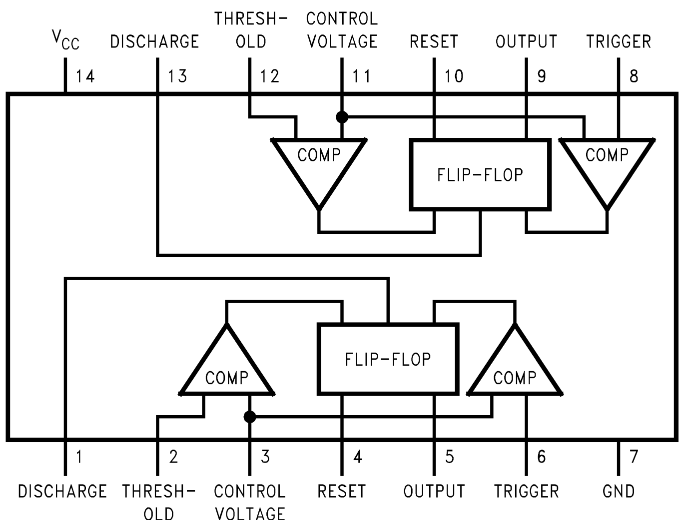
Figure 10. Discharge Transistor (Pin 1, 13) Voltage vs Sink Current

7 Detailed Description

7.1 Overview

The LM556-MIL dual-timing circuit is a highly stable device for generating accurate time delays or oscillations. The two timers operate independently from one another, only sharing V_{CC} and ground. For each individual timer, additional terminals are provided for triggering or resetting. In the monostable mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable mode operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms and the output circuit can source or sink up to 200 mA.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The LM556-MIL is specified for operation from 4.5 V to 16 V. Many of the specifications apply from 0ºC to 70ºC. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Electrical Characteristics* and *Typical Characteristics* sections.

7.3.2 Timing from Microseconds Through Hours

The LM556-MIL has the ability to have timing parameters from the microseconds range to hours. The time delay of the system can be determined by the time constant of the R and C values used for either the monostable or astable configuration. A nomograph is available for easy determination of R and C values for various time delays.

7.4 Device Functional Modes

The LM556-MIL can operate in both astable and monostable mode depending on the application requirements.

7.4.1 Monostable Mode

The LM556-MIL timer acts as a one-shot pulse generator. The pulse begins when the LM556-MIL timer receives a signal at the trigger input that falls below 1/3 of the voltage supply. The width of the output pulse is determined by the time constant of an RC network. The output pulse ends when the voltage on the capacitor equals 2/3 of the supply voltage. The output pulse width can be extended or shortened depending on the application by adjusting the R and C values. More details are given in the LM555 datasheet (SNAS548).

Device Functional Modes (continued)

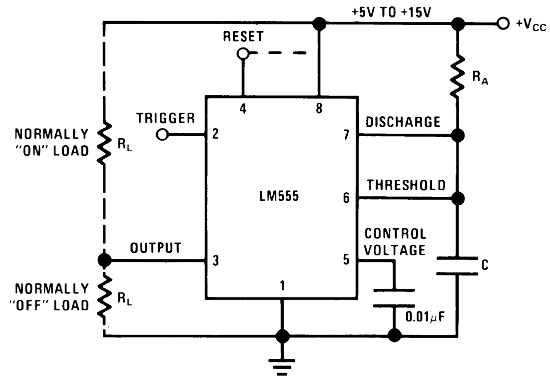


Figure 11. Monostable

7.4.2 Astable (Free-Running) Mode

The LM556-MIL timer can operate as an oscillator and puts out a continuous stream of rectangular pulses having a specified frequency. The frequency of the pulse stream depends on the values of RA, RB, and C. Again, more details are given in the LM555 datasheet (SNAS548).

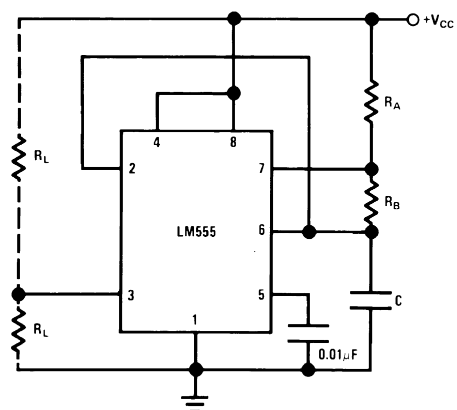


Figure 12. Astable

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM556-MIL timer can be used in various configurations. A typical application for the LM556-MIL timer in astable mode is to drive an audio device (such as a beeper) to provide a pulsed sound. This simple application can be modified to fit any application requirement.

8.2 Typical Application

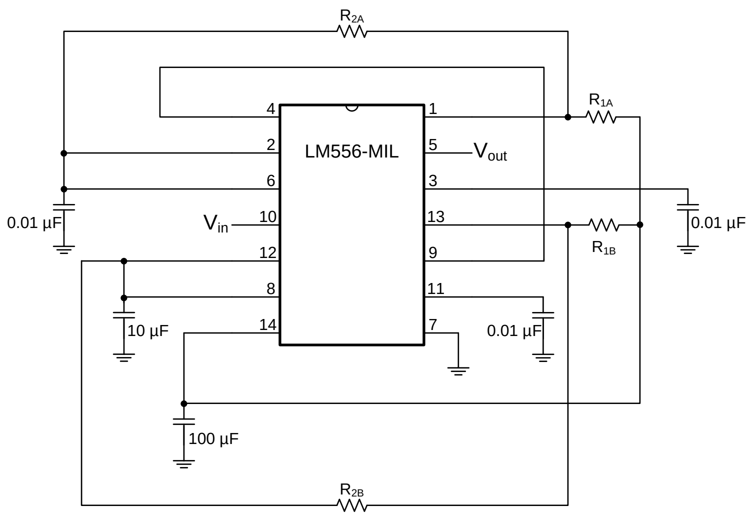


Figure 13. Typical Application

8.2.1 Design Requirements

The main design requirements for this application require setting one of the timers (Timer A in this case) to the same resonant frequency as the piezo transducer which can be set by choosing R_{1A}, R_{2A}, and C_A with Equation 1:

$$f_o = \frac{1.44}{((R_{1A} + 2R_{2A})C)} \quad (1)$$

The other design choice is to decide how often and long to produce the bleeping sound. This can be set by choosing R_{1B} and R_{2B} of Timer B (acts as the reset button for Timer A) with Equation 2:

$$D = \frac{R_{2B}}{R_{1B} + R_{2B}} \quad (2)$$

Other useful design equations like Equation 3 and Equation 4 are given below where t_h represents the time it takes to charge the capacitor of each individual timer and t_l represents the time it takes to discharge the capacitor.

Typical Application (continued)

$$t_h = 0.693(R_1 + R_2)C$$

where

- t_h represents the time it takes to charge the capacitor of each individual timer (3)

$$t_l = 0.693R_2C$$

where

- t_l represents the time it takes to discharge the capacitor. (4)

8.2.2 Detailed Design Procedure

Given that the resonant frequency of the piezo transducer is about 3 kHz, by choosing R_1, C and using Equation 1, R_2 can be determined to be 23.5 kΩ.

In order to have the sound be audible for half the period, the duty cycle for the triggering timer should be 50%. However, this is difficult to achieve because the recommended minimum value for R_1 is 1 kΩ. Therefore, a duty cycle of 49% was chosen for this application. By choosing R_1 to be 1 kΩ and using Equation 2, R_2 is found to be 24.5 kΩ.

8.2.3 Application Curve

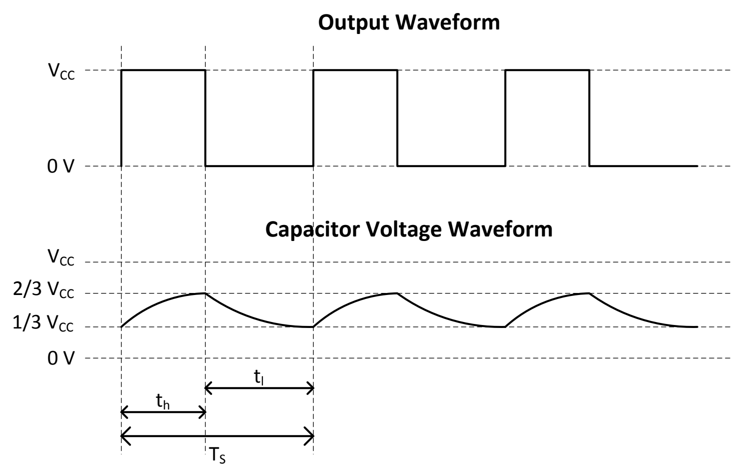


Figure 14. Capacitor Voltage and Output Waveforms in Astable Mode

9 Power Supply Recommendations

The LM556-MIL requires a voltage supply within 4.5 V to 16 V. Adequate power supply bypassing is necessary to protect associated circuitry. The minimum recommended capacitor value is 0.1 µF in parallel with a 1-µF electrolytic capacitor. Place the bypass capacitors as close as possible to the LM556-MIL and minimize the trace length

CAUTION

Supply voltages larger than 18 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

10 Layout

10.1 Layout Guidelines

Standard PCB rules apply to routing the LM556-MIL. The parallel combination of a 0.1-µF capacitor and a 1-µF electrolytic capacitor should be as close as possible to the LM556-MIL. The capacitor used for the time delay should also be placed as close as possible to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

10.2 Layout Example

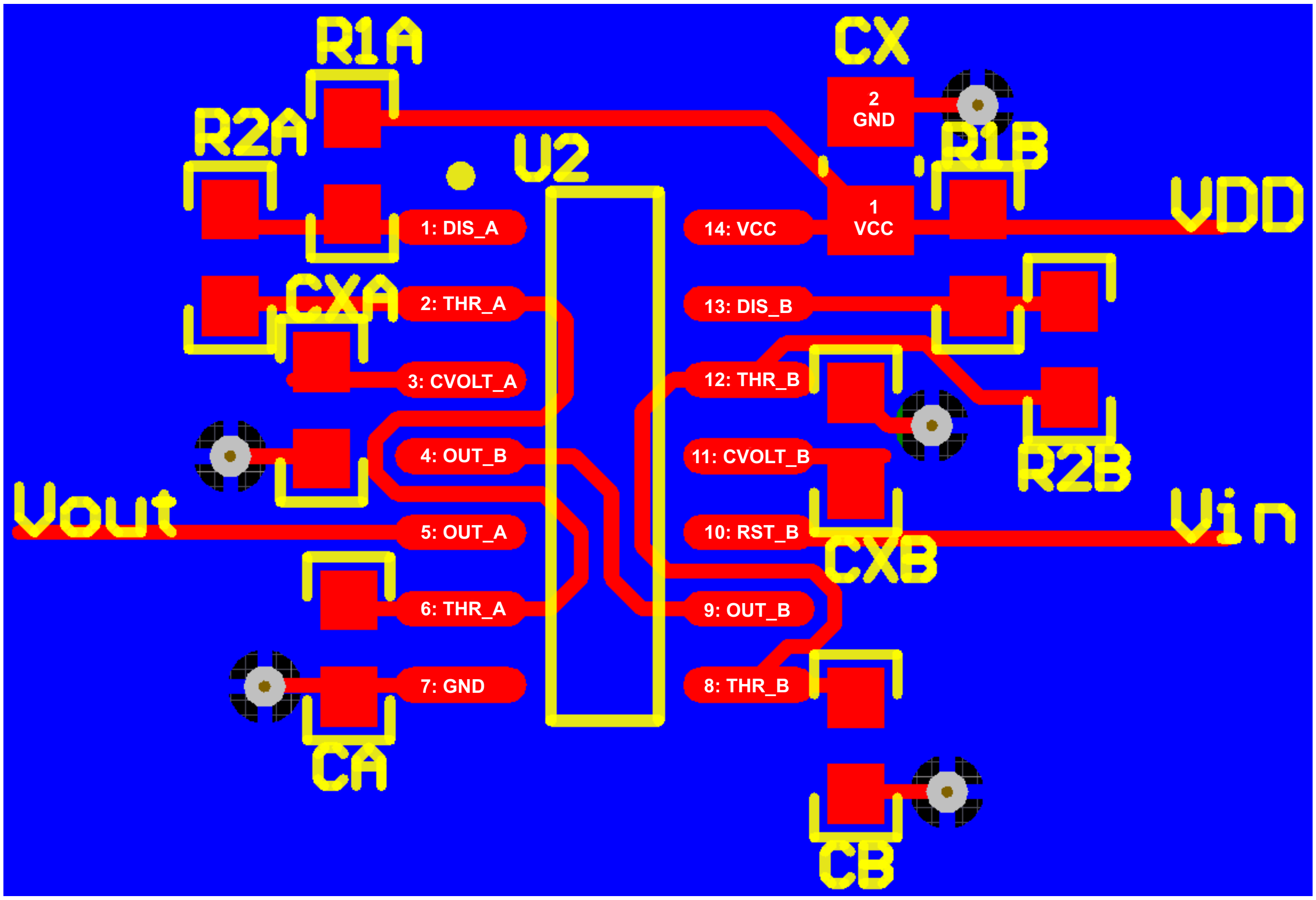


Figure 15. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

LM555 Timer, SNAS548

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM556 MD8	NRND	DIESALE	Y	0	324	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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