Low Cost, Single & Multi-Channel, Voltage-to-Frequency Converters

Preliminary Technical Data — AD7741/42

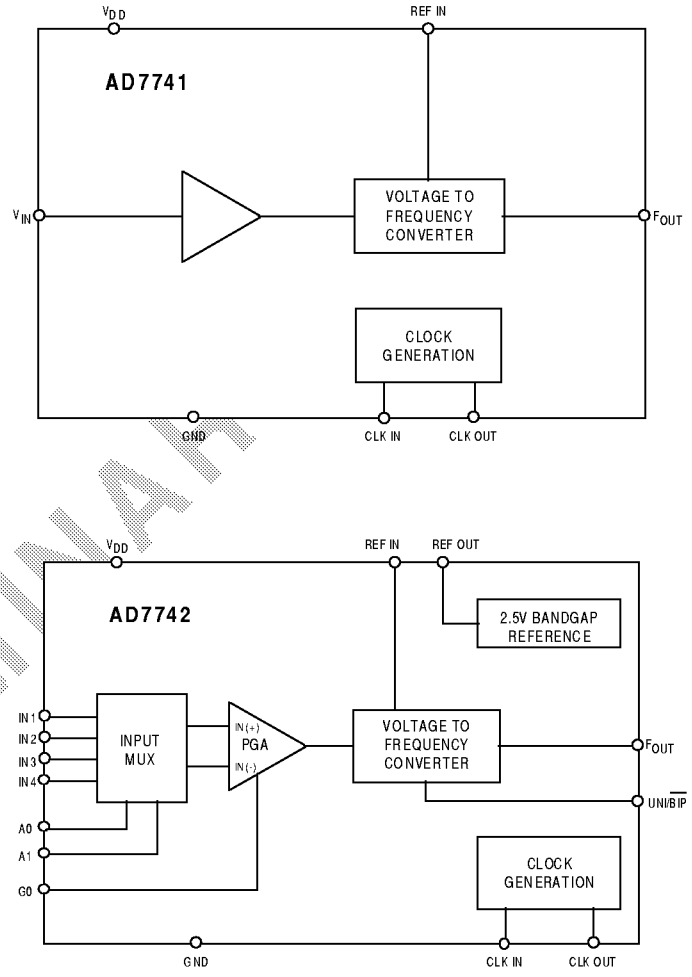
FEATURES

Synchronous Operation
Full-Scale Frequency (up to 3MHz) Set by External System Clock
F_{OUT} (max) = 45% of F_{CLOCK}
Low Nonlinearity:0.1% at F_{OUT} = 3MHz
Single +5V Supply Operation
Buffered Inputs
AD7741: Single-ended input
AD7742: 3 Pseudo-Differential inputs,
OR 2 Fully Differential inputs
Programmable Gain Front End
Selectable via Gain Select pin
On-chip +2.5V Reference Voltage (AD7742)
Internal/External Reference Option (AD7742)
No user trims required to achieve specified performance
Low Cost
Input Signal Ranges:
AD7741: 0V to +REF IN
AD7742: Unipolar: 0V to +REF IN/Gain
Bipolar: -REF IN/Gain to +REF IN/Gain
Minimum Number of External Components required
AD7741: 8-Pin DIP, 8-Lead 0.15" wide SOIC packages
AD7742: 16-Pin DIP, 16-Lead 0.15" wide SOIC packages

APPLICATIONS

Low Cost A/D Conversion
Common-Mode Voltage Isolation

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The AD7741 and AD7742 are a new generation of synchronous Voltage-to-Frequency Converters (VFC's). The AD7741 is a single-ended version in a small 8-pin DIP/SOIC package and the AD7742 is a multi-channel version in a 16-pin DIP/SOIC package. Small package, low cost, ease of use plus no user trims required to achieve specified performance were major design goals for these products.

The AD7742 contains an internal +2.5 V bandgap reference and offers two differential inputs or three pseudo-differential inputs. The AD7742 also allows the user the choice of pin-programming the channel and gain settings.

The AD7741 accepts a single-ended analog input range from 0 V to +REF IN and the AD7742 accepts differential analog input ranges from -REF IN to +REF IN. Both parts operate from a single +5 V supply consuming only 30 mW.

PRODUCT HIGHLIGHTS

1. The AD7741 is a single channel, single-ended VFC. It is available in an 8-pin DIP and in an 0.15" wide 8-lead SOIC package.
2. The AD7742 is a multi-channel VFC whose internal settings (PGA & Channel Select) can be pin selected by tying certain package pins high or low. It is available in a 16-pin DIP and in an 0.15" wide 16-lead SOIC package.
3. Low Power, Single Supply Operation
The AD7741 and AD7742 operate from a single +5 V supply and consume only 30 mW.

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(V_{DD} = +5 V± 5%, External Reference = +2.5 V; F_{CLK} = 5MHz; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	B Versions[1]	Y Versions[1]	Units	Test Conditions/Comments
ACCURACY				
Linearity Error				
F_{CLK} = 200 kHz	±0.1	±0.1	% of Span max.	
F_{CLK} = 2 MHz	±0.1	±0.1	% of Span max.	
F_{CLK} = 5 MHz	±0.1	±0.1	% of Span max.	
Power Supply Rejection Ratio	0.01	0.01	%/V max	
Offset Error	TBD	TBD	µV max.	
Offset Error Drift	TBD	TBD	µV /°C typ.	
Gain Error	±0.5	±0.5	% of Span max.	
Gain Error Drift	TBD	TBD	ppm/°C typ.	
ANALOG INPUT				
Input Current	±1.0	±1.0	nA typ	100nA max
Input Voltage Range	0V to +REF IN	0V to +REF IN	Volts	
VOLTAGE REFERENCE				
REF IN				
Input Voltage	2.5	2.5	V nom	
Input Impedance	TBD	TBD	kΩtyp	
LOGIC OUTPUT (F_{OUT})				
Output High Voltage, V_{INH}	4.0	4.0	V min	I_{SOURCE} = 800 µA except for CLK_{OUT}
Output Low Voltage, V_{INL}	0.4	0.4	V max	I_{SINK} = 1.6 mA except for CLK_{OUT}
Output Frequency	$0.05F_{CLOCK}$	$0.05F_{CLOCK}$	kHz min	V_{IN}=0V
	$0.45F_{CLOCK}$	$0.45F_{CLOCK}$	kHz max	V_{IN}=+REF IN
LOGIC INPUTS[3]				
ALL INPUTS EXCEPT CLK_{IN}				
Input High Voltage, V_{INH}	2.0	2.0	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	10	pF typ	
CLK_{IN} ONLY				
Input High Voltage, V_{INH}	3.5	3.5	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	10	pF typ	
CLOCK FREQUENCY				
F_{CLKIN}	100	100	kHz min	For Specified performance
	5	5	MHz max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
I_{DD}	8	8	mA max	V_{DD} = 5V± 5%
Power Dissipation	40	40	mW max	Typically 30mW

NOTES
[1]Temperature Ranges are as follows: B Version, –40°C to +85°C; Y Version, –40°C to +105°C.
[2]See Terminology.
[3]Guaranteed by design and characterization, not production tested
Span = Maximum output frequency - Minimum output frequency
Specifications subject to change without notice.

AD7742-PRELIMINARY SPECIFICATIONS

(V_{DD} = +5 V ± 5%, External Reference = +2.5 V; F_{CLK} = 5MHz; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	B Versions[1]	Y Versions[1]	Units	Test Conditions/Comments
ACCURACY				
Linearity Error				
F_{CLK} = 200 kHz	±0.1	±0.1	% of Span max.	
F_{CLK} = 2 MHz	±0.1	±0.1	% of Span max.	
F_{CLK} = 5 MHz	±0.1	±0.1	% of Span max.	
Channel-to-Channel Isolation	TBD	TBD	dB typ	V_{IN} ?=kHz
Power Supply Rejection Ratio	0.01	0.01	%/V max	
Unipolar Offset Error	TBD	TBD	µV max.	
Unipolar Offset Error Drift	TBD	TBD	µV/°C typ.	
Unipolar Gain Error	±0.5	±0.5	% of Span max.	
Unipolar Gain Error Drift	TBD	TBD	ppm/°C typ.	
Bipolar Offset Error	±100	±100	µV max.	
Bipolar Zero Error	TBD	TBD	µV max.	
Bipolar Gain Error	±0.5	±0.5	% of Span max.	
CMR	TBD	TBD	dB	
ANALOG INPUT				
Input Current	±1.0	±1.0	nA typ	100nA max.
Common Mode Range[4]	-300mV to V_{DD} - 2V	-300mV to V_{DD} - 2V	Volts	
Differential Input Voltage Range	±REF/Gain	±REF/Gain	Volts	Bipolar Input Range
	0 to REF/Gain	0 to REF/Gain	Volts	Unipolar Input Range
VOLTAGE REFERENCE				
REF IN				
Input Voltage	2.5	2.5	V nom	
Input Impedance	TBD	TBD	kΩ typ	
REF OUT				
Output Voltage Accuracy	2.4/2.6	2.4/2.6	V min/V max	
Output Temp Coeff	100	100	ppm/°C typ	
Line Regulation	TBD	TBD	µV/V max	
Load Regulation	TBD	TBD	µV/mA max	
Noise (0.1 Hz - 10 Hz)	TBD	TBD	µV (p-p) typ	
Output Resistance	100	100	kΩ typ	
Output Capacitance	TBD	TBD	pF typ	
LOGIC OUTPUT (F_{OUT})				
Output High Voltage, V_{INH}	4.0	4.0	V min	I_{SOURCE} = 800 µA except for CLK_{OUT}
Output Low Voltage, V_{INL}	0.4	0.4	V max	I_{SINK} = 1.6 mA except for CLK_{OUT}
Output Frequency	$0.05F_{CLOCK}$	$0.05F_{CLOCK}$	kHz min	V_{IN}=0V (Unipolar)
				V_{IN}=-REF IN/Gain (Bipolar)
	$0.45F_{CLOCK}$	$0.45F_{CLOCK}$	kHz max	V_{IN}=+REF IN/Gain (Unipolar)
				V_{IN}=+REF IN/Gain (Bipolar)
LOGIC INPUTS[3]				
ALL INPUTS EXCEPT CLK_{IN}				
Input High Voltage, V_{INH}	2.0	2.0	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	10	pF typ	
CLK_{IN} ONLY				
Input High Voltage, V_{INH}	3.5	3.5	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	10	pF typ	
CLOCK FREQUENCY				
F_{CLKIN}	100	100	kHz min	For Specified performance
	5	5	MHz max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
I_{DD}	8	8	mA max	V_{DD} = 5V± 5%
Power Dissipation	40	40	mW max	Typically 30mW

NOTES

[1]Temperature Ranges are as follows: B Version, –40°C to +85°C; Y Version, –40°C to +105°C.

[2]See Terminology.

[3]Guaranteed by design and characterization, not production tested.

[4]The absolute input voltage on the different input pins must not go more positive than Vdd - 2V or more negative than GND - 400mV. The common-mode voltage applies to those inputs which form differential pairs.

Span = Max output frequency - Min output frequency

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2]

(V_{DD} = +5 V ± 5%, External Reference = +2.5 V; F_{CLOCK} = 5MHz; All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
F_{CLOCK}	100	kHz min	Clock Frequency
	5	MHz max	
t_{HIGH}/t_{LOW}	45/55	min	Clock Mark / Space Ratio
	55/45	max	
t_1	9	ns typ	CLK Edge to F_{OUT} Edge Delay
t_2	TBD	ns typ	F_{OUT} Rise Time
t_3	TBD	ns typ	F_{OUT} Fall Time

NOTES
[1]Sample tested at +25°C to ensure compliance.
[2]See Figure 1.
Specifications subject to change without notice

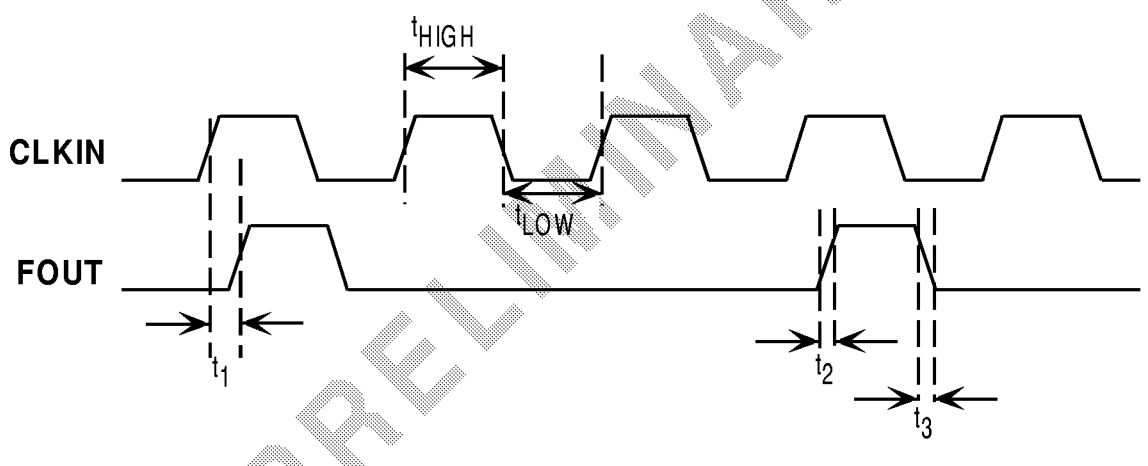


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

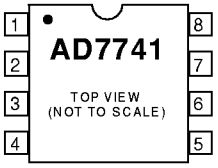
(T_A = +25°C unless otherwise noted)

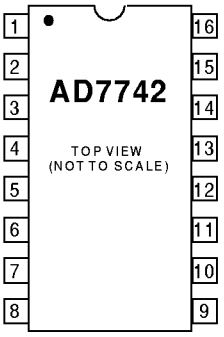
V_{DD} to GND ..... -0.3 V to +7 V
Analog Input Voltage to GND ..... -5 V to +7V
Reference Input Voltage to GND ..... -0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND ..... -0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (B Version) ..... -40°C to +85°C
  Automotive (Y Version) ..... -40°C to +105°C
  Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package
  Power Dissipation (8-pin DIP) ..... 520 mW
  Power Dissipation (16-pin DIP) ..... 550 mW
  θ_{JA} Thermal Impedance (8-pin DIP) ..... 125°C/W
  θ_{JA} Thermal Impedance (16-pin DIP) ..... 117°C/W
  Lead Temperature (Soldering, 10 sec) ..... +260°C
SOIC Package
  Power Dissipation (8-Lead) ..... 290 mW
  Power Dissipation (16-Lead) ..... 360 mW
  θ_{JA} Thermal Impedance (8-Lead) ..... 157°C/W
  θ_{JA} Thermal Impedance (16-Lead) ..... 125°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION

DIP and SOIC





AD7741/42 ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7741BN	-40°C to +85°C	N-8
AD7741YR	-40°C to + 105°C	R-8
AD7742BN	-40°C to +85°C	N-16
AD7742YR	-40°C to + 105°C	R-16A

*N = Plastic DIP, R = Small Outline IC (SOIC).

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD7741 PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Description
	V_{DD}	Positive supply voltage, +5 V ± 5%.
	GND	Analog Ground. Ground reference for Programmable Gain Amplifier, Voltage-to-Frequency Con verter and Bandgap Reference.
	CLKOUT	External Clock Output. When the master clock for the device is a crystal, the crystal is connected between CLKIN and CLKOUT. When an external clock is applied to CLKIN, CLKOUT provides an inverted clock signal. This clock must be buffered before being used to provide a clock source for a microprocessor, ADC or other system components.
	CLKIN	External Clock Input. The master clock for the device can be provided in the form of a crystal or an external clock. A crystal can be tied across the CLKIN, CLKOUT pins. Alternatively, the CLKIN pin can be driven with a CMOS-compatible clock and CLKOUT left unconnected. The frequency on CLK IN can be as high as 5MHz.
	REF IN	Voltage Reference Input. A precision reference (e.g. REF192) is applied to this pin.
	V_{IN}	Analog Input Channel. The analog input range is from 0V to REF IN. An input signal equal to 0V results in an output frequency of F_{OUT} min (5% of F_{CLOCK}) and an input of REF IN results in an output frequency of F_{OUT} max (45% of F_{CLOCK}).
	F_{OUT}	Frequency Output.

AD7742 PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Description
	F_{OUT}	Frequency Output
	V_{DD}	Positive supply voltage, +5 V ± 5%.
	GND	Analog Ground.
	A1	Channel Select Input. This is used as a channel select input in conjunction with A0 to select one of four possible input channel configurations allowable.
	A0	Channel Select Input. This is used as a channel select input in conjunction with A1 to select one of four possible input channel configurations allowable.
	CLKOUT	External Clock Output. When the master clock for the device is a crystal, the crystal is connected between CLKIN and CLKOUT. When an external clock is applied to CLKIN, CLKOUT provides an inverted clock signal. This clock must be buffered before being used to provide a clock source for a microprocessor, ADC or other system components.
	CLKIN	External Clock Input. The master clock for the device can be provided in the form of a crystal or an external clock. A crystal can be tied across the CLKIN, CLKOUT pins. Alternately, the CLKIN pin can be driven with a CMOS-compatible clock and CLKOUT left unconnected. The frequency on CLK IN can be as high as 5MHz.
	UNI/BIP	Unipolar/BIPOLAR Input Select. This pin determines whether the device is to operate with differential bipolar input signals (common mode range: -300mV to (V_{DD}-2V)) or whether the differential analog input signals are always positive. With UNI/BIP high, a differential analog input signal equal to 0 V results in an output frequency of F_{OUT} min (5% of F_{CLOCK}) and an input of REF IN/Gain results in an output frequency of F_{OUT} max (45% of F_{CLOCK}). With UNI/BIP low, a differential analog input signal of -REF IN/Gain results in an output frequency of F_{OUT} min (5% of F_{CLOCK}) and an input of +REF IN/Gain results in an output frequency of F_{OUT} max (45% of F_{CLOCK}).
	REFOUT	Voltage Reference Output. A +2.5V reference is provided at this pin. This reference can be tied directly to REF IN. It can also be used to drive external circuitry if it is buffered first.
	REFIN	Voltage Reference Input. This defines the span of the VFC. For specified operation a +2.5 V reference is required at this pin. It can be tied to REF OUT directly or, if a precision reference is available, it can be applied to this pin.
	IN1	Analog Input Channel 1. This is either a pseudo-differential input with respect to IN4 or it is the positive input of a differential analog input pair when used with IN2 (See Table I). In bipolar mode the differential analog input voltage range is ±REF IN /Gain of the PGA. In unipolar mode the differential analog input voltage range is 0 to +REF IN /Gain.
	IN2	Analog Input Channel 2. This is either a pseudo-differential input with respect to IN4 or it is the negative input of a differential analog input pair when used with IN1 (See Table I).
	IN3	Analog Input Channel 3. This is the positive input of a differential analog input pair when used with IN4 (See Table I).
	IN4	Analog Input Channel 4. This is either the common input for pseudo-differential inputs on IN1 and IN2 or it is the negative input of a analog input pair when used with IN3 (See Table I).
	G0	Gain Select Input. This is used as a gain select input for the PGA to select one of two gains for the PGA.

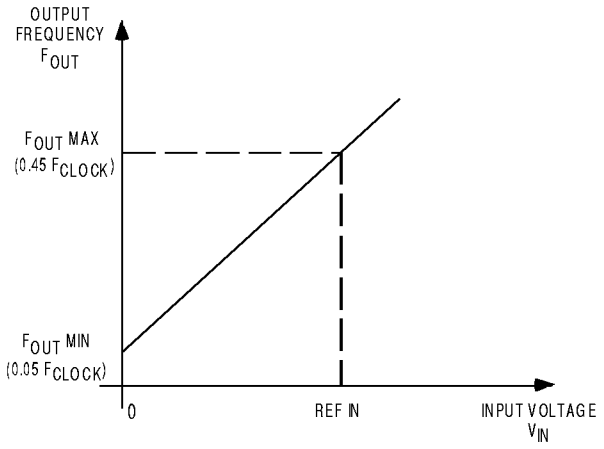


Figure 1. AD7741 Transfer Characteristic for Input Range from 0 V to REF IN.

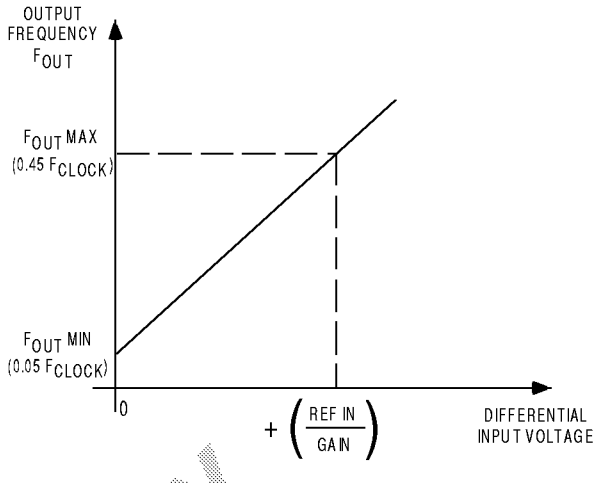


Figure 2. AD7742 Transfer Characteristic for Unipolar Differential input range: 0 V to REF IN/Gain; the input Common Mode Range must be between -300mV and V_{DD} -2V. UNI/BIP pin tied to V_{DD}.

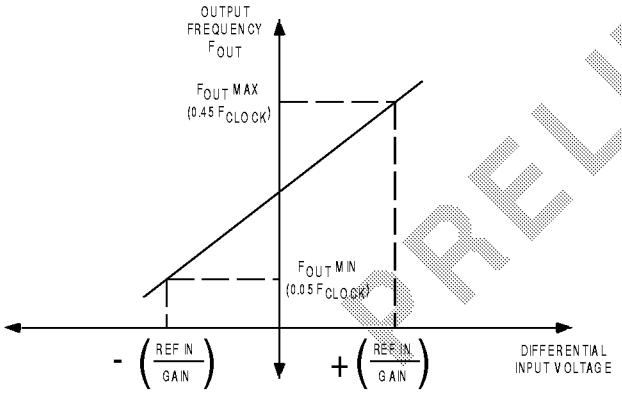


Figure 3. AD7742 Transfer Characteristic for Bipolar Differential Input Range: -REF IN/Gain to +REF IN/Gain (the Common Mode Range is from -300mV to V_{DD} - 2 V). UNI/BIP pin tied to GND.

TABLE I. AD7742 INPUT CHANNEL SELECTION

A1	A0	IN(+)	IN(-)	TYPE
0	0	IN1	IN4	Pseudo Diff
0	1	IN2	IN4	Pseudo Diff
1	0	IN3	IN4	Full Diff
1	1	IN1	IN2	Full Diff

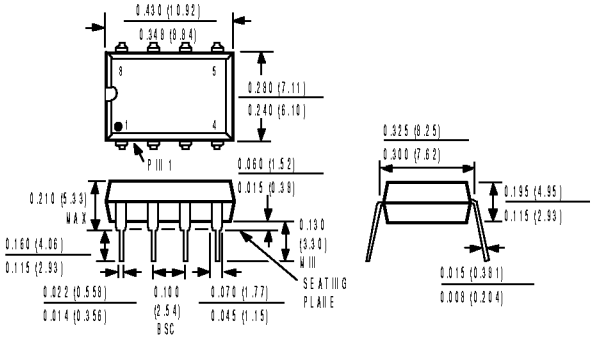
TABLE II. AD7742 GAIN SETTING SELECTION

UNI/BIP	G0	Gain Setting, G	Differential Input Voltage Span (REF IN =2.5V)	
1	0	X1	0 to +2.5 V	0 to +REF IN/Gain
1	1	X2	0 to +1.25 V	0 to +REF IN/Gain
0	0	X1	-2.5 to +2.5 V	-REF IN/Gain to +REF IN/Gain
0	1	X2	-1.25 to +1.25 V	-REF IN/Gain to +REF IN/Gain

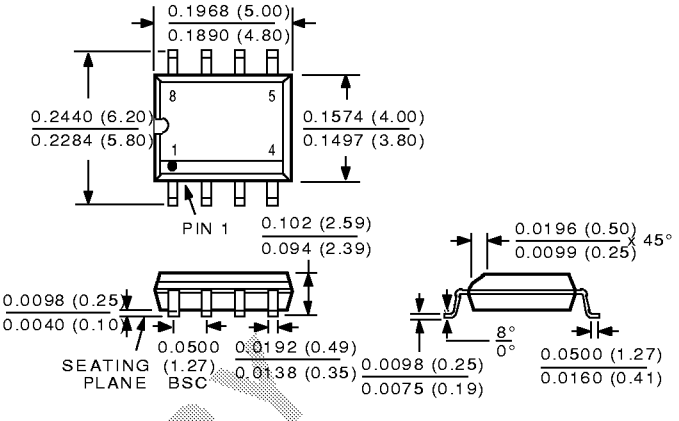
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

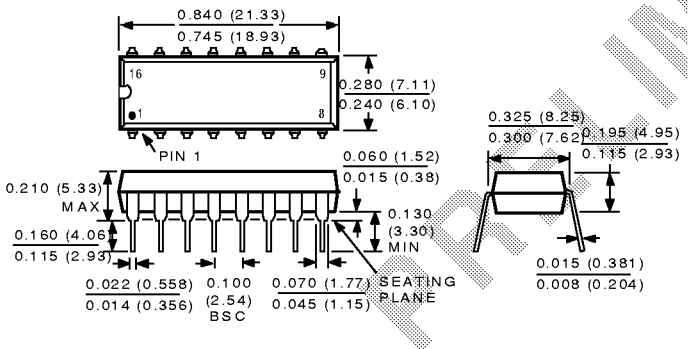
8-Pin Plastic DIP (N-8)



8-Lead SO (R-8)



16-Pin Plastic DIP (N-16)



16-Lead Narrow Body SO (R-16A)