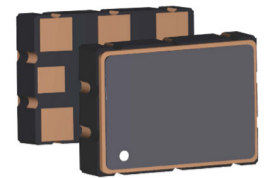


CLEARCLOCK™ | POWER OPTIMIZED 175fs VCXO



7.0 x 5.0 x 1.8 mm

RoHS/RoHS II Compliant

MSL = 1



ESD SENSITIVE

AV7

FEATURES

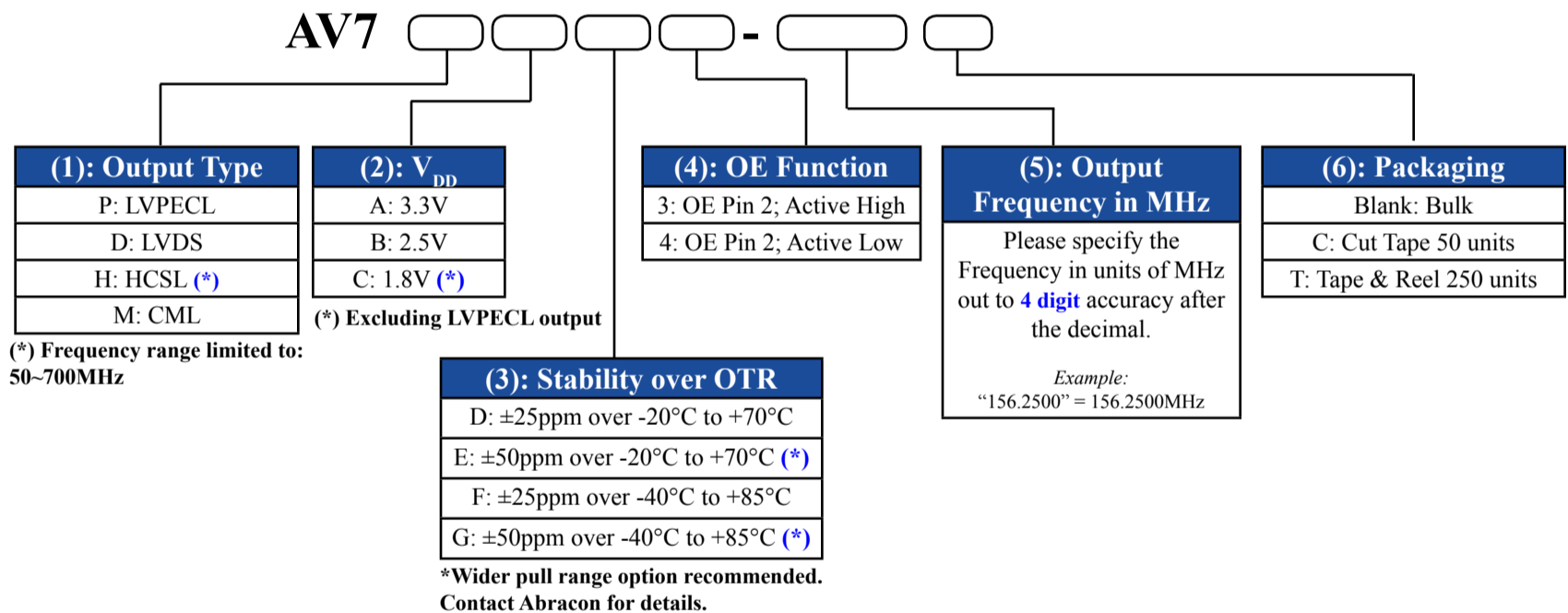
- 175fs typ jitter (300fs MAX)
- Widest in-class frequency range from 50 to 2100MHz
- Excellent spurious suppression
- 68mA MAX I_{DD} (CML)
- Lowest in-class power consumption
- Supports LVPECL, HCSL, LVDS, CML outputs
- ±100ppm pull range
- -40°C to 85°C or -20°C to 70°C operation
- Industry standard 5x7mm footprint
- Supports 3.3V, 2.5V or 1.8V operation

APPLICATIONS

- Networking and communications
- RF systems, base stations (BTS)
- Test and measurement
- 100/400GbEthernet
- Low noise phase locked loops
- Clean-up PLLs
- SONET/SDH
- Broadcast video
- Jitter cleaners

OPTIONS AND PART IDENTIFICATION [Note 1]

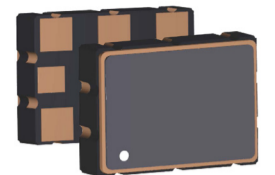
Note 1: Contact Abracon for part number requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal.



Part Number Example:

AV7PAF3-644.53125C

CLEARCLOCK™ | POWER OPTIMIZED 175fs VCXO



AV7

7.0 x 5.0 x 1.8 mm

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ESD SENSITIVE

COMMON KEY ELECTRICAL SPECIFICATIONS

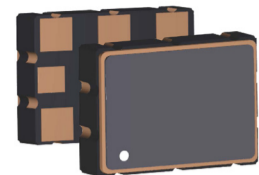
Parameters		Min.	Typ.	Max.	Unit	Notes	
Frequency Range	LVPECL	50		2100	MHz	Option "P"	
	LVDS	50		2100		Option "D"	
	HCSL	50		700		Option "H"	
	CML	50		2100		Option "M"	
Power Supply Voltage (V_{DD}) ^[Note 2]		2.97	3.3	3.63	V	Option "A"	
		2.25	2.5	2.75		Option "B"	
		1.71	1.8	1.89		Option "C"	
Current Consumption (I_{DD})	LVPECL		87	94	mA	@ $V_{DD}=3.3V$	
	LVDS		64	70			
	HCSL		75	80		@ $V_{DD}=1.8V$	
	CML		63	68			
Set Tolerance (as received) @ 25°C ±3°C		-5.00	<±3.00	+5.00	ppm	Relative to carrier	
Operating Temperature Range (OTR)		-40		+85	°C	See Options	
Storage Temperature		-55		+155	°C		
Frequency Stability over OTR		-25		+25	ppm	Option "D or F"	
		-50		+50		Option "E or G"	
Aging over 10-Year Product Life ^[Note 3]		-15		+15	ppm		
All Inclusive Frequency Accuracy over 10-Year Product Life ^[Note 3]		-50		+50	ppm	Specific to freq. stability option "D" or "F" (±25ppm)	
		-100		+100		Specific to freq. stability option "E" or "G" (±50ppm)	
Rise (Tr) / Fall Time (Tf)	LVPECL/LVDS/CML			0.35	nS	20% ↔ 80% waveform	
	HCSL			0.40			
Duty Cycle		45		55	%	@ 50% V_{DD}	
Start-up Time ^[Note 3]			< 5.0	10	ms		
Output High Voltage (V_{OH}) Output Low Voltage (V_{OL})	LVPECL	V_{OH}	$V_{DD}-1.165$		$V_{DD}-0.8$	V	50Ω into $V_{DD}-2.0V$ or Thevenin equivalent
		V_{OL}	$V_{DD}-2.0$		$V_{DD}-1.55$		
	LVDS	V_{OH}		1.4	1.6		100Ω between OUT and OUTN
		V_{OL}	0.9	1.1			
	HCSL	V_{OH}	0.66		1.15		50Ω to V_{DD}
		V_{OL}	0.0		0.15		
	CML	V_{OH}	$V_{DD}-0.085$		$V_{DD}=Max$		50Ω into GND
		V_{OL}	$V_{DD}-0.6$		$V_{DD}-0.32$		
Output Enable (OE) Control			$0.8*(V_{DD})$		V		
				$0.2*(V_{DD})$			

Note 2: Supply Voltage (Vdd) = 1.8V option not available with LVPECL output

Note 3: Relative to initial measured frequency @ 25°C ±3°C

REVISED: 11.10.2017

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AV7

7.0 x 5.0 x 1.8 mm

RoHS/RoHS II Compliant

MSL = 1



ESD SENSITIVE

COMMON KEY ELECTRICAL SPECIFICATIONS

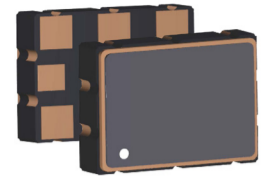
PARAMETERS		MIN.	TYP.	MAX.	UNIT	NOTES
Output Enable Time				2.5	ms	
Output Disable Time				10	μs	
Output Disable Current Consumption	LVPECL		85	86	mA	@ V _{dd} =3.3V
	LVDS		63	65		
	HCSL		77	78		@ V _{dd} =1.8V
	CML		62	67		
Voltage Control Function						
Control Voltage (Vc)	Vdd=3.3V	0.3	1.65	3.0	V	
	Vdd=2.5V	0.25	1.25	2.25		
	Vdd=1.8V	0.18	0.9	1.62		
Frequency Pulling Range		±80	±100		ppm	
Linearity			±5	±10	%	
Transfer Function		Positive Transfer				
Input Impedance		5.0			MΩ	
Bandwidth			10.0		kHz	Measured @ -3dB
Harmonics				-5.0	dBc	
RMS Phase Jitter (12kHz -20MHz BW)			200	300	fsec	@ Vdd=3.3V

TYPICAL PHASE NOISE AND JITTER CHARACTERISTICS (@25°C ± 3°C) [Note 4]

Frequency (MHz)	148.35165	155.52	322.265625
RF Output	LVDS	LVPECL	LVPECL
Supply Voltage (Vdd)	1.8V	3.3V	3.3V
Control Voltage (Vc)	0.9V	1.65V	1.65V
RMS Phase Jitter (fsec) 12kHz-20MHz BW	169	129	136
Phase Noise (dBc/Hz)	100Hz	-74	-68
	1kHz	-100	-93
	10kHz	-122	-125
	100kHz	-140	-140
	1MHz	-150	-150
	10MHz	-156	-159
	20MHz	-157	-159

Note 4: Refer to following Section for selected Phase Noise Plots

CLEARCLOCK™ | POWER OPTIMIZED 175fs VCXO



AV7

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RoHS/RoHS II Compliant

MSL = 1

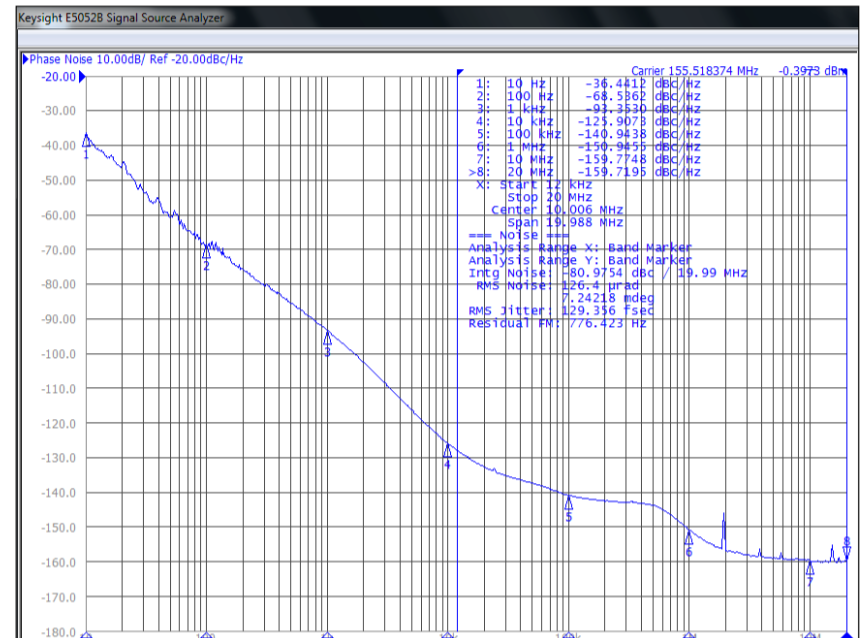
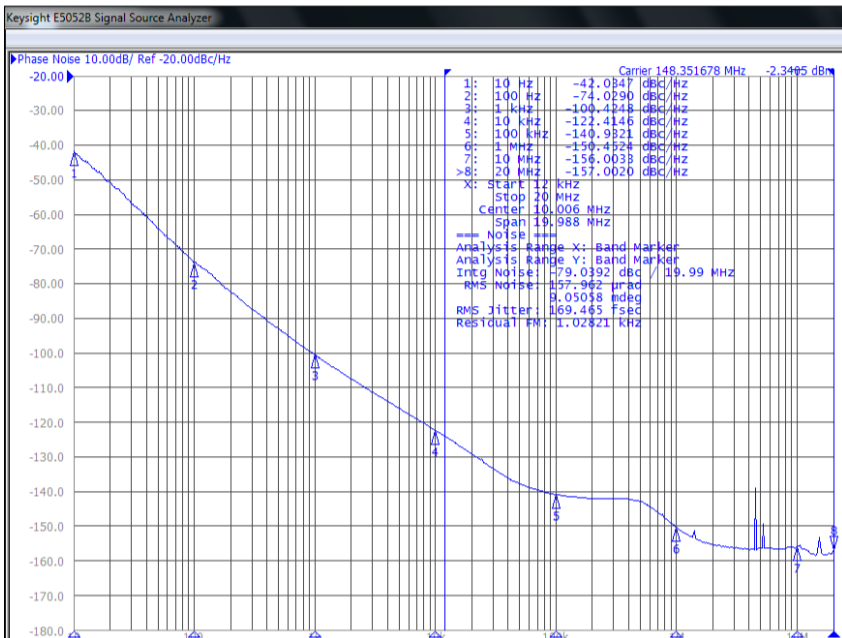


ESD SENSITIVE

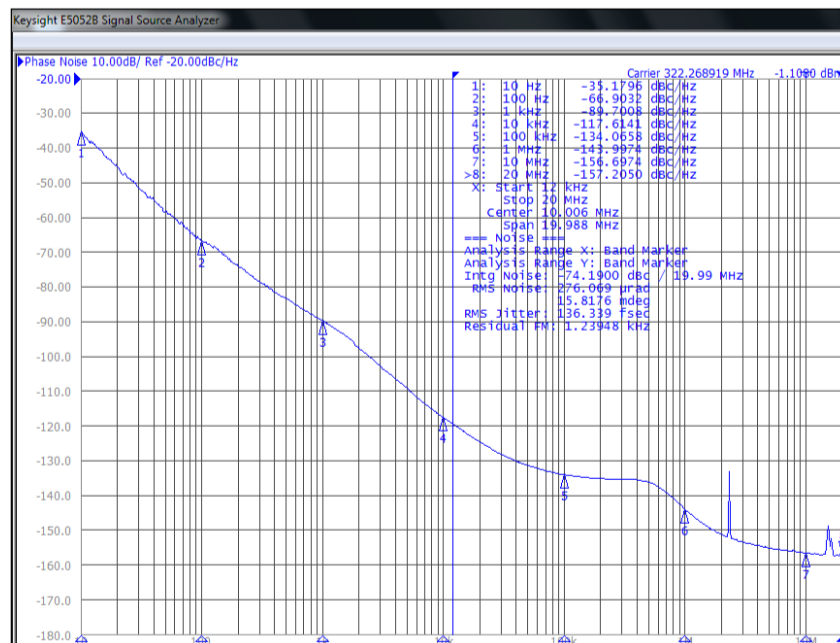
SELECTED PHASE NOISE PLOTS (@25°C ± 3°C)

148.35165MHz – LVDS – Vdd=1.8V; Vc=0.9V

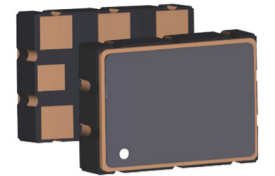
155.52MHz – LVPECL – Vdd=3.3V; Vc=1.65V



322.265625MHz – LVPECL – Vdd=3.3V; Vc=1.65V



CLEARCLOCK™ | POWER OPTIMIZED 175fs VCXO



7.0 x 5.0 x 1.8 mm

RoHS/RoHS II Compliant

MSL = 1



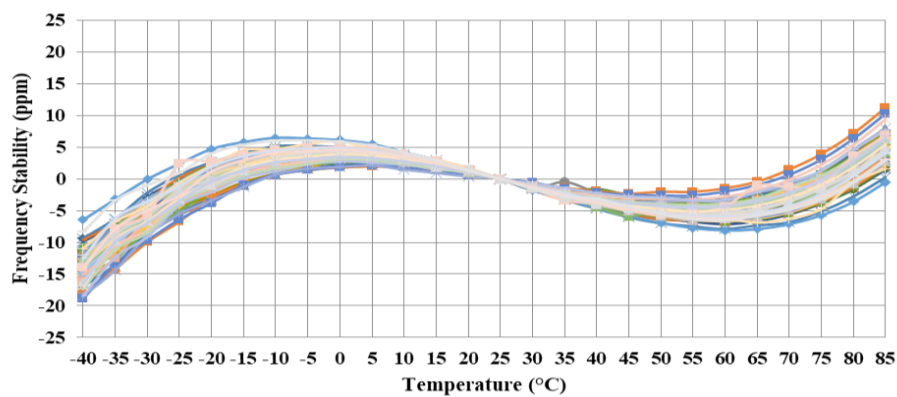
ESD SENSITIVE

AV7

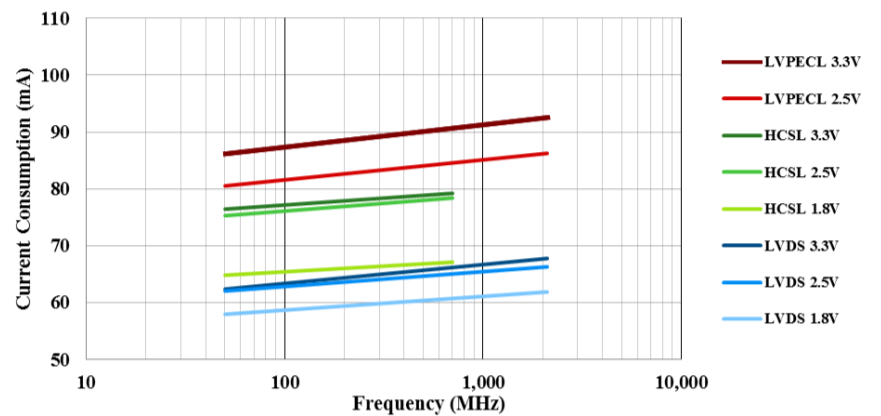
Typical Frequency Vs. Temperature Characteristics

Typical Current Consumption (I_{dd}) Vs. Frequency Characteristics (@ 25°C ± 3°C)

Frequency Stability vs. Temperature
AV7PAF3-122.8800 (50 units)

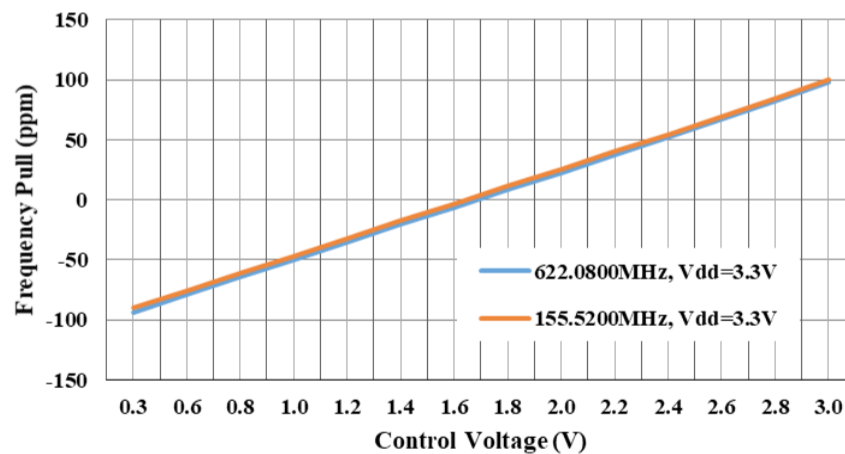


Current Consumption (I_{dd}) vs. Frequency
AV7

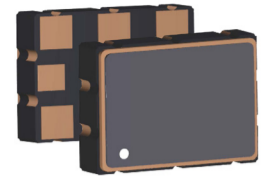


Typical Frequency Pull vs. Control Voltage (V_c) @ 25°C ± 3°C

Frequency Pull vs. Control Voltage (V_c)
AV7



CLEARCLOCK™ | POWER OPTIMIZED 175fs VCXO



7.0 x 5.0 x 1.8 mm

Pb RoHS/RoHS II Compliant

MSL = 1

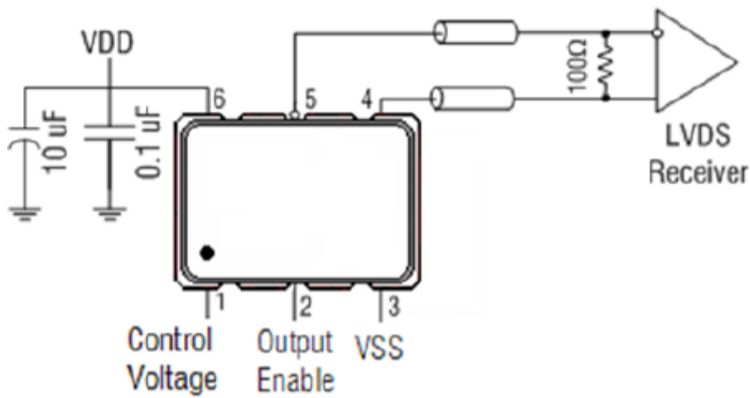


ESD SENSITIVE

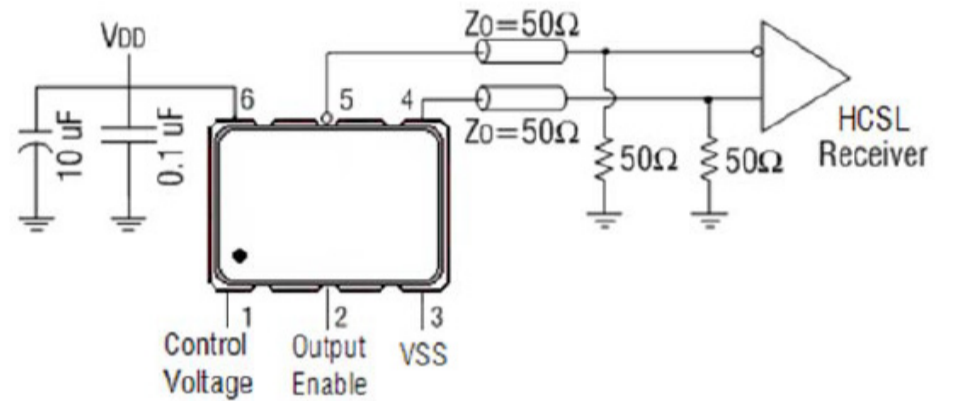
AV7

RECOMMENDED TEST CIRCUIT

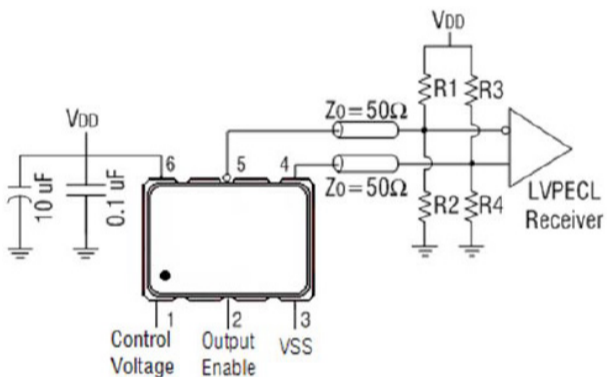
LVDS



HCSL

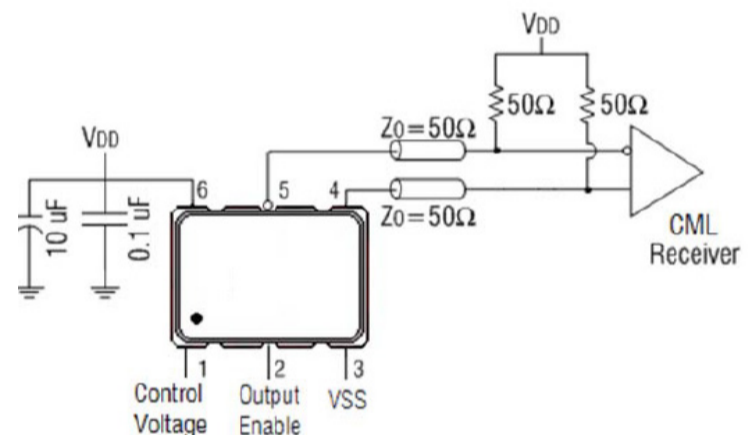


LVPECL

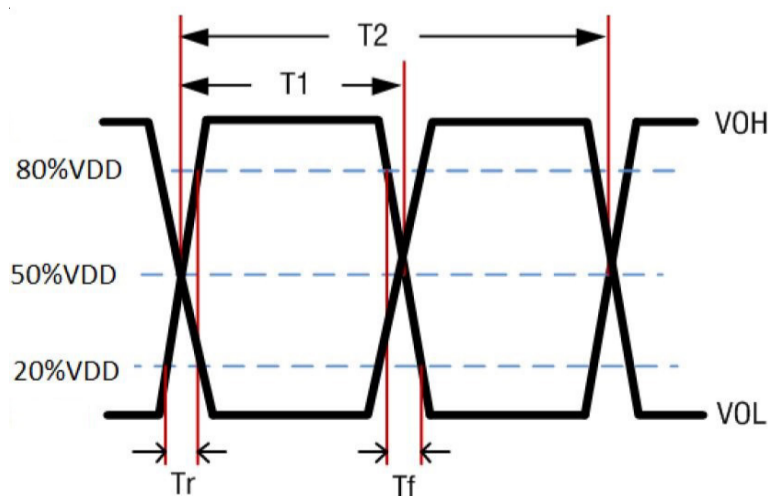


VDD=3.3V: R1=R3=127Ω; R2=R4=82.5Ω
VDD=2.5V: R1=R3=250Ω; R2=R4=62.5Ω

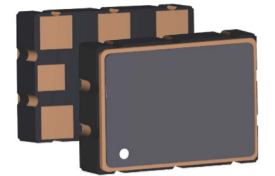
CML



DIFFERENTIAL OUTPUT WAVEFORM



CLEARCLOCK™ | POWER OPTIMIZED 175fs VCXO



AV7

7.0 x 5.0 x 1.8 mm

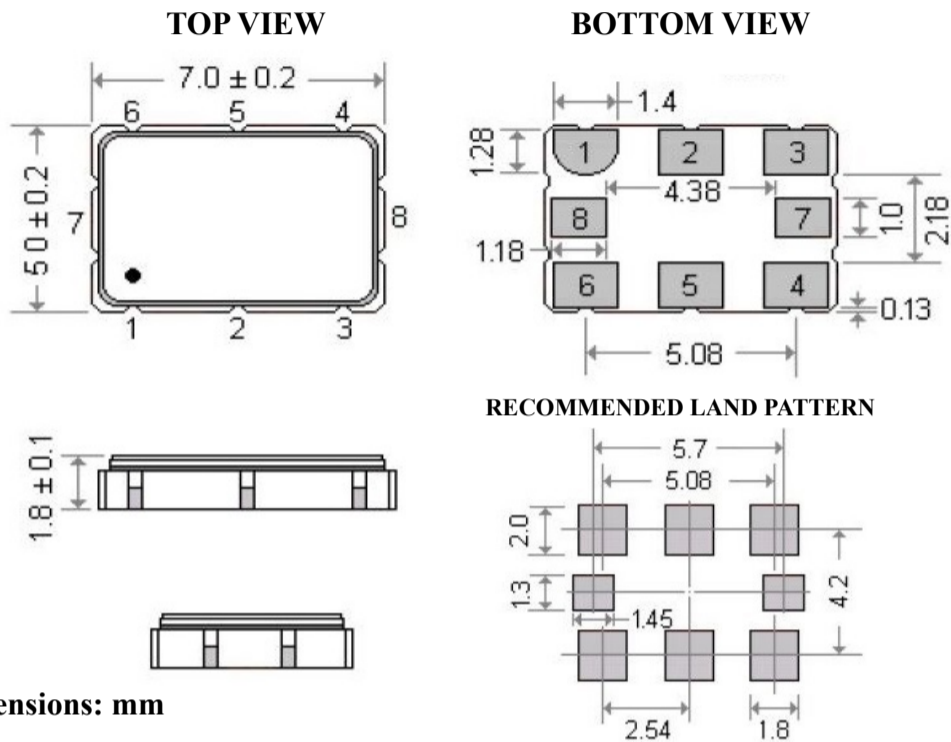
RoHS/RoHS II Compliant

MSL = 1



ESD SENSITIVE

MECHANICAL DIMENSIONS

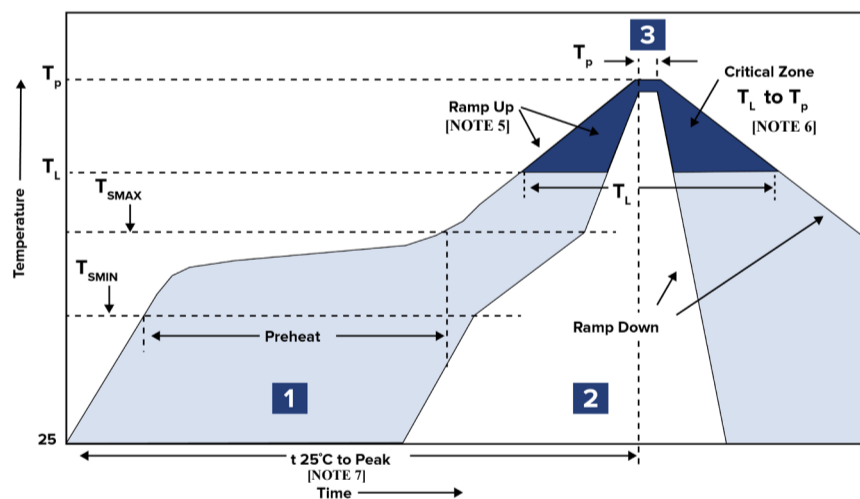


PIN #	FUNCTION
# 1	Control Voltage (V _c)
# 2	Option 3: Enable: Active HIGH Disable: Active LOW Option 4: Enable: Active LOW Disable: Active HIGH
# 3	GND
# 4	Output
# 5	Complementary output
# 6	Supply Voltage (V _{DD})
# 7	No connect
# 8	No connect

*Compatible with industry standard 5x7mm footprint. Pin 7 and 8 are no connect solder pads, not required.

Dimensions: mm

REFLOW PROFILE



Zone	Description	Temperature	Time
1	Preheat / Soak	T _S MIN ~ T _S MAX 150°C ~ 200°C	60 ~ 180 sec.
2	Reflow	T _L 217°C	60 ~ 150 sec.
3	Peak heat	T _p 260°C±5°C	20 ~ 40 sec.

Note 5: Ramp Up Rate (T_L → T_p) = 3°C / sec. MAX

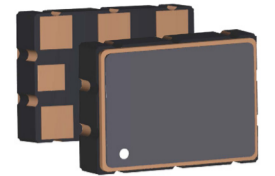
Note 6: Ramp Down Rate (T_p → T_L) = 6°C / sec. MAX

Note 7: Time 25°C to Peak Temperature (25°C → T_p) = 8 minutes MAX

*Can withstand 2 times reflow

*All temperatures refer to topside of the package, measured on the package body surface

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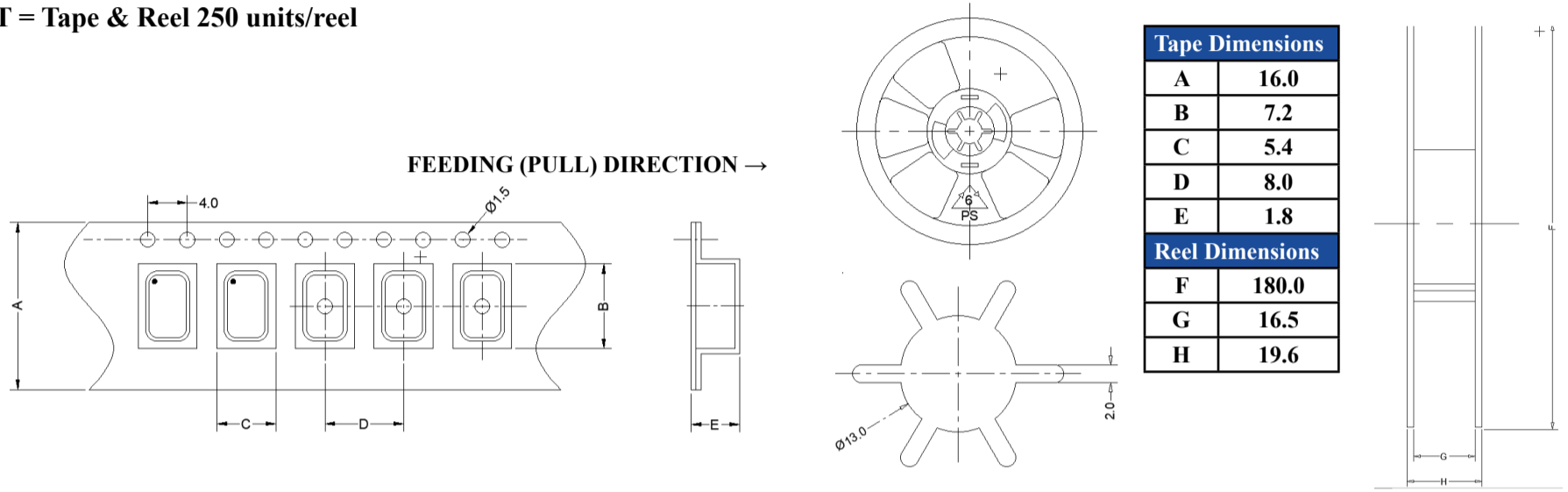


ESD SENSITIVE

PACKAGING

C = Cut Tape 50 units

T = Tape & Reel 250 units/reel



Dimensions: mm