PM4329

HDLIU 32

Hardware Specification

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U.S. Patent No.US5973977 and US6774693. Canadian Patent No. CA2242152. Other relevant patent grants may also exist.

Table of Contents

List of Figures

List of Tables

1 Definitions

Table 1 Definitions

Term	Definition
CDRC	Clock and Data Recovery Unit
CSU	Clock Synthesis Unit
HDLIU	High Density Line Interface Unit
IBCD	Inband Code Detector
JAT	Jitter Attenuator
LIUSHIM	Line Interface Unit Digital Shim
PDVD	Pulse Density Violator Detector
PISO	Parallel In Serial Out
PMON	Performance Monitor
PRBS	Pseudo Random Binary Sequence
SBI	Scaleable Bandwidth Interconnect
SBI TR	Scaleable Bandwidth Interconnect Transport
SIPO	Serial In Parallel Out
XIBC	Inband Code Transmitter
XPDE	Pulse Density Enforcer
J1	J1 mode is compatible to T1 mode. Whenever T1 is mentioned J1 applies.

2 Pinout

2.1 PCB Floor Planning Diagram

Figure 1 HDLIU 32 Interface Arrangement (Bottom View)

SBI/SBI TR Inputs	LIU #24-#32 Interfaces	SBI/SBI TR Outputs
LIU #1-#7 Interfaces	PM4239 HDLIU 32	LIU #17-#23 Interfaces
MPIF I/O	LIU #8-#16 Interfaces	SBI/SBI TR Inputs

2.2 Pin Description

Table 2 SBI Control and Timing

Pin Name	Type	Function
REFCLK	Input	**SBI Reference Clock (REFCLK).** The SBI reference clock signal (REFCLK) provides reference timing for the either SBI ADD and DROP busses. REFCLK is nominally a 50% duty cycle clock of frequency 19.44 MHz ±50ppm.
DC1FP	Input	**SBI DROP bus C1 frame pulse signal (DC1FP).** The SBI DROP bus C1 frame pulse signal (DC1FP) provides Drop frame synchronization for devices connected via an SBI interface. DC1FP must be asserted for 1 REFCLK cycle every 500 µs or multiples thereof (i.e. every 9720 n REFCLK cycles, where n is a positive integer). All devices connected to the SBI DROP bus must be synchronized to a DC1FP signal from a single source. DC1FP is sampled on the rising edge of REFCLK.
AC1FP	Input	**SBI ADD bus C1 frame pulse signal (AC1FP).** The SBI ADD bus C1 frame pulse signal (AC1FP) provides Add frame synchronization for devices connected via an SBI interface. AC1FP must be asserted for 1 REFCLK cycle every 500 µs or multiples thereof (i.e. every 9720 n REFCLK cycles, where n is a positive integer). All devices connected to the SBI ADD bus must be synchronized to a AC1FP signal from a single source. AC1FP is sampled on the rising edge of REFCLK.
DSYNC	Input	**SBI TR DROP bus Synchronization (DSYNC).** The SBI TR DROP bus Synchronization (DSYNC) signal is used to indicate the address for Group 1, Link 1 (1,1), when groups 2 and 3 are also aligned to link 1 (2,1 and 3,1). This signal is used to ensure address synchronization between two or more SBI TR bus devices. SBI TR devices must use the DSYNC to realign internal address generators such that the next address is 2,1 The DSYNC will be active high for one REFCLK cycle every 252 REFCLK cycles, when all groups are aligned to link 1. DSYNC is sampled on the rising edge of REFCLK.
ASYNC	Input	**SBI TR ADD bus Synchronization (ASYNC).** The SBI TR ADD bus Synchronization (ASYNC) signal is used to indicate the address for Group 1, Link 1 (1,1), when groups 2 and 3 are also aligned to link 1 (2,1 and 3,1). This signal is used to ensure address synchronization between two or more SBI TR bus devices. SBI TR devices must use the ASYNC to realign internal address generators such that the next address is 2,1 The ASYNC will be active high for one REFCLK cycle every 252 REFCLK cycles, when all groups are aligned to link 1. ASYNC is sampled on the rising edge of REFCLK.

Pin Name	Type	Function
C1FPOUT/ ALINKRATE[0]	Output	**C1 octet frame pulse output signal (C1FPOUT).** The C1 octet frame pulse output signal (C1FPOUT) may be used to provide frame synchronization for devices interconnected via an SBI interface. C1FPOUT is asserted for 1 REFCLK cycle every 500 µs (i.e. every 9720 REFCLK cycles). If C1FPOUT is used for synchronization, it must be connected to the A/DC1FP inputs of all the devices connected to the SBI ADD or DROP bus. C1FPOUT is updated on the rising edge of REFCLK. C1FPOUT shares the same pin as the ALINKRATE[0] output. C1FPOUT is selected when the SBI_MODE bit, is set to logic 0.

Table 3 SBI System Side Interface

Pin Name	Type	Function
DDATA[0] DDATA[1] DDATA[2] DDATA[3] DDATA[4] DDATA[5] DDATA[6] DDATA[7]	Input	**The SBI DROP bus data signals (DDATA[7:0]).** DDATA[7:0] contain time division multiplexed transmit data from up to 84 independently timed links. Link data is transported as T1 or E1 tributaries within the SBI TDM bus structure. The HDLIU 32 may be configured to extract data from up to 32 T1/E1 tributaries within the structure. DDATA[7:0] are sampled on the rising edge of REFCLK.
DDP/ DPARITY	Input	**The SBI DROP bus parity signal (DDP).** DDP carries the even or odd parity for the DROP bus signals. The parity calculation encompasses the DDATA[7:0], DPL and DV5 signals. Multiple devices can drive the SBI DROP bus at uniquely assigned tributary column positions. This parity signal is intended to detect accidental driver clashes in the column assignment. DDP is sampled on the rising edge of REFCLK. DDP shares the same pin as the DPARITY input. DDP is selected when the SBI_MODE bit, is set to logic 0.
DPL/ DVALID	Input	**The SBI DROP bus payload signal (DPL).** DPL indicates valid data within the SBI TDM bus structure. This signal is asserted during all octets making up a tributary. This signal may be asserted during the V3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed TDM bus structure. This signal may be deasserted during the octet following the V3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed TDM bus structure. DPL is sampled on the rising edge of REFCLK. DPL shares the same pin as the DVALID input. DPL is selected when the SBI_MODE bit, is set to logic 0.
DV5/ DLINKRATE[0]	Input	**The SBI DROP bus payload indicator signal (DV5).** DV5 locates the position of the floating payloads for each tributary within the SBI TDM bus structure. Timing differences between the port timing and the TDM bus timing are indicated by adjustments of this payload indicator relative to the fixed TDM bus structure. All movements indicated by this signal must be accompanied by appropriate adjustments in the DPL signal. DV5 is sampled on the rising edge of REFCLK. DV5 shares the same pin as the DLINKRATE[0] input. DV5 is selected when the SBI_MODE bit, is set to logic 0.

Pin Name	Type	Function
ADATA[0] ADATA[1] ADATA[2] ADATA[3] ADATA[4] ADATA[5] ADATA[6] ADATA[7]	Tristate Output	**The SBI ADD bus data signals (ADATA[7:0]).** ADATA[7:0] contain time division multiplexed receive data from up to 84 independently timed links. Link data is transported as T1 or E1 tributaries within the SBI TDM bus structure. The HDLIU 32 may be configured to insert data into up to 32 T1/E1 tributaries within the structure. Multiple LIU devices can drive the SBI ADD bus at uniquely assigned tributary column positions. ADATA[7:0] are tristated when the HDLIU 32 is not outputting data on a particular tributary column. ADATA[7:0] are updated on the rising edge of REFCLK.
ADP/ APARITY	Tristate Output	**The SBI ADD bus parity signal (ADP).** ADP carries the even or odd parity for the ADD bus signals. The parity calculation encompasses the ADATA[7:0], APL and AV5 signals. Multiple LIU devices can drive this signal at uniquely assigned tributary column positions. ADP is tristated when the HDLIU 32 is not outputting data on a particular tributary column. This parity signal is intended to detect accidental source clashes in the column assignment. ADP is updated on the rising edge of REFCLK. ADP shares the same pin as the APARITY output. ADP is selected when the SBI_MODE bit, is set to logic 0.
APL/ AVALID	Tristate Output	**The SBI ADD bus payload signal (APL).** APL indicates valid data within the SBI TDM bus structure. This signal is asserted during all octets making up a tributary. This signal may be asserted during the V3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed TDM bus structure. This signal may be deasserted during the octet following the V3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed TDM bus structure. Multiple LIU devices can drive this signal at uniquely assigned tributary column positions. APL is tristated when the HDLIU 32 is not outputting data on a particular tributary column. APL is updated on the rising edge of REFCLK. APL shares the same pin as the AVALID output. APL is selected when the SBI_MODE bit, is set to logic 0.
AV5/ AALARM	Tristate Output	**The SBI ADD bus payload indicator signal (AV5).** AV5 locates the position of the floating payloads for each tributary within the SBI TDM bus structure. Timing differences between the port timing and the TDM bus timing are indicated by adjustments of this payload indicator relative to the fixed TDM bus structure. Multiple LIU devices can drive this signal at uniquely assigned tributary column positions. AV5 is tristated when the HDLIU 32 is not outputting data on a particular tributary column. AV5 is updated on the rising edge of REFCLK. AV5 shares the same pin as the AALARM output. AV5 is selected when the SBI_MODE bit, is set to logic 0.
AACTIVE	Output	**The SBI ADD bus active indicator signal (AACTIVE).** AACTIVE is asserted whenever the HDLIU 32 is driving the SBI ADD bus signals, ADATA[7:0], ADP, APL and AV5. AACTIVE is updated on the rising edge of REFCLK.

Table 4 SBI TR System Side Interface

Pin Name	Type	Function
DDATA[0] DDATA[1] DDATA[2] DDATA[3] DDATA[4] DDATA[5] DDATA[6] DDATA[7]	Input	**The SBI TR DROP bus data signals (DDATA[7:0]).** DDATA[7:0] contain time division multiplexed transmit data from up to 84 T1/63 E1independently timed links. Link data is transported as T1 or E1 tributaries within the SBI TR TDM bus structure. The HDLIU 32 may be configured to extract data from up to 32 T1/E1 tributaries within the structure. DDATA[7:0] are sampled on the rising edge of REFCLK.
DLINKRATE[0]/ DV5 DLINKRATE[1] DLINKRATE[2] DLINKRATE[3] DLINKRATE[4] DLINKRATE[5]	Input	**The SBI TR DROP bus link rate signals (DLINKRATE[5:0]).** DLINKRATE[5:0] transport link rate information indicating link data rate inaccuracies with respect to the REFCLK. DLINKRATE[5:0] are sampled on the rising edge of REFCLK. DLINKRATE[0] shares the same pin as the DV5 input. DLINKRATE[0] is selected when the SBI_MODE bit, is set to logic 1.
DPARITY/DDP	Input	The SBI TR DROP bus parity signal (DPARITY) carries the even parity for the DROP bus signals. The parity calculation encompasses the DDATA[7:0], DLINKRATE[5:0] and DVALID signals. Multiple devices can drive the SBI TR DROP bus at uniquely assigned tributary column positions. This parity signal is intended to detect accidental driver clashes in the column assignment. DPARITY is sampled on the rising edge of REFCLK. DPARITY shares the same pin as the DDP input. DPARITY is selected when the SBI_MODE bit, is set to logic 1.
DVALID/DPL	Input	**The SBI TR DROP bus valid signal (DVALID).** DVALID is used to qualify the DDATA[7:0] bus. The DVALID for Link 1, Group 1 (1,1) is generated in the same cycle as the DSYNC pulse. DVALID is sampled on the rising edge of REFCLK. DVALID shares the same pin as the DPL input. DVALID is selected when the SBI_MODE bit, is set to logic 1.
ADATA[0] ADATA[1] ADATA[2] ADATA[3] ADATA[4] ADATA[5] ADATA[6] ADATA[7]	Tristate Output	**The SBI TR ADD bus data signals (ADATA[7:0]).** ADATA[7:0] contain time division multiplexed receive data from up to 84 T1/63 E1 independently timed links. Link data is transported as T1 or E1 tributaries within the SBI TR TDM bus structure. The HDLIU 32 may be configured to insert data into up to 32 T1/E1 tributaries within the structure. Multiple LIU devices can drive the SBI TR ADD bus at uniquely assigned tributary column positions. ADATA[7:0] are tristated when the HDLIU 32 is not outputting data on a particular tributary column. ADATA[7:0] are updated on the rising edge of REFCLK.
ALINKRATE[0]/ C1FPOUT ALINKRATE[1] ALINKRATE[2] ALINKRATE[3] ALINKRATE[4] ALINKRATE[5]	Tristate Output	**The SBI TR ADD bus link rate signals (ALINKRATE[5:0]).** ALINKRATE[5:0] transport link rate information indicating link data rate inaccuracies with respect to the REFCLK. ALINKRATE[5:0] are updated on the rising edge of REFCLK. ALINKRATE[0] shares the same pin as the C1FPOUT output. ALINKRATE[0] is selected when the SBI_MODE bit, is set to logic 1.
APARITY/ADP	Tristate Output	**The SBI TR ADD bus parity signal (APARITY).** APARITY carries the even parity for the ADD bus signals. The parity calculation encompasses the ADATA[7:0], ALINKRATE[5:0], AVALID and AALARM signals.

Pin Name	Type	Function
		Multiple LIU devices can drive this signal at uniquely assigned tributary column positions. APARITY is tristated when the HDLIU 32 is not outputting data on a particular tributary column. This parity signal is intended to detect accidental source clashes in the column assignment. APARITY is updated on the rising edge of REFCLK. APARITY shares the same pin as the ADP output. APARITY is selected when the SBI_MODE bit, is set to logic 1.
AVALID/APL	Tristate Output	**The SBI TR ADD bus valid signal (AVALID).** AVALID is used to qualify the ADATA[7:0] bus. The AVALID for Link 1, Group 1 (1,1) is generated in the same cycle as the ASYNC pulse. Multiple LIU devices can drive this signal at uniquely assigned tributary column positions. AVALID is tristated when the HDLIU 32 is not outputting data on a particular tributary column. AVALID is updated on the rising edge of REFCLK. AVALID shares the same pin as the APL output. AVALID is selected when the SBI_MODE bit, is set to logic 1.
AALARM/AV5	Tristate Output	**The SBI TR ADD bus alarm signal (AALARM).** AALARM is used to transfer link alarm conditions across the SBI TR ADD bus. Multiple LIU devices can drive this signal at uniquely assigned tributary column positions. AALARM is tristated when the HDLIU 32 is not outputting data on a particular tributary column. AALARM is updated on the rising edge of REFCLK. AALARM shares the same pin as the AV5 output. AALARM is selected when the SBI_MODE bit, is set to logic 1.

Table 5 Transmit Line Interface

Pin Name	Type	Function
TXTIP[1] TXTIP[2] TXTIP[3] TXTIP[4] TXTIP[5] TXTIP[6] TXTIP[7] TXTIP[8] TXTIP[9] TXTIP[10] TXTIP[11] TXTIP[12] TXTIP[13] TXTIP[14] TXTIP[15] TXTIP[16] TXTIP[17] TXTIP[18] TXTIP[19] TXTIP[20] TXTIP[21] TXTIP[22] TXTIP[23]	Analog Output	**Transmit Analog Positive Pulse (TXTIP[32:1]).** When the transmit analog line interface is enabled, the TXTIP[x] analog outputs drive the transmit line pulse signal through an external matching transformer. TXTIP[x] is normally connected to the positive lead of the transformer primary. After a reset, TXTIP[x] is high impedance. The TLIUENB bit of the LIU’s LIUSHIM Transmit Control and Status register must be programmed to logic 0 to remove the high impedance state.

Pin Name	Type	Function
TXTIP[24] TXTIP[25] TXTIP[26] TXTIP[27] TXTIP[28] TXTIP[29] TXTIP[30] TXTIP[31] TXTIP[32]		
TXRING[1] TXRING[2] TXRING[3] TXRING[4] TXRING[5] TXRING[6] TXRING[7] TXRING[8] TXRING[9] TXRING[10] TXRING[11] TXRING[12] TXRING[13] TXRING[14] TXRING[15] TXRING[16] TXRING[17] TXRING[18] TXRING[19] TXRING[20] TXRING[21] TXRING[22] TXRING[23] TXRING[24] TXRING[25] TXRING[26] TXRING[27] TXRING[28] TXRING[29] TXRING[30] TXRING[31] TXRING[32]	Analog Output	**Transmit Analog Negative Pulse (TXRING[32:1]).** When the transmit analog line interface is enabled, the TXRING[x] analog outputs drive the transmit line pulse signal through an external matching transformer. TXRING[x] is normally connected to the negative lead of the transformer primary. After a reset, TXRING[x] is high impedance. The TLIUENB bit of the LIU's LIUSHIM Transmit Control and Status register must be programmed to logic 0 to remove the high impedance state.

Table 6 Receive Line Interface

Pin Name	Type	Function
RXTIP[1] RXTIP[2] RXTIP[3] RXTIP[4] RXTIP[5] RXTIP[6] RXTIP[7] RXTIP[8] RXTIP[9] RXTIP[10] RXTIP[11] RXTIP[12]	Analog Input	**Receive Analog Positive Pulse (RXTIP[32:1]).** When the analog receive line interface is enabled, RXTIP[x] samples the received line pulse signal from an external isolation transformer. RXTIP[x] is normally connected directly to the positive lead of the receive transformer secondary

Pin Name	Type	Function
RXTIP[13] RXTIP[14] RXTIP[15] RXTIP[16] RXTIP[17] RXTIP[18] RXTIP[19] RXTIP[20] RXTIP[21] RXTIP[22] RXTIP[23] RXTIP[24] RXTIP[25] RXTIP[26] RXTIP[27] RXTIP[28] RXTIP[29] RXTIP[30] RXTIP[31] RXTIP[32]		
RXRING[1] RXRING[2] RXRING[3] RXRING[4] RXRING[5] RXRING[6] RXRING[7] RXRING[8] RXRING[9] RXRING[10] RXRING[11] RXRING[12] RXRING[13] RXRING[14] RXRING[15] RXRING[16] RXRING[17] RXRING[18] RXRING[19] RXRING[20] RXRING[21] RXRING[22] RXRING[23] RXRING[24] RXRING[25] RXRING[26] RXRING[27] RXRING[28] RXRING[29] RXRING[30] RXRING[31] RXRING[32]	Analog Input	**Receive Analog Negative Pulse (RXRING[32:1]).** When the analog receive line interface is enabled, RXRING[x] samples the received line pulse signal from an external isolation transformer. RXRING[x] is normally connected directly to the negative lead of the receive transformer secondary.

Table 7 Timing Options Control

Pin Name	Type	Function
XCLK1	Input	**Crystal Clock Input (XCLK1).** This signal provides a stable, global timing reference for LIUs #1- #16 internal circuitry via an internal clock synthesizer. XCLK1 is a nominally jitter free clock at 1.544 MHz in T1 mode and 2.048 MHz in E1 mode. In T1 mode, a 2.048 MHz clock may be used as a reference.
XCLK2	Input	**Crystal Clock Input (XCLK2).** This signal provides a stable, global timing reference for LIUs #17 - #32 internal circuitry via an internal clock synthesizer. XCLK2 is a nominally jitter free clock at 1.544 MHz in T1 mode and 2.048 MHz in E1 mode. In T1 mode, a 2.048 MHz clock may be used as a reference.
RSYNC1	Output	**Recovered Clock Synchronization Signal (RSYNC1).** This output signal is the recovered, jitter attenuated, receiver line rate clock (1.544 or 2.048 MHz) of one of the 32 T1 or E1 channels (LIUs #1- #32). Or, optionally the recovered, jitter-attenuated clock synchronously divided by 193 (T1 mode) or 256 (E1 mode) to create a 8 kHz timing reference signal. The default is to source RSYNC1 from LIU #1. If the two internal CSUs are configured for different modes (e.g. CSU#1 is configured for T1 and CSU#2 is configured for E1) the recovered clock should only be selected from one bank of 16 (i.e. LIUs 1 to 16 or LIUs 17 to 32). When the HDLIU 32 is in a loss of signal state, RSYNC1 is derived from the XCLK1/2 input or, optionally, is held high.
RSYNC2	Output	**Recovered Clock Synchronization Signal (RSYNC2).** This output signal is the recovered, jitter attenuated, receiver line rate clock (1.544 or 2.048 MHz) of one of the 32 T1 or E1 channels (LIUs #1- #32). Or, optionally, the recovered, jitter attenuated clock synchronously divided by 193 (T1 mode) or 256 (E1 mode) to create a 8 kHz timing reference signal. The default is to source RSYNC2 from LIU #1. If the two internal CSUs are configured for different modes (e.g. CSU#1 is configured for T1 and CSU#2 is configured for E1) the recovered clock should only be selected from one bank of 16 (i.e. LIUs 1 to 16 or LIUs 17 to 32). When the HDLIU 32 is in a loss of signal state, RSYNC2 is derived from the XCLK1/2 input or, optionally, is held high.

Table 8 Alarm Interface

Pin Name	Type	Function
LOS	Output	Loss of Signal Alarm (LOS). This signal outputs the LOS status of the 32 LIUs in a serial format that repeats every 32 XCLK1 cycles. The presence of the LOS status for LIU #1 on this output is indicated by the LOS_L1 output pulsing high. On the following XCLK1 cycle, the LOS status for LIU #2 is output, then LIU #3, and so on. When the serial peripheral interface is enabled, the status of the LOS alarm can also be determined by reading the LOSV bit in the CDRC Interrupt Status register. LOS is updated on the falling edge of XCLK1.
LOS_L1	Output	Loss of Signal LIU #1 indicator (LOS_L1). This signal is pulsed high for one XCLK1 cycle every 32 XCLK1 cycles and indicates that the LOS status for LIU #1 is being output on LOS. LOS_L1 is updated on the falling edge of XCLK1.

Table 9 Miscellaneous Control Signals

Pin Name	Type	Function
RSTB	Input	**Active Low Reset (RSTB).** This signal provides an asynchronous HDLIU 32 reset. RSTB is a Schmidt triggered input with an internal pull up resistor.
RES_0[1]	Input	This pin must be tied low for normal operation.
RES_0[2] RES_0[3] RES_0[4] RES_0[5]	Analog I/O	These pins must be connected to an analog ground for normal operation.
RES_0[6] RES_0[7] RES_0[8] RES_0[9]	Analog I/O	These pins must be connected to an analog ground for normal operation.
RES_0[10]	Input	This pin must be tied to ground for normal operation.
RES_0[11]	Input	This pin must be tied to ground for normal operation.
TXHIZ	Input	**Transmitter tri-state enable (TXHIZ).** Setting TXHIZ=1 forces each of the transmitters into a high impedance state (i.e. TXTIP[32:1] and TXRING[32:1]).
LINELB	Input	**Line Loopback enable (LINELB).** Setting LINELB=1 forces each of the LIU's into line loopback. When line loopback is enabled the recovered data is internally directed to the digital inputs of the transmit jitter attenuator.
RXTERM	Input	**Receive Termination enable (RXTERM).** This input is used in T1 100Ω and E1 120Ω mode to globally enable receive internal termination of the analog line receiver. When set to logic 1 the internal termination is enabled in the analog line receiver. When set to logic 0, the internal termination of the analog line receiver is bypassed and external termination must be used. Note that external termination is always required in E1 75Ω mode, therefore the RXTERM pin should be tied down to ground if any one of the 32 ports is used in E1 75Ω mode.
DVMP	Analog I/O	**Analog Reserved.** This pin must be left unconnected.

Pin Name	Type	Function
DVMN	Analog I/O	**Analog Reserved.** This pin must be left unconnected.

Table 10 Microprocessor Interface

Pin Name	Type	Function
AD[0] AD[1] AD[2] AD[3] AD[4] AD[5] AD[6] AD[7]	I/O	**Lower Address Bus/ Bi-directional Data Bus (AD[7:0]).** Multiplexed Lower Address and Bi-directional Data Bus (AD[7:0]) is used to address registers and supply data to be written, or output data which is being read. The ALE signal must be used to latch the address presented on the AD[7:0] inputs.
A[8] A[9] A[10] A[11] A[12] A[13]	Input	**Upper Address Bus (A[13:8]).** This bus selects specific registers during HDLIU 32 register accesses. Signal A[13] selects between normal mode and test mode register access. A[13] has an internal pull down resistor. The ALE signal must be used to latch the address presented on the A[13:8] inputs.
ALE	Input	**Address Latch Enable (ALE)** This signal is active high and latches the address bus contents, A[13:8] and AD[7:0], when low. When ALE is high, the internal address latches are transparent. ALE allows the HDLIU 32 to interface to a multiplexed address/data bus. The ALE input has an internal pull up resistor.
WRB	Input	**Active Low Write Strobe (WRB)** This signal is low during a HDLIU 32 register write access. The AD[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low. Alternatively, the AD[7:0] bus contents are clocked into the addressed register on the rising CSB edge while WRB is low.
RDB	Input	**Active Low Read Enable (RDB).** This signal is low during HDLIU 32 register read accesses. The HDLIU 32 drives the AD[7:0] bus with the contents of the addressed register while RDB and CSB are low.
CSB	Input	**Active Low Chip Select (CSB).** CSB must be low to enable HDLIU 32 register accesses. CSB must go high at least once after power up to clear internal test modes. If CSB is not used, it should be tied to an inverted version of RSTB, in which case, RDB and WRB determine register accesses.
INTB	Open-drain Output	**Active low open Drain Interrupt (INTB).** This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that INTB will remain low until all active unmasked interrupt sources are acknowledged at their sources at which time, INTB will tristate.

Table 11 JTAG Interface

Pin Name	Type	Function
TDO	Tristate Output	**Test Data Output (TDO).** This signal carries test data out of the HDLIU 32 via the IEEE 1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output that is tri-stated except when scanning of data is in progress.
TDI	Input	**Test Data Input (TDI).** This signal carries test data into the HDLIU 32 via the IEEE 1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull up resistor.
TCK	Input	**Test Clock (TCK).** This signal provides timing for test operations that can be carried out using the IEEE 1149.1 test access port.
TMS	Input	**Test Mode Select (TMS).** This signal controls the test operations that can be carried out using the IEEE 1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull up resistor.
TRSTB	Input	**Active low Test Reset (TRSTB).** This signal provides an asynchronous HDLIU 32 test access port reset via the IEEE 1149.1 test access port. TRSTB is a Schmidt triggered input with an internal pull up resistor. TRSTB must be asserted during the power up sequence. Note that if not used, TRSTB should be connected to the RSTB input.

Table 12 Analog Power

Pin Name	Type	Function
AVD[1] AVD[2] AVD[3] AVD[4] AVD[5] AVD[6] AVD[7] AVD[8] AVD[9] AVD[10] AVD[11] AVD[12] AVD[13] AVD[14] AVD[15]	Analog Power	**Analog Power (AVD[15:1].** AVD[15:1] provide power for the transmit and receive LIU analog circuitry. AVD[15:1] should be connected to analog + 3.3V.
CAVD1	Analog Power	**Clock Synthesis Unit Analog Power (CAVD1).** CAVD1 supplies power for the transmit clock synthesis unit. CAVD1 should be connected to analog +3.3V.
CAVD2	Analog Power	**Clock Synthesis Unit Analog Power (CAVD2).** CAVD2 supplies power for the transmit clock synthesis unit. CAVD2 should be connected to analog +3.3V.

Table 13 Digital Power

Pin Name	Type	Function
VDDI18[1] VDDI18[2] VDDI18[3] VDDI18[4] VDDI18[5] VDDI18[6] VDDI18[7] VDDI18[8] VDDI18[9] VDDI18[10]	Power	**Core Power (VDDI18[10:1]).** The VDDI18[10:1] pins should be connected to a well decoupled +1.8V DC power supply.
VDDO33[1] VDDO33[2] VDDO33[3] VDDO33[4] VDDO33[5] VDDO33[6] VDDO33[7] VDDO33[8] VDDO33[9] VDDO33[10] VDDO33[11]	Power	**I/O Power (VDDO33[11:1]).** The VDDO33[11:1] pins should be connected to a well decoupled +3.3V DC power supply.

Table 14 Ground

Pin Name	Type	Function
VSS[1] VSS[2] VSS[3] VSS[4] VSS[5] VSS[6] VSS[7] VSS[8] VSS[9] VSS[10] VSS[11] VSS[12] VSS[13] VSS[14] VSS[15] VSS[16] VSS[17] VSS[18] VSS[19] VSS[20] VSS[21] VSS[22] VSS[23] VSS[24]	Power	**Ground (VSS[24:1]).** The VSS[24:1] pins should be connected to Ground.

Notes

1. All HDLIU 32 inputs and bi-directionals present minimum capacitive loading.
1. All HDLIU 32 inputs and bi-directionals, when configured as inputs, tolerate TTL logic levels.

2. All HDLIU 32 outputs and bi-directionals have at least 8 mA drive capability, except the TDO output that has at least 6 mA drive capability.
3. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.
4. Inputs A[13]. RES_0[1] and RES_0[10] have internal pull-down resistors.

3 Functional Description

3.1 Block Description

3.1.1 Receive Interface

The analog receive interface is configurable to operate in both E1 and T1 short haul applications. Short-haul T1 is defined as transmission over less than 655 ft of cable to/from the cross connect. Short-haul E1 is defined as transmission on any cable that attenuates the signal by less than 6 dB.

The receiver sensitivity can be improved to medium haul performance provided line equalization is enabled. When line equalization is enabled the receiver is able to detect E1 and T1 compatible signals with typically up to 22dB and 24dB cable loss respectively. The receiver can be configured to detect and clear the alarm of LOS (Loss of Signal) specified in the E1 G.775 standard.

Receive Interface external components

Figure 2 shows the external components that are connected to the analog receive interface. Refer to Table 15 for the descriptions of the components detailed in Figure 2.

Figure 2 External Analog Receive Interface Circuit

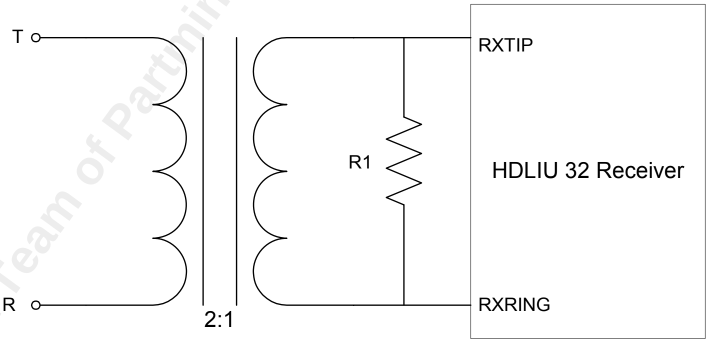


Table 15 External Analog Receive Interface Components

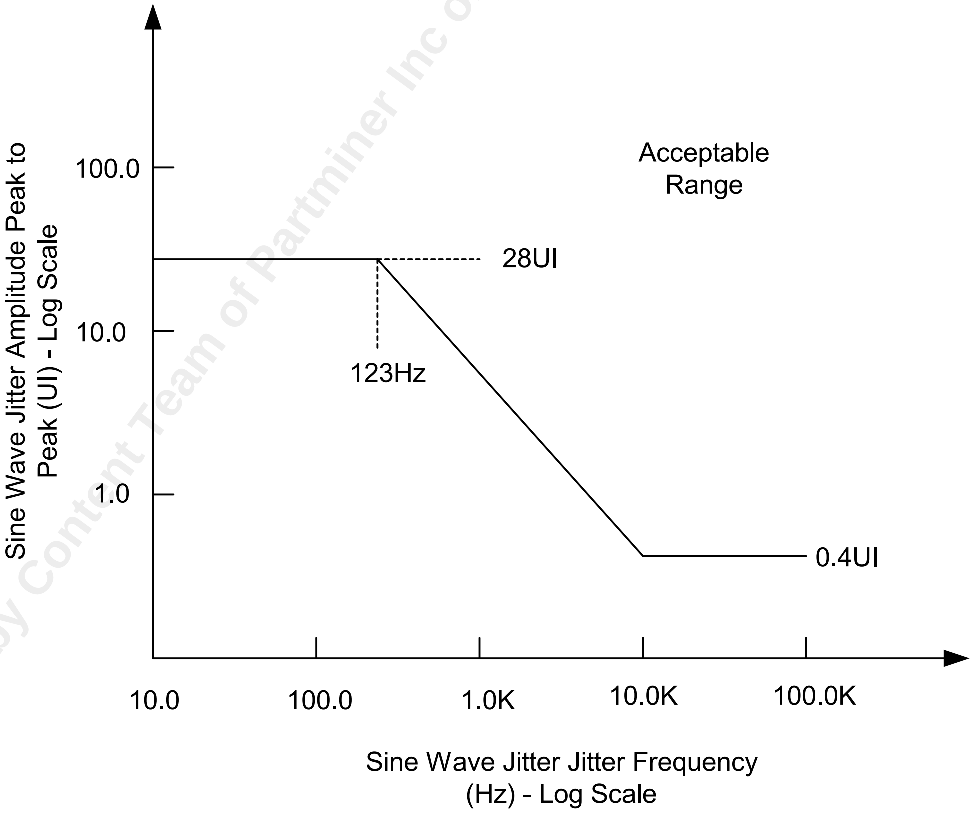
Format	R1
DSX-1 Zo=100Ω	Not Required
E1 Zo=120Ω	Not Required
E1 Zo=75Ω	18.7Ω +/- 1%, 0.25W resistor

3.1.2 Clock and Data Recovery (CDRC)

The Clock and Data Recovery function is provided by the Clock and Data Recovery (CDRC) block. The CDRC provides clock and PCM data recovery, B8ZS and HDB3 decoding, line code violation detection, and loss of signal detection. It recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop and reconstructs the NRZ data. Loss of signal is indicated after a programmable threshold of consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs and is cleared after the occurrence of a single line pulse. An alternate loss of signal indication is provided which is cleared upon meeting a 1-in-8 pulse density criteria for T1 and a 1-in-4 pulse density criteria for E1. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and when the signal returns. A line code violation is defined as a bipolar violation (BPV) for AMI-coded signals, is defined as a BPV that is not part of a zero substitution code for B8ZS-coded signals, and is defined as a bipolar violation of the same polarity as the last bipolar violation for HDB3-coded signals.

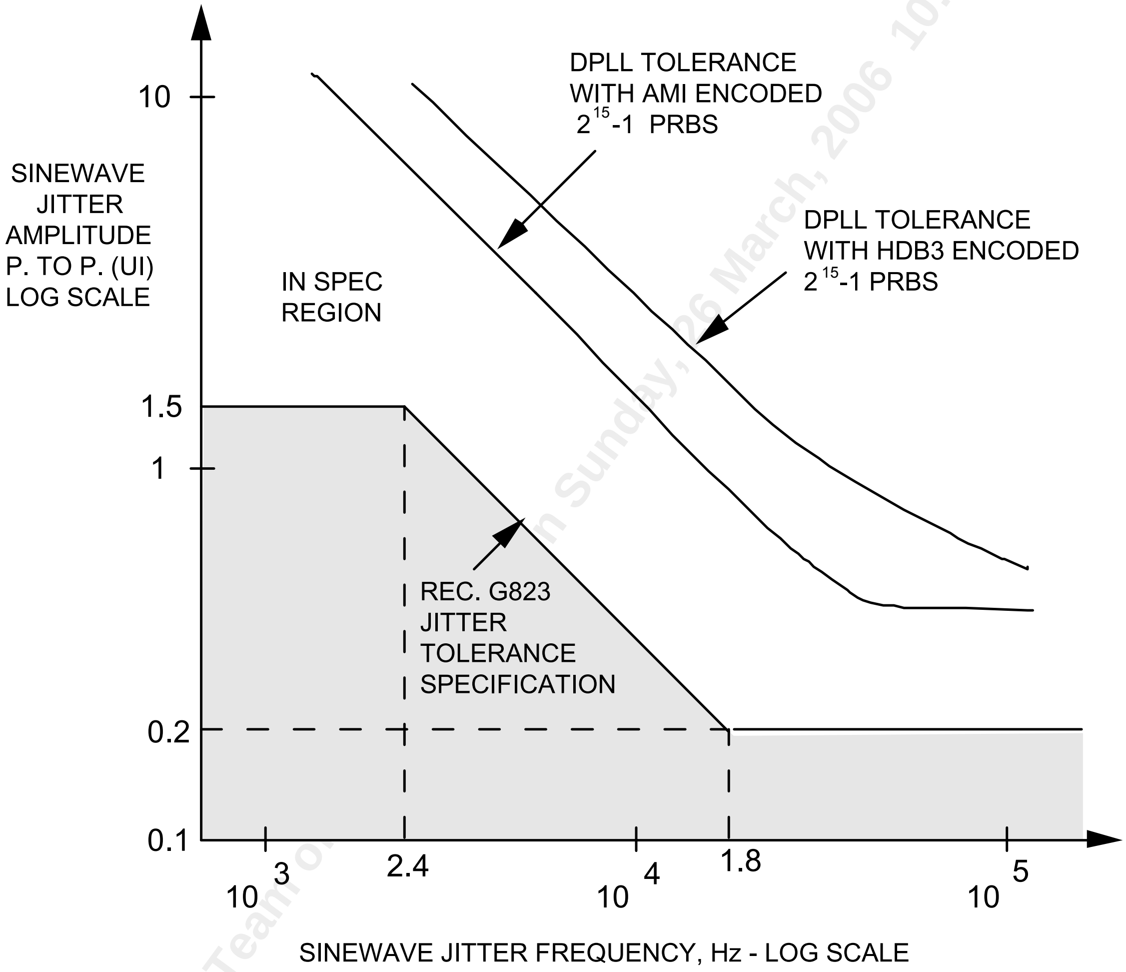
In T1 mode, the input jitter tolerance of the HDLIU 32 complies with the Bellcore Document TA-TSY-000170 and with the AT&T specification TR62411, as shown in Figure 3. The tolerance is measured with a QRSS sequence (2^{20}-1 with 14 zero restriction).

Figure 3 T1 Jitter Tolerance - AT&T specification TR62411



For E1 applications, the input jitter tolerance complies with the ITU-T Recommendation G.823 “The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy.” Figure 4 illustrates this specification and the performance of the phase-locked loop.

Figure 4 Compliance with ITU-T Specification G.823 for E1 Input Jitter



3.1.3 Receive Jitter Attenuator (RJAT)

The Receive Jitter Attenuator (RJAT) digital PLL attenuates the jitter present on the RXTIP/RXRING inputs.

The jitter characteristics of the Receive Jitter Attenuator (RJAT) are the same as the Transmit Jitter Attenuator (TJAT).

3.1.4 T1 Inband Loopback Code Detector (IBCD)

The T1 Inband Loopback Code Detection function is provided by the IBCD block. This block detects the presence of either of two programmable INBAND LOOPBACK ACTIVATE and DEACTIVATE code sequences in the receive data stream. Each INBAND LOOPBACK code sequence is defined as the repetition of the programmed code in the PCM stream for at least 5.1 seconds. The detection algorithm tolerates more than the minimum number of discrepancy bits in order to detect framed PCM data in the presence of a 10^{-2} bit error rate. The code sequence detection and timing is compatible with the specifications defined in T1.403-1993, TA-TSY-000312, and TR-TSY-000303. LOOPBACK ACTIVATE and DEACTIVATE code indication is provided through internal register bits. An interrupt is generated to indicate when either code status has changed.

3.1.5 T1 Pulse Density Violation Detector (PDVD)

The Pulse Density Violation Detection function is provided by the PDVD block. The block detects pulse density violations of the requirement that there be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). The PDVD also detects periods of 16 consecutive zeros in the incoming data. Pulse density violation detection is provided through an internal register bit. An interrupt is generated to signal a 16 consecutive zero event, and/or a change of state on the pulse density violation indication.

3.1.6 Performance Monitor Counters (PMON)

The Performance Monitor block accumulates line code violation events with a saturating counter over consecutive intervals as defined by the period between writes to trigger registers (typically 1 second). When the trigger is applied, the PMON transfers the counter value into holding registers and resets the counter to begin accumulating events for the interval. The counter is reset in such a manner that error events occurring during the reset are not missed.

3.1.7 Pseudo Random Binary Sequence Generation and Detection (PRBS)

The Pseudo Random Binary Sequence Generator/Detector (PRBS) block is a software selectable PRBS generator and checker for 2^{11}-1, 2^{15}-1 or 2^{20}-1 PRBS polynomials for use in the T1 and E1 links. PRBS patterns may be generated and detected in either the transmit or receive directions.

3.1.8 T1 Inband Loopback Code Generator (XIBC)

The T1 Inband Loopback Code Generator (XIBC) block generates a stream of inband loopback codes (IBC) to be inserted into a T1 data stream. The IBC stream consists of continuous repetitions of a specific code. The contents of the code and its length are programmable from 3 to 8 bits.

3.1.9 Pulse Density Enforcer (XPDE)

The Pulse Density Enforcer function is provided by the XPDE block. Pulse density enforcement is enabled by a register bit within the XPDE.

This block monitors the digital output of the transmitter and detects when the stream is about to violate the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window. If a density violation is detected, the block can be enabled to insert a logic 1 into the digital stream to ensure the resultant output no longer violates the pulse density requirement. When the XPDE is disabled from inserting logic 1s, the digital stream from the transmitter is passed through unaltered.

3.1.10 Transmit Jitter Attenuator (TJAT)

The Transmit Jitter Attenuation function is provided by a digital phase lock loop and 80-bit deep FIFO. The depth of the 80-bit FIFO is fully programmable; to allow the depth to be optimized for low latency applications. The TJAT receives jittery; dual-rail data in NRZ format on two separate inputs, which allows bipolar violations to pass through the block uncorrected. The incoming data streams are stored in a FIFO timed to the transmit clock. The respective input data emerges from the FIFO timed to the jitter-attenuated clock.

The jitter attenuator generates the jitter-free 1.544 MHz or 2.048 MHz Transmit clock output by adjusting the Transmit clock’s phase in 1/96 UI increments to minimize the phase difference between the generated Transmit clock and input data clock to TJAT. Jitter fluctuations in the phase of the input data clock are attenuated by the phase-locked loop within TJAT so that the frequency of Transmit clock is equal to the average frequency of the input data clock. For T1 applications, to best fit the jitter attenuation transfer function recommended by TR 62411, phase fluctuations with a jitter frequency above 5.7 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 5.7 Hz are tracked by the generated Transmit clock. In E1 applications, the corner frequency is 7.6 Hz. To provide a smooth flow of data out of TJAT, the Transmit clock is used to read data out of the FIFO.

If the FIFO read pointer (timed to the Transmit clock) comes within one bit of the write pointer (timed to the input data clock), TJAT will track the jitter of the input clock. This permits the phase jitter to pass through unattenuated, inhibiting the loss of data.

Jitter Characteristics

The TJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 61 Unit Intervals peak-to-peak (UIpp) of input jitter at jitter frequencies above 5.7 Hz (7.6 Hz for E1). For jitter frequencies below 5.7 Hz (7.6 Hz for E1), more correctly called wander, the tolerance increases 20 dB per decade. In most applications the TJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The TJAT block meets the stringent low frequency jitter tolerance requirements of AT&T TR 62411 and thus allows compliance with this standard and the other less stringent jitter tolerance standards cited in the references.

TJAT exhibits negligible jitter gain for jitter frequencies below 5.7 Hz (7.6 Hz for E1), and attenuates jitter at frequencies above 5.7 Hz (7.6 Hz for E1) by 20 dB per decade. In most applications, the TJAT block will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through TJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of a 1/96 UI phase adjustment quantum. TJAT meets the jitter attenuation requirements of AT&T TR 62411. The block allows the implied jitter attenuation requirements for a TE or NT1 given in ANSI Standard T1.408, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403 to be met.

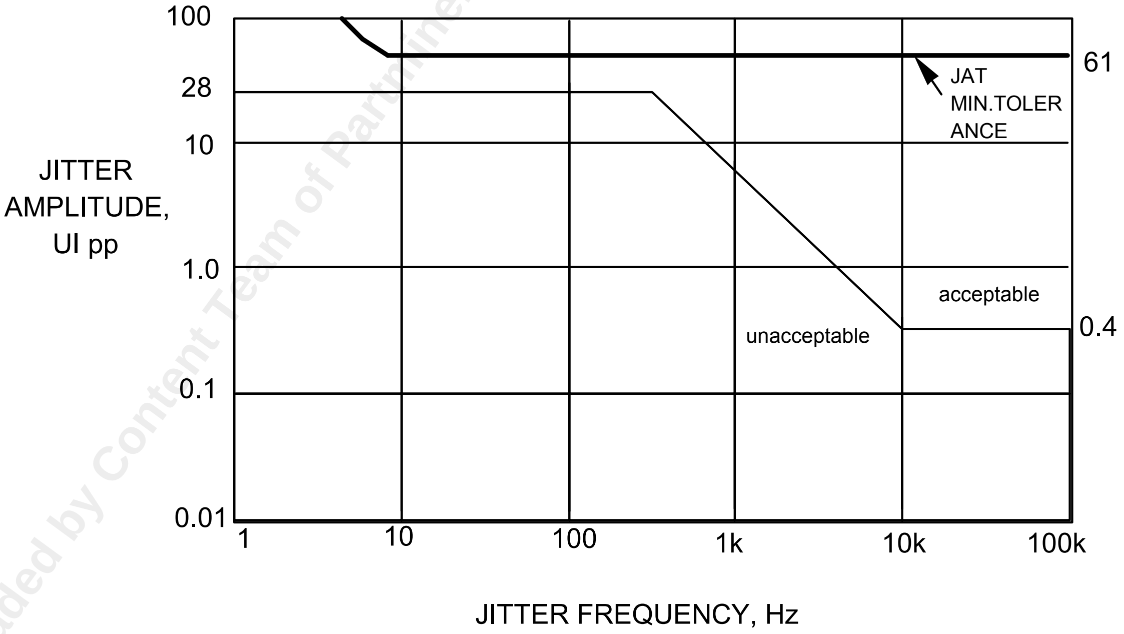
Jitter Tolerance

Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For TJAT, the input jitter tolerance is 61 Unit Intervals peak-to-peak (UIpp) with a worst-case frequency offset of 354 Hz. It is 80 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK (T1/E1 crystal reference clock) and that of the input data clock.

Note

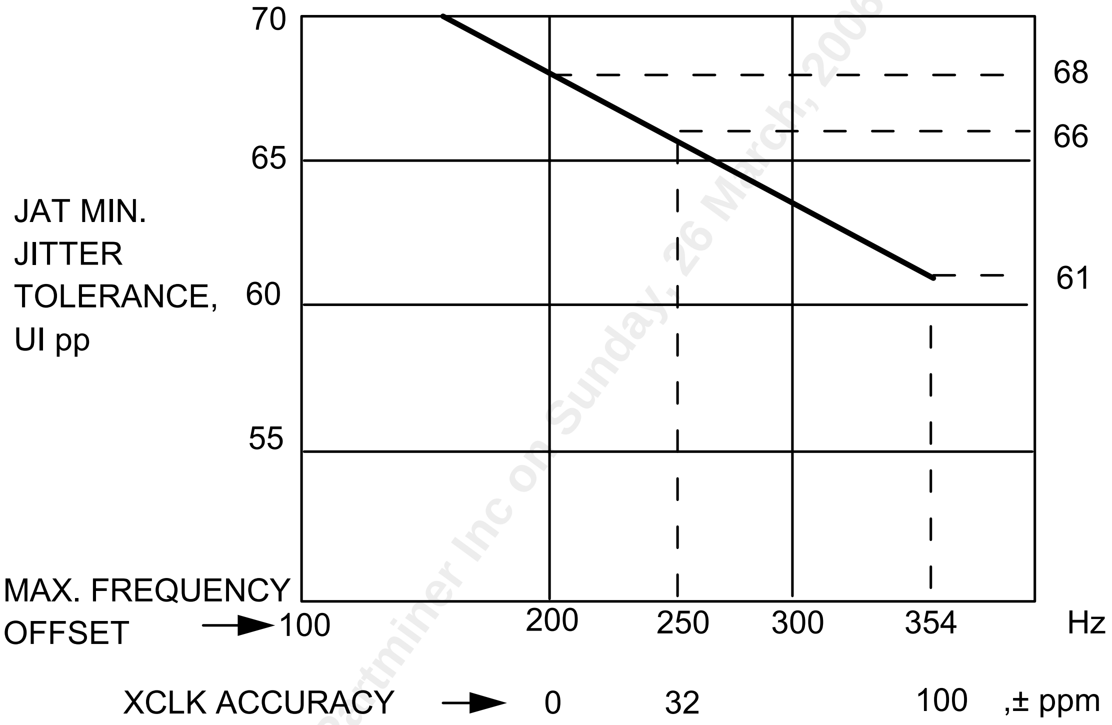
- The jitter tolerance is dependent on the TJAT FIFO depth. The numbers quoted above are achieved with the FIFO set to the maximum depth of 80 bits.

Figure 5 TJAT Jitter Tolerance



The accuracy of the XCLK frequency and that of the TJAT PLL reference input clock used to generate the jitter-free Transmit clock output have an effect on the minimum jitter tolerance. Given that the TJAT PLL reference clock accuracy can be ±200 Hz and that the XCLK input accuracy can be ±50 ppm, the minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK are shown in Figure 6.

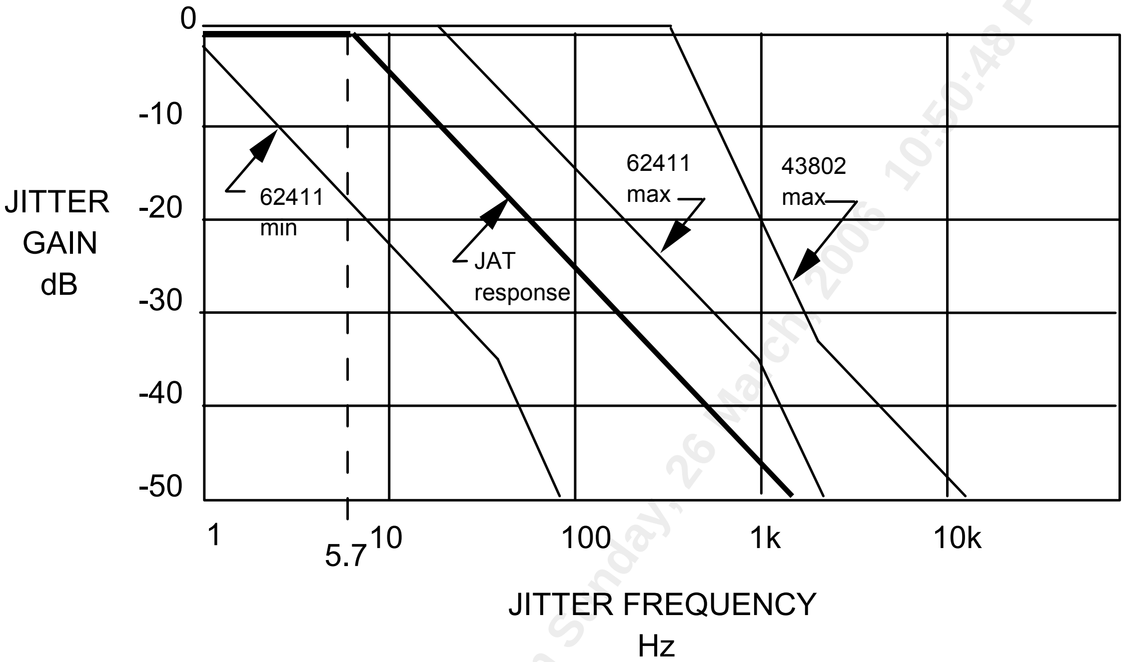
Figure 6 TJAT Minimum Jitter Tolerance vs. Crystal Reference Clock Accuracy



Jitter Transfer

For T1 applications, the output jitter for jitter frequencies from 0 to 5.7 Hz (7.6 Hz for E1) is no more than 0.1 dB greater than the input jitter, excluding residual jitter. Jitter frequencies above 5.7 Hz (7.6 Hz for E1) are attenuated at a level of 6 dB per octave, as shown in Figure 7. The figure is valid for the case where the N1 = FFH in the TJAT Jitter Attenuator Divider N1 Control register and N2 = FFH in the TJAT Divider N2 Control register.

Figure 7 TJAT Jitter Transfer



TJAT clock tracking and operating range

T1: In the non-attenuating mode, when the FIFO is within one UI of overrunning or underrunning, the tracking range is 1.48 MHz to 1.608 MHz. The guaranteed linear operating range for the jittered input clock is 1.544 MHz ± 200 Hz with worst-case jitter (61 UIpp), and maximum system clock frequency offset (± 50 ppm). The nominal range is 1.544 MHz ± 963 Hz with no jitter or system clock frequency offset.

E1: In the non-attenuating mode, when the FIFO is within one UI of overrunning or underrunning, the tracking range is 2.13 MHz to 1.97 MHz. The guaranteed linear operating range for the jittered input clock is 2.048 MHz ± 300 Hz with worst-case jitter (61 UIpp), and maximum system clock frequency offset (± 50 ppm). The nominal range is 2.048 MHz ± 1277 Hz with no jitter or system clock frequency offset.

Jitter Generation

In the absence of input jitter, the output jitter shall be less than 0.025 UIpp. This complies with the AT&T TR 62411 requirement of less than 0.025 UIpp of jitter generation.

3.1.11 Line Transmitter

The line transmitter generates Alternate Mark Inversion (AMI) transmit pulses suitable for use in the DSX-1 (short haul T1) and short haul E1 environments.

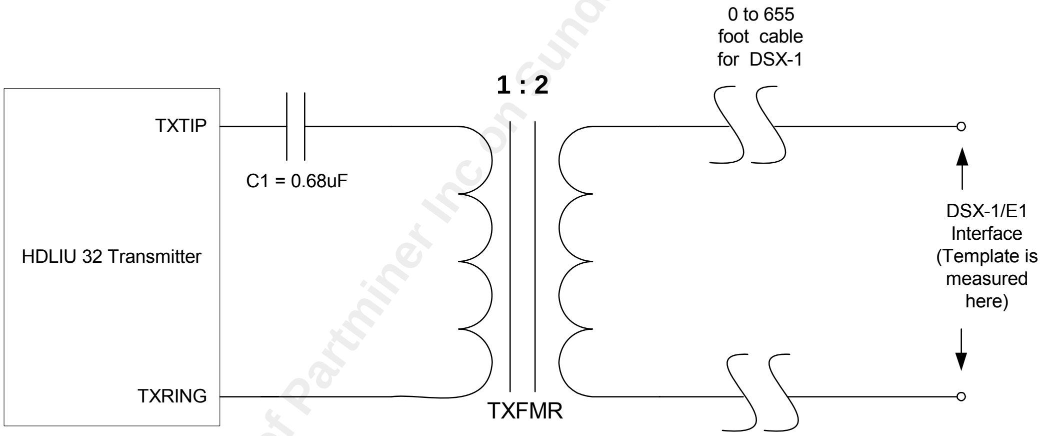
The output pulse shape is synthesized digitally with digital-to-analog (DAC) converters. The DAC's produce differential bipolar outputs that directly drive the TXTIP[32:1] and TXRING[32:1] pins. The output is applied to a line-coupling transformer in a differential manner, which when viewed from the line side of the transformer produce the output pulses at the required levels and ensures a small positive to negative pulse imbalance.

The pulse shape is user programmable. For T1 short haul, the cable length between the HDLIU 32 and the cross-connect (where the pulse template specifications are given) greatly affects the resulting pulse shapes. Hence, the data applied to the converter must account for different cable lengths. For CEPT E1 applications the pulse template is specified at the transmitter, thus only one setting is required.

External Analog Transmit Interface Circuit

Figure 8 shows the external components which are connected to the analog transmitter interface.

Figure 8 External Analog Transmit Interface Circuit



3.1.12 Timing Options (TOPS)

The Timing Options block provides a means of selecting the source of the internal input clock to the TJAT block, and the reference clock for the TJAT digital PLL.

3.1.13 External Analog Interface Circuits

Refer to the Hardware Design Guide for HDLIU 32 document (PMC-2031949).

3.1.14 Scaleable Bandwidth Interconnect Transport (SBI TR) Interface

The Scaleable Bandwidth Interconnect Transport (SBI TR) Bus is a synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links of varying bandwidth. The bus is timed to a reference 19.44MHz clock, a 2 kHz (or fraction thereof) frame pulse and synchronization pulse. All sources and sinks of data on the bus are timed to the reference clock, frame pulse and synchronization pulse.

The SBI TR Bus is a parallel bus that can be used as alternative to SBI in applications where latency is of concern. The SBI TR is used to transfer link information consisting of data, alarm and link rate information with minimum latency.

The multiplexed links are separated into three groups. Each group may be configured independently to carry up to 28 T1/J1s or 21 E1s. The HDLIU 32 may be configured to support 16 T1/J1 and 16 E1 tributaries simultaneously.

3.1.15 Scaleable Bandwidth Interconnect (SBI) Interface

The Scaleable Bandwidth Interconnect is a synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links of varying bandwidth. The bus is timed to a reference 19.44MHz clock and a 2 kHz (or fraction thereof) frame pulse. All sources and sinks of data on the bus are timed to the reference clock and frame pulse.

Timing is communicated across the Scaleable Bandwidth Interconnect by floating data structures. Payload indicator signals in the SBI control the position of the floating data structure and therefore the timing. When sources are running faster than the SBI the floating payload structure is advanced by an octet by passing an extra octet in the V3 octet locations. When the source is slower than the SBI the floating payload is retarded by leaving the octet after the V3 octet unused. Both these rate adjustments are indicated by the SBI control signals.

The SBI multiplexing structure is modeled on the SONET/SDH standards. The SONET/SDH virtual tributary structure is used to carry T1/J1 and E1 links.

The SBI structure uses a locked SONET/SDH structure fixing the position of the TUG-3/TU-3 relative to the STS-3/STM-1 transport frame. The SBI is also of fixed frequency and alignment as determined by the reference clock (REFCLK) and frame indicator signal (C1FP). Frequency deviations are compensated by adjusting the location of the T1/J1/E1 channels using floating tributaries as determined by the V5 indicator and payload signals (DV5, AV5, DPL and APL). Note that the HDLIU 32 always operates as a clock slave on the SBI DROP bus and as a clock master on the SBI ADD bus, i.e. it does not support the AJUST_REQ and DJUST_REQ timing adjustment request signals defined in the SBI bus specification.

The multiplexed links are separated into three Synchronous Payload Envelopes (SPE). Each envelope may be configured independently to carry up to 28 T1/J1s or 21 E1s. The HDLIU 32 may be configured to support 16 T1/J1 and 16 E1 tributaries simultaneously.

3.1.16 SBI Extractor and PISO

The SBI Extract block receives data from the either the SBI or the SBI TR DROP bus and converts it to serial bit streams for transmission. The SBI Extract block may be configured to enable or disable extraction of individual tributaries within the SBI/SBI TR DROP bus. It may also be configured to generate an all-1s output to the transmit LIU when an alarm indication is signaled for a particular tributary via the SBI bus.

3.1.17 SBI Inserter and SIPO

The SBI Insert block receives serial data from the LIUs and inserts it on the either the SBI or SBI TR ADD bus. The SBI Insert block may be configured to enable or disable transmission of individual tributaries on to the SBI/SBI TR ADD bus.

3.1.18 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported.

Note

- See PMC-Sierra’s JTAG Application Note (document number PMC-2021518) for functional details.

JTAG_ID[31:28] = 2h ;Rev ID,

JTAG_ID[27:12] = 4329h ;Device ID,

JTAG_ID[11:0] = 0CDh ;PMC_ID.

3.1.19 Microprocessor Interface

The Microprocessor Interface Block provides normal and test mode registers, the interrupt logic, and the logic required to connect to the Processor Interface. The Microprocessor Interface uses a multiplexed address/data bus. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the HDLIU 32.

4 Functional Timing

4.1 SBI Interface

Figure 9 SBI Bus Functional Timing

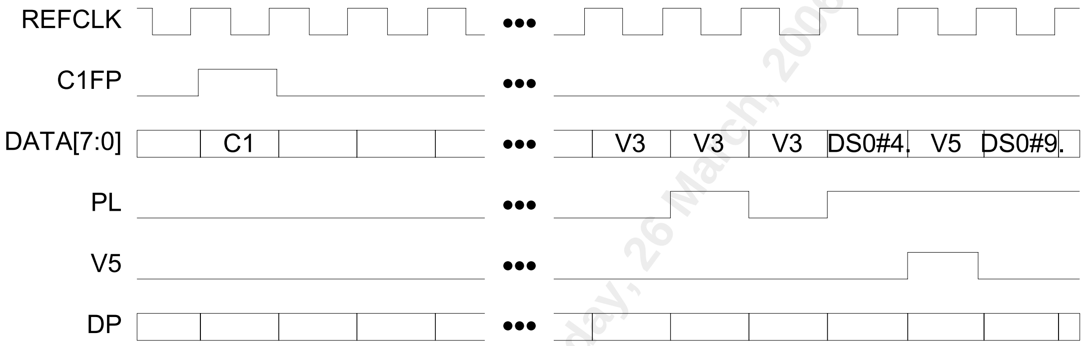
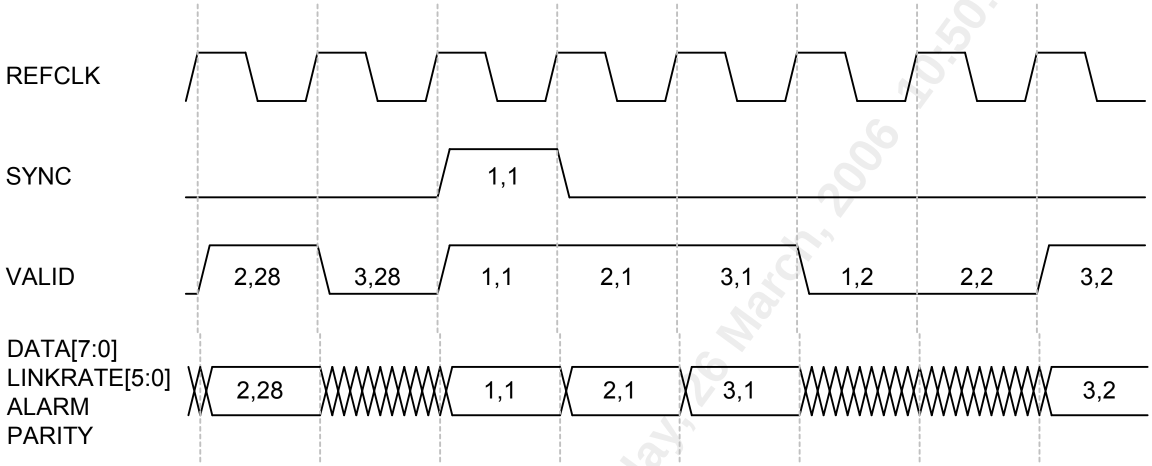


Figure 9 illustrates the operation of the SBI Bus, using a negative justification on the second to last V3 octet as an example. The justification is indicated by asserting PL high during the V3 octet. The timing diagram also shows the location of one of the tributaries by asserting V5 high during the V5 octet.

The SBI ADD and DROP busses operate in an identical manner. Signal names on the ADD bus have an A prepended to them (e.g., AC1FP, ADATA[7:0], etc.) and those on the DROP bus have an D prepended to them (e.g., DC1FP, DDATA[7:0], etc.).

4.2 SBI TR Interface

Figure 10 SBI TR Functional Timing



Note:

1. Figure 10 illustrates the operation of the SBI TR for an application in which 84 data links are supported. The waveform shows *data* being transferred on DATA[7:0]. The *link rate* and *alarm* information follow the same timing as the *data* on DATA[7:0]. LINKRATE[5:0] and ALARM information however are not validated by VALID and therefore must be generated correctly every cycle independently of VALID.

The SYNC is a reference signal that may be externally generated. SYNC marks the address for GROUP 1, LINK 1 (1,1), when GROUPs 2 and 3 are also aligned to link 1 (2,1 and 3,1).

5 Power

5.1 Normal Operating Conditions

Table 16 Normal Operating Voltages for 0.18 um CMOS

	Operating Range[1]			Reference (approx.)
Supply Voltages	**Minimum (V)**	**Typical (V)**	**Maximum (V)**	
1.8V Core Supply Voltage (VDDI18)	1.71	1.80	1.89	+/- 5%
3.3V Analog Supply Voltage (AVD)	3.13	3.3	3.47	+/- 5%
3.3V I/O Supply Voltage (VDDO33)	3.13	3.3	3.47	+/- 5%

Notes:

1. Power supply, D.C. characteristics, and A.C. timing are characterized across these operating ranges, unless otherwise stated.

Table 17 Power Condition Definition

	Typical	Thermal	Max
Process	Nominal	Nominal +2 sigmas of process variation	Nominal +6 sigmas of process variation
Voltage	Nominal Vdd	Maximum Vdd	Maximum Vdd
Temperature	Tj=75C	Tj=105C	Tj as indicated

5.2 Power Requirements

Table 18 Power Requirements

Mode and Conditions	Parameter	Typical Consumption	Thermal Dissipation	Max Consumption
T1, 0-110ft, 1010 pattern SBI/SBI TR, 32 channels active Internal termination active	IDDOP1V8	0.15A	-	-
	IDDOP3V3	0.95A	-	-
	Total Power	3.41W	-	-
T1, 550-660ft, all ones pattern SBI/SBI TR, 32 channels active Internal termination active	IDDOP1V8	-	-	0.3A
	IDDOP3V3	-	-	2.685A
	Total Power	-	6.31W	9.4W
E1 120Ω, 0dB, 1010 pattern SBI/SBI TR, 32 channels active Internal termination active	IDDOP1V8	0.14A	-	-
	IDDOP3V3	0.86A	-	-
	Total Power	3.09W	-	-
E1 120Ω, 0dB, all ones pattern SBI/SBI TR, 32 channels active Internal termination active	IDDOP1V8	-	-	0.23A
	IDDOP3V3	-	-	1.53A
	Total Power	-	5.26W	5.46W
E1 75Ω, 0dB, 1010 pattern SBI/SBI TR, 32 channels active Internal termination active	IDDOP1V8	0.14A	-	-
	IDDOP3V3	0.96A	-	-
	Total Power	3.43W	-	-
E1 75Ω, 0dB, all ones pattern SBI/SBI TR, 32 channels active Internal termination active	IDDOP1V8	-	-	0.21A
	IDDOP3V3	-	-	1.73A
	Total Power	-	4.33W	6.39W

Notes:

1. SBI TR/SBI Bus outputs (except AACTIVE) and microprocessor outputs are loaded with 100pF. All other outputs are loaded with 50pF.
2. The "Max Consumption" includes the operating current of both the HDLIU 32 device and the transmit line driver. Whereas, the "Thermal Dissipation" is the power dissipated by the HDLIU 32 device only.
3. Power values are calculated using the formula:

$$\text{Power} = \sum i(\text{VDD} \times \text{IDD})$$

Where i denotes all the various power supplies on the device, VDD is the voltage for supply i in accordance with the condition, and IDD is the current for supply i.

5. For further details on the power consumption refer to the "PM4329 HDLIU 32 Power Consumption Summary Application Note" (PMC-2041530).

Table 19 Conditions for Power Requirements

	Typical	Power For Thermal Calculations	Maximum Current
Process	Nominal	Nominal +2 sigmas of process variation*	Nominal +6 sigmas of process variation
Voltage	Nominal Vdd	Maximum Operating Vdd	Maximum Vdd
Temperature	Tj=75C	Tj=105C	Temperature that yields the highest current

* The power number for nominal process + 2 sigma of process variation is recommended for thermal calculations as it will be highest power dissipation of all parts in almost all applications.

6 Thermal Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for use in both central office equipment[1] and outside plant equipment[1].

Table 20 Thermal Information

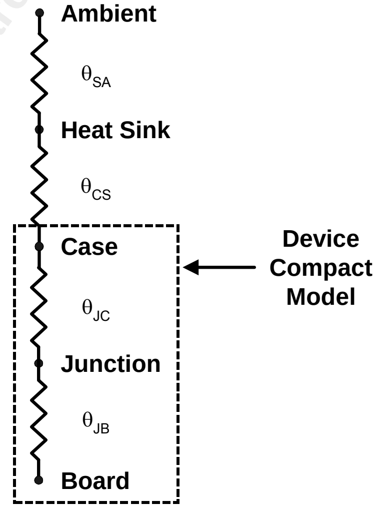
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2].	125 °C

Table 21 Device Compact Model[2]

Junction-to-Case Thermal Resistance, θ_{JC}	0.46 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	9.26 °C/W

Table 22 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	The sum of $\theta_{SA} + \theta_{CS}$ must be less than or equal to: $[(105 - T_A) / P_D] - \theta_{JC}]$ °C/W where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package[5]
	θ_{SA} and θ_{CS} are required for long-term operation



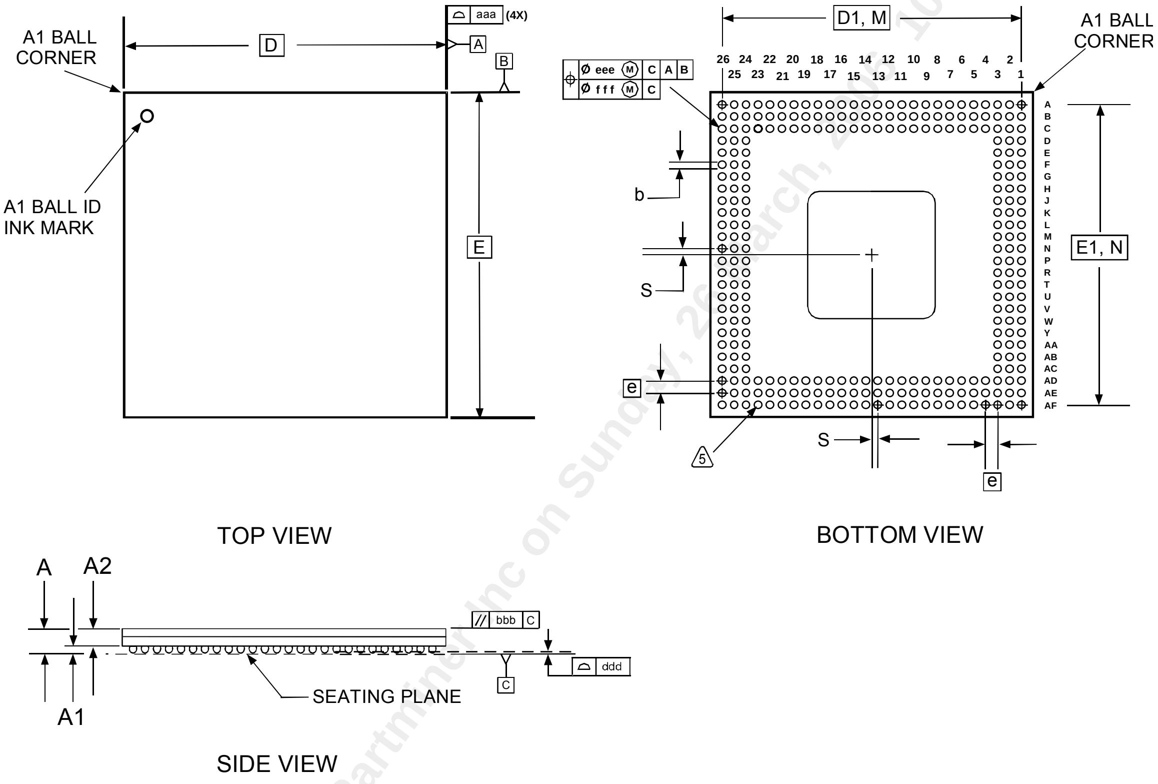
Notes

1. Central Office Equipment meets the ambient temperature requirement for Commercial Equipment (0°C to +70 °C). Outside Plant Equipment meets the ambient temperature requirement for Industrial Equipment (-40°C to +85°C).
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core; for more information about the GR-63-CORE standard, see Telcordia Technologies. *Network Equipment-Building System (NEBS) Requirements: Physical Protection: Telcordia Technologies Generic Requirements GR-63-CORE*. Issue 1. October 1995.
3. θ_{JC}, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8; for more information about the JESD51-8 standard, see Electronic Industries Alliance 1999. *Integrated Circuit Thermal Test Method Environmental Conditions - Junction-to-Board: JESD51-8*. October 1999.
4. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place
5. Power depends upon the operating mode. To obtain power information, refer to the column under thermal in Table 18 Power Requirements.

7 Package Specification

The package conforms to JEDEC JESD51 (2S2P).

Figure 11 276 PIN L2BGA -27x27 MM BODY



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) DIAMETER OF SOLDER MASK OPENING IS 0.45 +/- 0.025 MM DIAMETER (SMD).
6) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE M0-192, VARIATION AAL-1, BUT DOES NOT MEET SOLDER BALL POSITION SPECIFICATION.

PACKAGE TYPE : 276 L2 BALL GRID ARRAY - L2BGA

BODY SIZE : 27 x 27 x 1.47 MM

Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	eee	f f f	S
Min.	-	0.50	-	-	-	-	-	-	0.50	-	-	-	-	-	-	-
Nom.	1.55	0.60	0.95	27.00 BSC	25.00 BSC	27.00 BSC	25.00 BSC	26x26	0.63	1.00 BSC	-	-	-	-	-	-
Max.	-	0.70	-	-	-	-	-	-	0.70	-	0.20	0.25	0.20	0.30	0.10	0.50

8 DC Characteristics

Table 23 DC Characteristics

Symbol	Parameter	Min (V)	Typ (V)	Max (V)	Conditions
VIL	Input Low Voltage	-0.5	—	0.8	Guaranteed Input LOW Voltage
VIH	Input High Voltage	2.0	—	VDDo+0.5	Guaranteed Input HIGH Voltage
VOL	Output or Bidirectional Low Voltage	—	0.1	0.4	VDDo = min, IOL = -6mA TDO outputs; -8mA for others.
VOH	Output or Bidirectional High Voltage	2.4	2.7	—	VDDo = min, IOH = 6mA TDO outputs; 8mA for others.

Table 24 DC Characteristics independent of Voltage levels

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VT+	Reset Input High Voltage	2.0	—	—	Volts	TTL Schmitt
VT-	Reset Input Low Voltage	—	—	0.8	Volts	TTL Schmitt
VTH	Reset Input Hysteresis Voltage	—	0.5	—	Volts	TTL Schmitt
IILPU	Input Low Current	+20	+83	+200	µA	VIL = GND[1,3]
IIHPU	Input High Current	-10	0	+10	µA	VIH = VDD[1,3]
IIL	Input Low Current	-10	0	+10	µA	VIL = GND[2,3]
IIH	Input High Current	-10	0	+10	µA	VIH = VDD[2,3]
CIN	Input Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF
COUT	Output Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF
CIO	Bidirectional Capacitance	—	5	—	pF	Excluding Package, Package Typically 2 pF

Notes

1. Input pin or bi-directional pin with internal pull-up resistor
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing)

Absolute maximum ratings are the worst-case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal operating conditions and continuous error-free operation under these conditions is not guaranteed.

Table 25 Absolute Maximum Ratings

Storage Temperature	-40 °C to +125 °C
1.8 V Supply Voltage (VDDI)	-0.5 V to +2.5 V
3.3 V Supply Voltage (VDDO)	-0.5 to +4.6 V
Input pad tolerance	-2 V < Vpin < VDDO +2 V for 10 ns, 100 mA max
Output pad overshoot limits	-2 V < Vpin < VDDO +2 V for 10 ns, 100 mA max
Voltage on Any Digital Pin	-0.3 V to VDD+0.3 V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead/Ball Temperature	225 +0 –5 °C
Absolute Maximum Junction Temperature	+150 °C

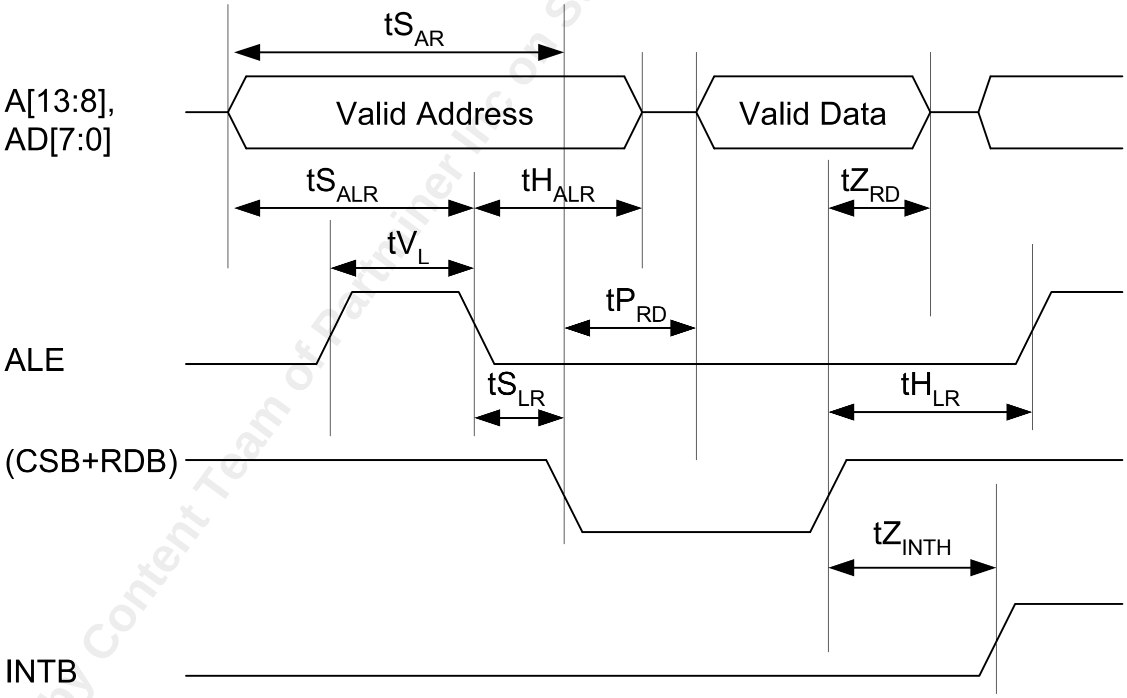
9 Microprocessor Interface Timing

(T_A = -40°C to +85°C, $V_{DDall33}$ = 3.3V ±5%, VDDI18 = 1.8V ±5%)

Table 26 Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	10		ns
tS_{LR}	Latch to Read Set-up	10		ns
tH_{LR}	Latch to Read Hold	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 12 Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

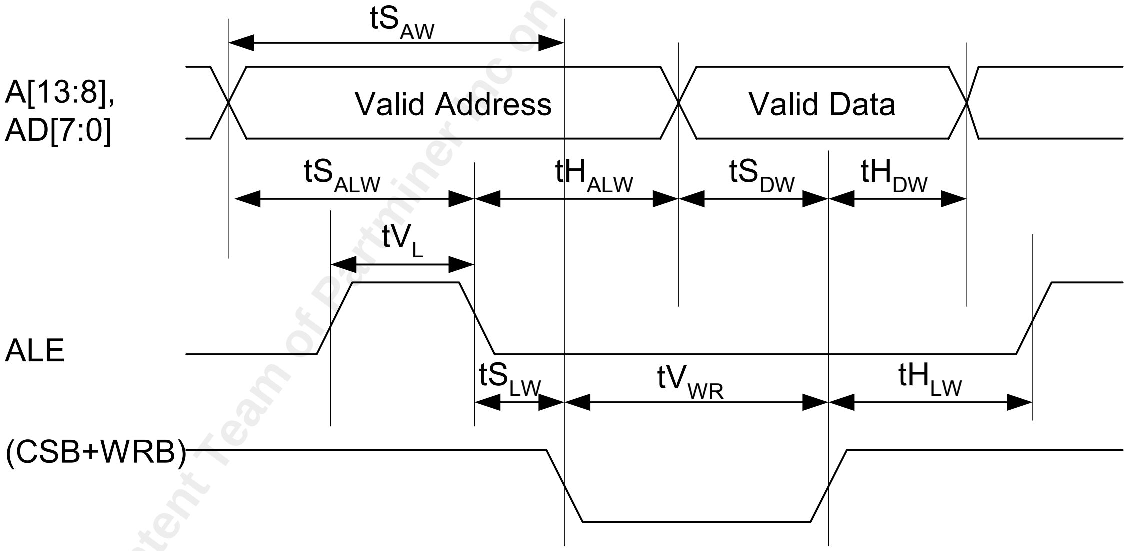
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (AD[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 27 Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	10		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 13 Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
3. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

10 AC Timing Characteristics

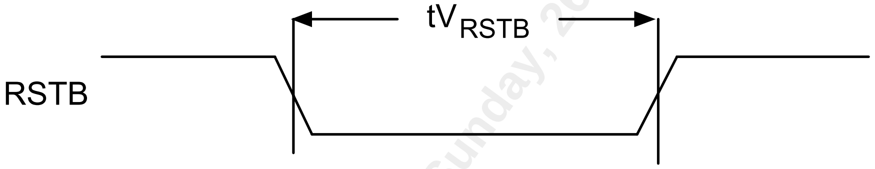
10.1 RSTB Timing

(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, VDDI18 = 1.8V ±5%)

Table 28 RSTB Timing

Symbol	Description	Min	Max	Units
tVRSTB	TRSTB, RSTB Pulse Width	100	—	ns

Figure 14 RSTB Timing



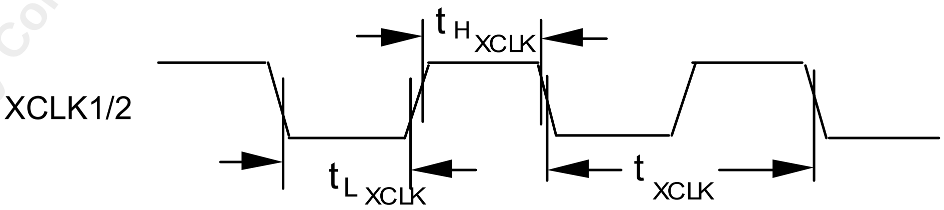
10.2 XCLK1/2 Input Timing

(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, VDDI18 = 1.8V ±5%)

Table 29 XCLK1/2 Input Timing

Symbol	Description	Min	Max	Units
tXCLK	XCLK1/2 Frequency (1.544 MHz or 2.048 MHz ± 50ppm)	1.544 -50ppm	2.048 +50ppm	MHz
tLXCLK	XCLK1/2 Low Pulse Width (Note 1)	160		ns
tHXCLK	XCLK1/2 High Pulse Width (Note 1)	160		ns

Figure 15 XCLK1/2 Input Timing



10.3 SBI TR Timing

(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, VDDI18 = 1.8V ±5%)

Table 30 Clocks and SBI TR Frame Pulse

Symbol	Description	Min	Max	Units
	REFCLK Frequency	19.44 – 50ppm	19.44 +50ppm	MHz
	REFCLK Duty Cycle	40	60	%
tS_{C1FP}	AC1FP, DC1FP Set-Up Time to REFCLK	4		ns
tH_{C1FP}	AC1FP, DC1FP Hold Time to REFCLK	0		ns
tS_{SYNC}	ASYNC, DSYNC Set-Up Time to REFCLK	4		ns
tH_{SYNC}	ASYNC, DSYNC Hold Time to REFCLK	0		ns

Figure 16 SBI TR Frame Pulse Timing

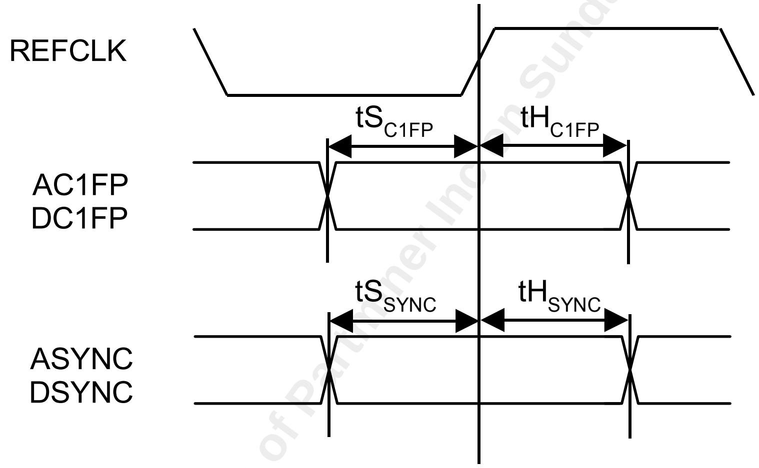


Table 31 SBI TR DROP BUS

Symbol	Description	Min	Max	Units
$tS_{SBITRDROP}$	All SBI TR DROP BUS Inputs Set-up Time to REFCLK	4		ns
$tH_{SBITRDROP}$	All SBI TR DROP BUS Inputs Hold Time to REFCLK	0		ns

Figure 17 SBI TR DROP BUS Input Timing

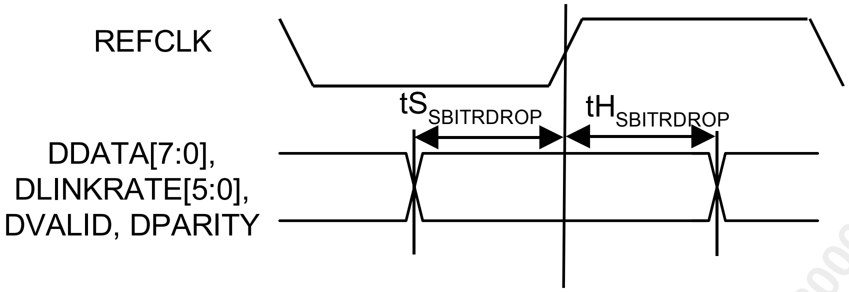
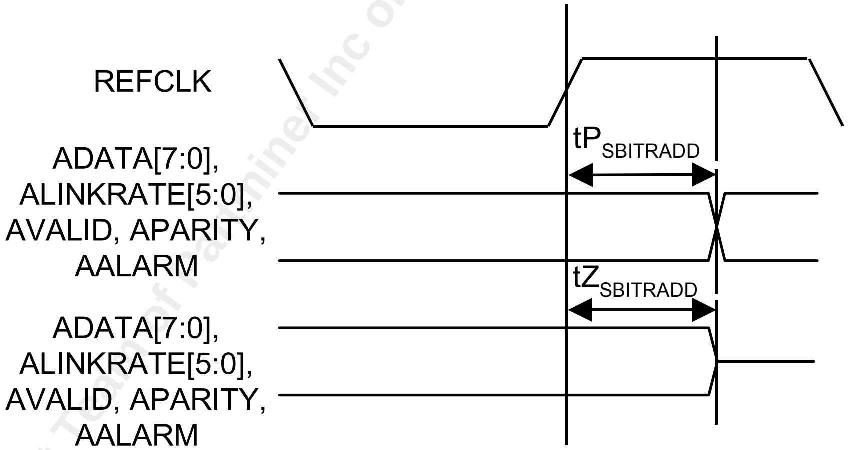


Table 32 SBI TR ADD BUS

Symbol	Description	Min	Max	Units
$tP_{SBITRADD}$	REFCLK to All SBI TR ADD BUS Outputs Valid	2	20	ns
$tZ_{SBITRADD}$	REFCLK to All SBI TR ADD BUS Outputs (except ADATA[7:0] Tri-state	2	17	ns
$tZ_{SBITRADD}$	REFCLK to ADATA[7:0] Tristate	2	17	ns

Figure 18 SBI TR ADD BUS Timing



10.4 SBI Interface

(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, VDDI18 = 1.8V ±5%)

Table 33 Clocks and SBI Frame Pulse

Symbol	Description	Min	Max	Units
	REFCLK Frequency	19.44 – 50ppm	19.44 +50ppm	MHz
	REFCLK Duty Cycle	40	60	%

Symbol	Description	Min	Max	Units
TS_{C1FP}	AC1FP, DC1FP Set-Up Time to REFCLK	4		ns
TH_{C1FP}	AC1FP, DC1FP Hold Time to REFCLK	0		ns
$TP_{C1FPOUT}$	REFCLK to C1FPOUT Valid	1	20	ns

Figure 19 SBI Frame Pulse Timing

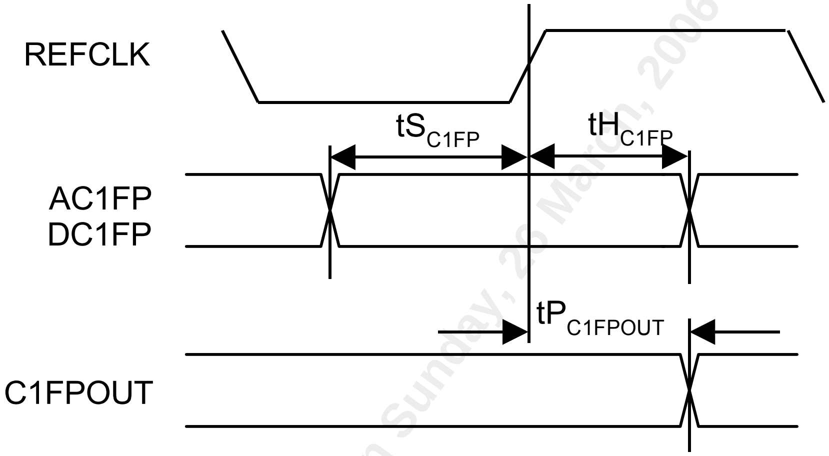


Table 34 SBI DROP BUS

Symbol	Description	Min	Max	Units
tSSBIDROP	All SBI DROP BUS Inputs Set-Up Time to REFCLK	4		ns
tHSBIDROP	All SBI DROP BUS Inputs Hold Time to REFCLK	0		ns

Figure 20 SBI DROP BUS Timing

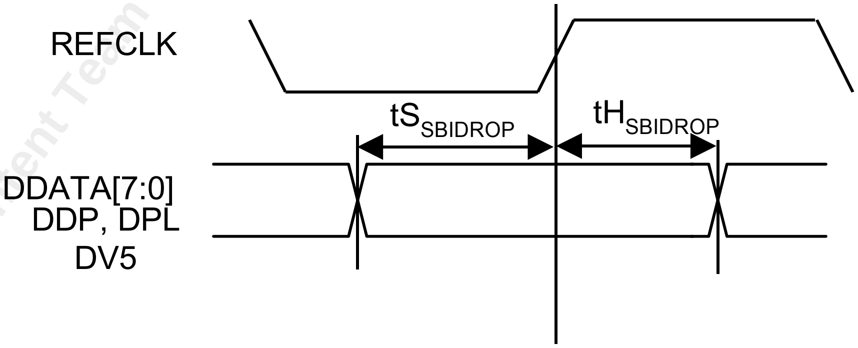
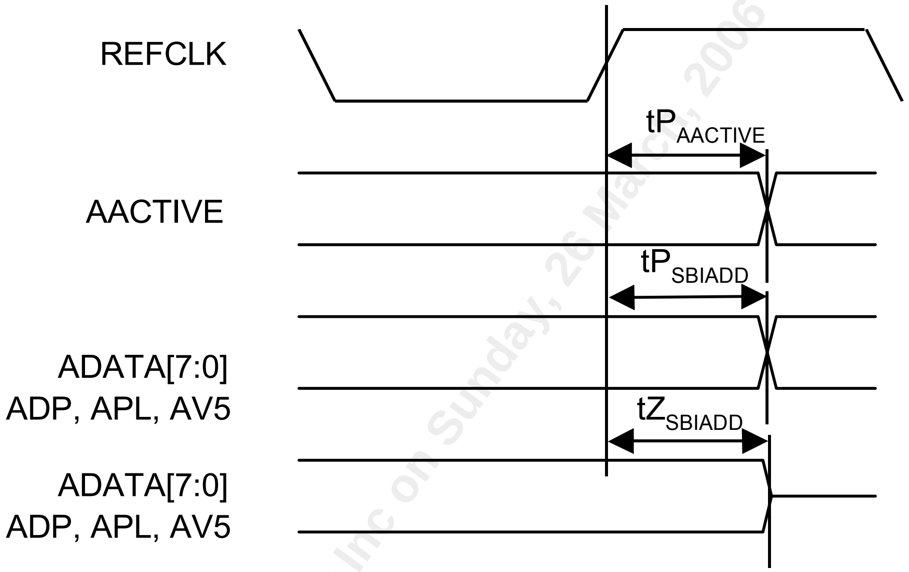


Table 35 SBI ADD BUS

Symbol	Description	Min	Max	Units
$tP_{AACTIVE}$	REFCLK to AACTIVE Valid	2	15	ns

Symbol	Description	Min	Max	Units
tP_{SBIADD}	REFCLK to All SBI ADD BUS Outputs (except AACTIVE) Valid	2	20	ns
tZ_{SBIADD}	REFCLK to All SBI ADD BUS Outputs (except AACTIVE) Tristate	2	20	ns

Figure 21 SBI ADD BUS Timing



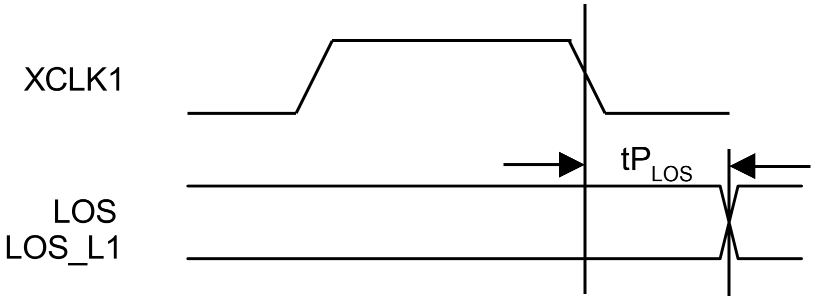
10.5 Alarm Interface

(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, VDDI18 = 1.8V ±5%)

Table 36 Alarm Interface

Symbol	Description	Min	Max	Units
tP_{LOS}	XCLK1 to LOS, LOS_L1 Output Prop. Time	-50	50	ns

Figure 22 Alarm Interface Timing



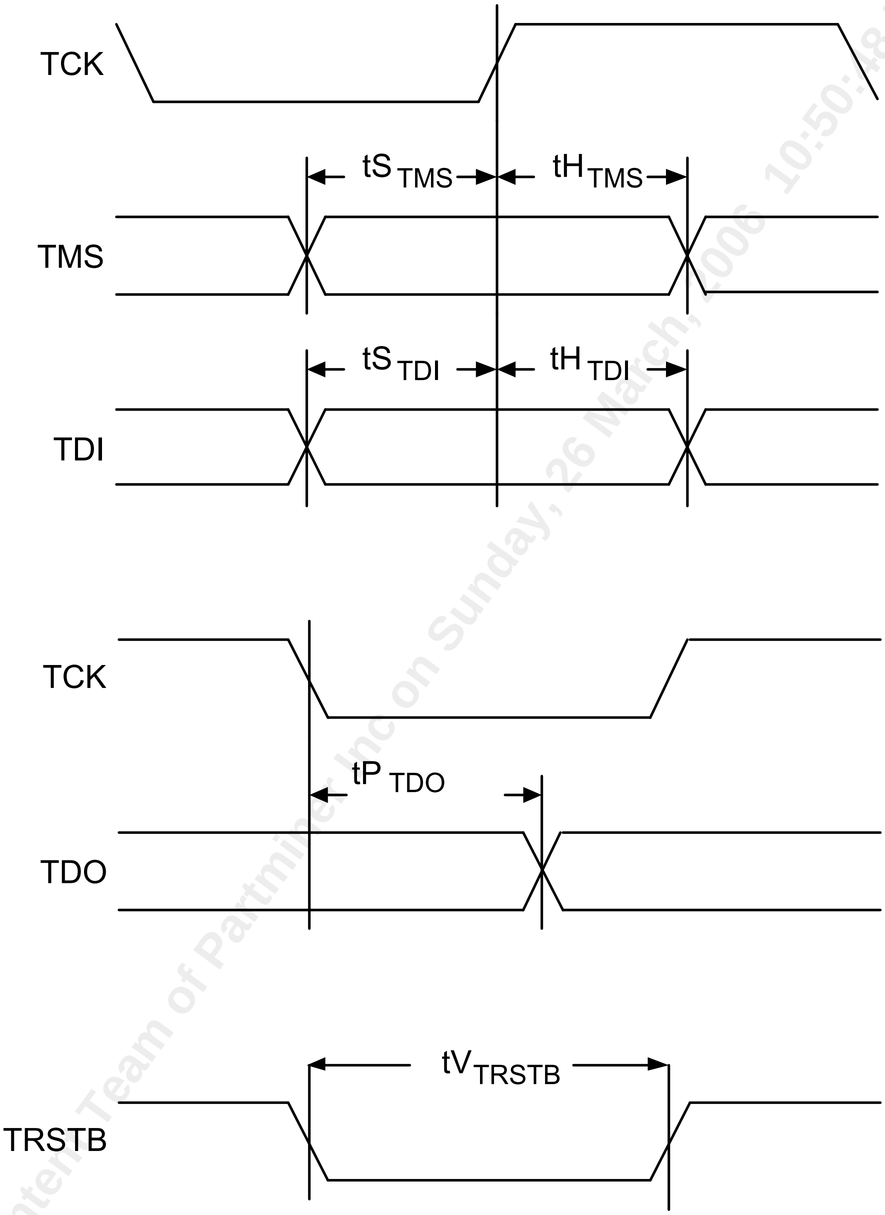
10.6 JTAG Port Interface

(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, VDDI18 = 1.8V ±5%)

Table 37 JTAG Port Interface

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
t_{STMS}	TMS Set-up time to TCK	50		ns
t_{HTMS}	TMS Hold time to TCK	50		ns
t_{STDI}	TDI Set-up time to TCK	50		ns
t_{HTDI}	TDI Hold time to TCK	50		ns
t_{PTDO}	TCK Low to TDO Valid	2	50	ns
t_{VTRSTB}	TRSTB Pulse Width	100		ns

Figure 23 JTAG Port Interface Timing



Notes on HDLIU 32 Timing:

1. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.
2. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
3. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
4. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

5. Maximum output propagation delays are measured with a 100 pF load on the SBI TR/SBI Bus outputs (except AACTIVE) and a 50 pF load on all other outputs. Minimum output propagation delays are measured with a 10 pF load on the outputs.

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