

DSL

Memory Specialties

產品承認書 (APPROVAL SHEET)

公司名稱 (Customer) : _____

客戶料號 (Customer P/N) : _____

產品名稱 (Part Description) : _____ PC-133 128MB 144PIN SO-DIMM

製造原廠 (Manufacture) : _____ Data Specialties Co., Ltd.

商標料號 (P/N) : _____ DSSP16161XH75AB

晶片廠牌 (Chip Brand) : _____ ProMOS (16M*16)

晶片編號 (DRAM P/N) : _____ V54C3256164VJI7

更新日期 (Update date) : _____ 2015/06/12

版本 (Version) : _____ Ver. 1.2

CUSTOMER APPROVAL BY			

DATA SPECIALTIES CO.,LTD.

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DSSP16161XH75AB

128MB PC133 SO-DIMM

Specifications

Density:	128MB	Data Rate:	133 MT/s
Pin Count:	144-pin	CAS Latency:	3
Version:	Un-buffered	Voltage:	3.3V
Type:	SO-DIMM	PCB Layers:	6
Speed:	PC-133	ECC :	Non ECC
Component Config:	16Meg x 16	Module Ranks :	Single Rank

Features

- JEDEC-standard 144 pin, Small-Outline, Dual in line Memory Module (SO-DIMM)
- Serial Presence Detect with EEPROM
- Operating temperature range: 0°C to 70°C
- Fully Synchronous, All Signals Registered on Positive Edge of System Clock
- Single +3.3V (± 0.3V) Power Supply
- All Device Pins are LVTTTL Compatible
- 8192 Refresh Cycles every 64 ms
- Self-Refresh Mode
- Internal Pipelined Operation; Column Address can be changed every System Clock
- Programmable Burst Lengths: 1, 2, 4, 8, Full page
- Auto Precharge and Precharge all Banks by A10
- Data Mask Function (Byte control) by DQMB
- Mode Register Set Programming
- Programmable (CAS Latency: 2, 3 Clocks)
- PCB : Height (1.00 inch), double sided component
- All of Lead-free products are compliant for RoHS

Operating Frequencies

	DSSP16161XH75AB	
	@CL3	@CL2
Maximum Clock Frequency	133MHz (7.5ns)	100MHz (10ns)
CL-tRCD-tRP	3-3-3	2-2-2



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DSSP16161XH75AB

128MB PC133 SO-DIMM

Description

The DSSP16161XH75AB are 16Mx64bits Synchronous DRAM Modules. The modules are composed of eight 16Mx16bits CMOS Synchronous DRAMs in 400mil 54pin TSOP-II package, one 2Kbit EEPROM in 8pin TSSOP package on a 144pin glass-epoxy printed circuit board. The DSSP16161XH75AB Series are Dual In-line Memory Modules suitable for easy interchange and addition of 128Mbytes memory. The DSSP16161XH75AB Series are fully synchronous operation referenced to the positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth.

Absolute maximum ratings

Parameter	Symbol	Value	Unit
Operating ambient temperature	TA	0 ~ +70	°C
Storage temperature	Tstg	-55 ~ +125	°C
Voltage on any pin relative to Vss	Vin , Vout	-0.5 ~ +4.6	V
Supply voltage relative to VSS	VDD, VDDQ	-0.5 ~ +4.6	V

DC Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Power supply	VDD	3.0	3.3	3.6	V
Input high voltage	VIH	2.0	3.0	VDDQ+0.3	V
Input low voltage	VIL	-0.3	0	0.8	V
Output high voltage	VOH	2.4	--	--	V
Output low voltage	VOL	--	-	0.4-	V
Input leakage current	Ii(L)	-10	-	10	uA
Output leakage current	Io(L)	-10	-	10	uA

AC Operating Conditions

Parameter	Symbol	Value	Unit
AC Input High/Low Level Voltage	VIH / VIL	2.4 / 0.4	V
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V



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128MB PC133 SO-DIMM

Pin Description

Pin name	Function	Pin name	Function
A0 to A12	Address input	DQMB0 to DQMB7	Byte input / output mask
	- Row address A0 to A12	CLK0	Clock input
	- Column address A0 to A8	CKE0	Clock enable
BA0/BA1	Bank select address	SDA	Data input/output for SPD
DQ0 to DQ63	Data-input/output	SCL	Clock input for SPD
/CS0	Chip select	VDD	Power supply
/RAS	Row address asserted bank enable	VSS	Ground
/CAS	Column address asserted	NC	No connection
/WE	Write enable	DNU	Do Not Use

Pin Configuration

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VSS	25	DQMB1	49	DQ13	73	NC	97	DQ22	121	DQ24
2	VSS	26	DQMB5	50	DQ45	74	DNU	98	DQ54	122	DQ56
3	DQ0	27	VDD	51	DQ14	75	VSS	99	DQ23	123	DQ25
4	DQ32	28	VDD	52	DQ46	76	VSS	100	DQ55	124	DQ57
5	DQ1	29	A0	53	DQ15	77	NC	101	VDD	125	DQ26
6	DQ33	30	A3	54	DQ47	78	NC	102	VDD	126	DQ58
7	DQ2	31	A1	55	VSS	79	NC	103	A6	127	DQ27
8	DQ34	32	A4	56	VSS	80	NC	104	A7	128	DQ59
9	DQ3	33	A2	57	NC	81	VDD	105	A8	129	VDD
10	DQ35	34	A5	58	NC	82	VDD	106	BA0	130	VDD
11	VDD	35	VSS	59	NC	83	DQ16	107	VSS	131	DQ28
12	VDD	36	VSS	60	NC	84	DQ48	108	VSS	132	DQ60
13	DQ4	37	DQ8	61	CLK0	85	DQ17	109	A9	133	DQ29
14	DQ36	38	DQ40	62	CKE0	86	DQ49	110	BA1	134	DQ61
15	DQ5	39	DQ9	63	VDD	87	DQ18	111	A10/AP	135	DQ30
16	DQ37	40	DQ41	64	VDD	88	DQ50	112	A11	136	DQ62
17	DQ6	41	DQ10	65	/RAS	89	DQ19	113	VDD	137	DQ31
18	DQ38	42	DQ42	66	/CAS	90	DQ51	114	VDD	138	DQ63
19	DQ7	43	DQ11	67	/WE	91	VSS	115	DQMB2	139	VSS
20	DQ39	44	DQ43	68	DNU	92	VSS	116	DQMB6	140	VSS
21	VSS	45	VDD	69	/CS0	93	DQ20	117	DQMB3	141	SDA
22	VSS	46	VDD	70	A12	94	DQ52	118	DQMB7	142	SCL
23	DQMB0	47	DQ12	71	DNU	95	DQ21	119	VSS	143	VDD
24	DQMB4	48	DQ44	72	NC	96	DQ53	120	VSS	144	VDD



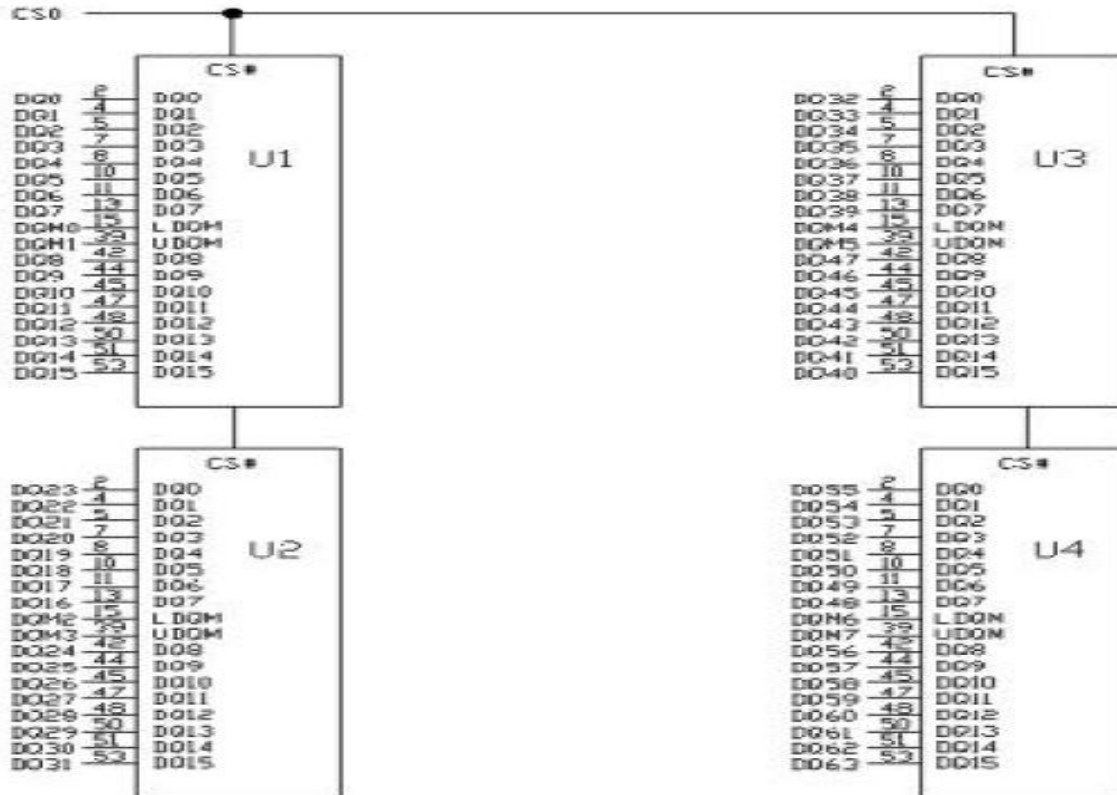
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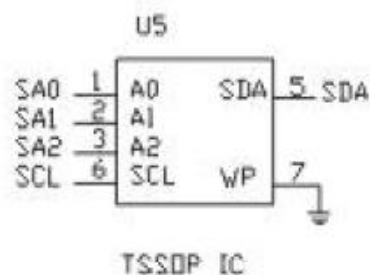
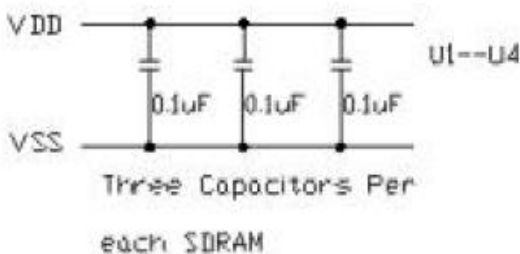
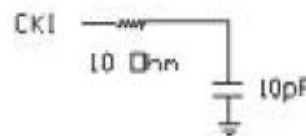
128MB PC133 SO-DIMM

Block Diagram:



- RAS# → SDRAM U1--U4
- CAS# → SDRAM U1--U4
- WE# → SDRAM U1--U4
- A0--AN → SDRAM U1--U4
- BA0--BA1 → SDRAM U1--U4
- CKE0 → SDRAM U1--U4
- DDn → Every DD pin of SDRAM
10 Ohm

Clock wiring		
Clock Input	SDRAMS	LOCATIONS
CK0	4 SDRAMs	U1--U4





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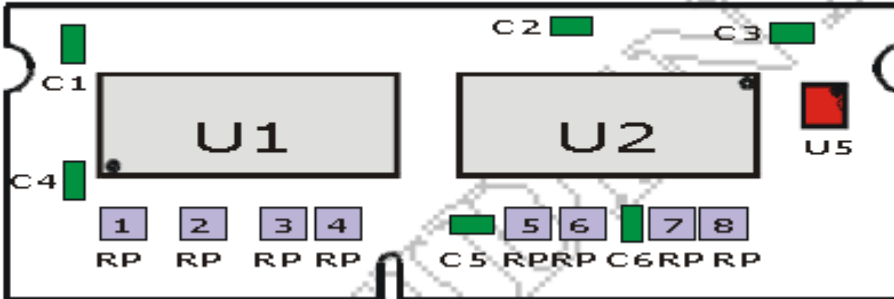
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128MB PC133 SO-DIMM

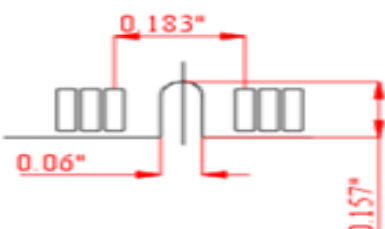
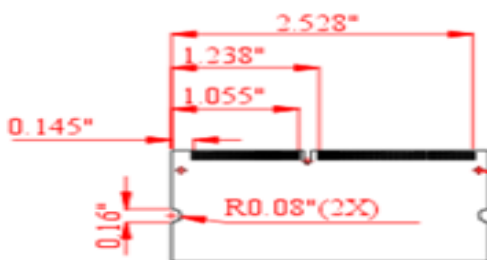
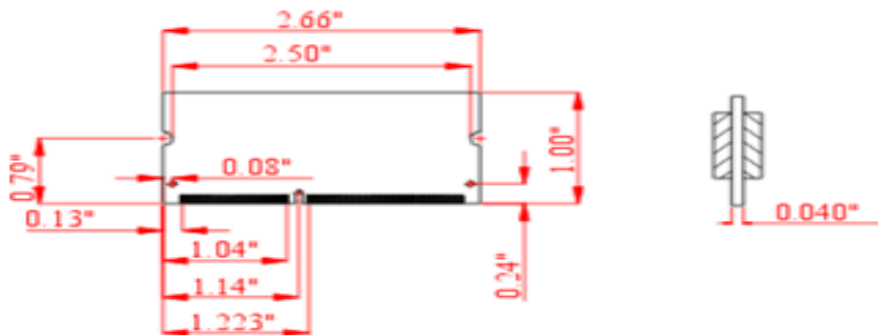
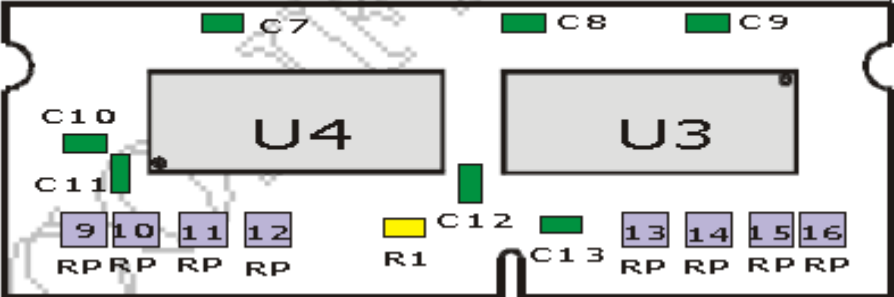
MODULE DIMENSIONS

SDRAM Part No. : ProMOS - V54C3256164VJI7 SDRAM TSOPII

FRONT SIDE 1-BANK



BOTTOM SIDE 1-BANK





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128MB PC133 SO-DIMM

SERIAL PRESENCE DETECT

Byte No.	Function Described	Function Supported	Hex Value
0	Number of Bytes utilized by module manufacturer	128 Bytes	80h
1	Total number of Bytes in SPD device	256 Bytes	08h
2	Memory type	SDRAM	04h
3	Number of row address on this assembly	13	0Dh
4	Number of column address on this assembly	9	09h
5	Number of module rows on this assembly	1Row	01h
6	Data width of this assembly	64 bits	40h
7	Module data width (continued)	--	00h
8	Module voltage interface leaves	LVTTL	01h
9	SDRAM cycle Time @CAS latency of 3	7.5ns	75h
10	SDRAM access time from Clock @CAS Latency of 3	5.4ns	54h
11	Module configuration type	Non-ECC	00h
12	Refresh rate & type	7.8μ s	82h
13	Primary SDRAM width	X16	10h
14	Error checking SDRAM width	Not use	00h
15	Minimum clock delay for back-to back random Column address (tCCD)	1 CLK	01h
16	Burst length supported	1,2,4,8, & full page	8Fh
17	Number of banks on SDRAM device	4 banks	04h
18	CAS latency supported	2,3	06h
19	CS latency	0 CLK	01h
20	WE latency	0 CLK	01h
21	SDRAM module attributes	Non-buffered	00h
22	SDRAM device attributes: General	0E	0Eh
23	SDRAM cycle time @CAS latency of 2	10ns	A0h
24	SDRAM access time @CAS latency of 2	6ns	60h
25	SDRAM cycle time @CAS latency of 1	--	00h
26	SDRAM access time @CAS latency of 1	--	00h
27	Minimum row precharge time (=tRCD)	20ns	14h
28	Minimum row activate to row active delay (=tRP)	15ns	0Fh
29	Minimum RAS to CAS DELAY (=tRRD)	20ns	14h
30	Minimum active precharge time (=tRAS)	45ns	2Dh



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128MB PC133 SO-DIMM

SERIAL PRESENCE DETECT

Byte No	Function Described	Function Supported	Hex Value
31	Module row density	128MB	20h
32	Command and address signal input setup time	1.5ns	15h
33	Command and address signal input hold time	0.8ns	08h
34	Data signal input setup time	1.5ns	15h
35	Data signal input hold time	0.8ns	08h
36to61	Superset information	--	00h
62	SPD Revision code	--	00h
63	Checksum for Bytes 0~62	--	--
64to94	Manufacturer's information	--	00h
95to98	Module serial number	--	00h
99to127	Manufacturer specific data (may be used in future)	Undefined	--
128to225	Open for customer use	Undefined	--

Revision History

Revision	Month	Year	History
1.0	February	2002	Initial Release
1.1	February	2002	Typo Correction
1.2	June	2015	Change IC P/N