

### FEATURES

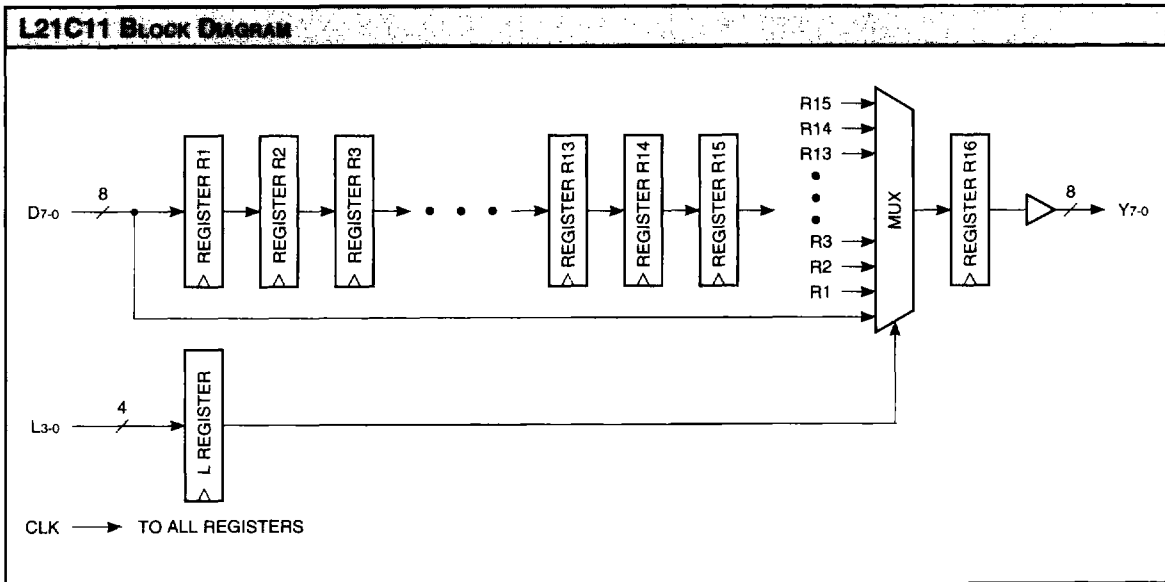
- ❑ Variable Length 8-bit Wide Shift Register
- ❑ Selectable Delay Length from 1 to 16 Stages
- ❑ Low Power CMOS Technology
- ❑ Replaces TRW/Raytheon TMC2111
- ❑ Load, Shift, and Hold Instructions
- ❑ Separate Data In and Data Out Pins
- ❑ DECC SMD No. 5962-96793
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Ceramic DIP
  - 28-pin Plastic LCC, J-Lead
  - 28-pin Ceramic LCC

### DESCRIPTION

The **L21C11** is a high-speed, low power CMOS variable length shift register. It consists of a single 8-bit wide, adjustable length shift register. The shift register can be programmed to any length from 1 to 16 stages inclusive. The length of the shift register is determined by the Length Code (L3-0) as shown in Table 1.

The data input is applied to a chain of registers which are clocked on the rising edge of the CLK input. These registers are numbered R1 through R15. A multiplexer serves to route the contents of any register, R1 through R15, or the data input, D7-0, to the output register, denoted R16. Note that the minimum-length path from data input to output is through R16, consisting of a single stage of delay.

The Length Code (L3-0) controls the number of delay stages applied to the D7-0 inputs as shown in Table 1. When the Length Code is 0, the input is delayed by 1 clock period. When the Length Code is 1, the delay is 2 clock periods, and so forth. The Length Code inputs are latched on the rising edge of CLK. The Length Code value may be changed at any time without affecting the contents of registers R1 through R15.



## 8-bit Variable Length Shift Register

Length Code				Delay
L3	L2	L1	L0	Y7-0
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

### MAXIMUM RATINGS

*Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature .....	-65°C to +150°C
Operating ambient temperature .....	-55°C to +125°C
VCC supply voltage with respect to ground .....	-0.5 V to +7.0 V
Input signal with respect to ground .....	-3.0 V to +7.0 V
Signal applied to high impedance output .....	-3.0 V to +7.0 V
Output current into low outputs .....	25 mA
Latchup current .....	> 400 mA

### OPERATING CONDITIONS

*To meet specified electrical and switching characteristics*

Mode	Temperature Range	Supply Voltage
Active Operation, Com.	0°C to +70°C	4.75 V ≤ VCC ≤ 5.25 V
Active Operation, Mil.	-55°C to +125°C	4.50 V ≤ VCC ≤ 5.50 V

### ELECTRICAL CHARACTERISTICS Over Operating Conditions (Note 4)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	VCC = Min., IOH = -12 mA	2.4			V
VOL	Output Low Voltage	VCC = Min., IOL = 24 mA			0.5	V
VIH	Input High Voltage		2.0		VCC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
Iix	Input Current	Ground ≤ VIN ≤ VCC (Note 12)			±20	µA
ICC1	VCC Current, Dynamic	(Notes 5, 6)		10	20	mA
ICC2	VCC Current, Quiescent	(Note 7)			1.0	mA

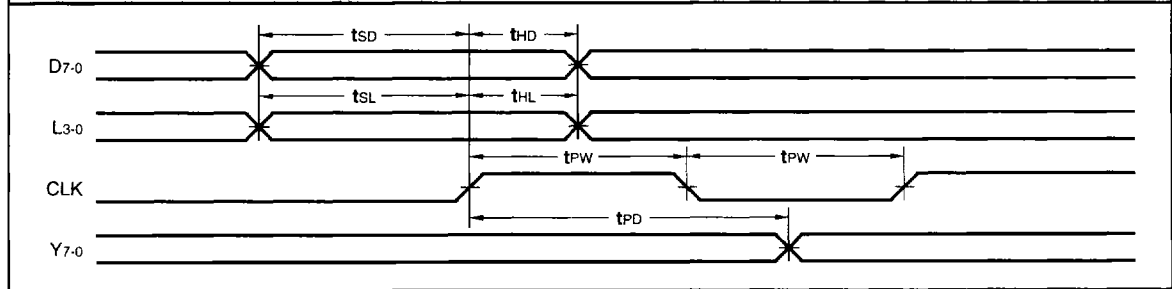
**SWITCHING CHARACTERISTICS**

<b>COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)</b>							
Symbol	Parameter	L21C11-					
		25		20		15	
		Min	Max	Min	Max	Min	Max
t <sub>PD</sub>	Output Delay		25		20		15
t <sub>PW</sub>	Clock Pulse Width	15		12		10	
t <sub>SD</sub>	Data Setup Time	20		10		8	
t <sub>HD</sub>	Data Hold Time	2		0		0	
t <sub>SL</sub>	Length Code Setup Time	20		10		8	
t <sub>HL</sub>	Length Code Hold Time	2		0		0	

<b>MILITARY OPERATING RANGE (-55°C to +125°C) Notes 9, 10 (ns)</b>							
Symbol	Parameter	L21C11-					
		30		25		20	
		Min	Max	Min	Max	Min	Max
t <sub>PD</sub>	Output Delay		30		25		20
t <sub>PW</sub>	Clock Pulse Width	15		12		12	
t <sub>SD</sub>	Data Setup Time	25		10		10	
t <sub>HD</sub>	Data Hold Time	2		2		0	
t <sub>SL</sub>	Length Code Setup Time	25		10		10	
t <sub>HL</sub>	Length Code Hold Time	2		2		0	

**5**

**SWITCHING WAVEFORMS**



**NOTES**

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at -0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of -0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

- N = total number of device outputs
- C = capacitive load per output
- V = supply voltage
- F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tDIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified IOH and IOL at an output voltage of VOH min and VOL max respectively. Alternatively, a diode bridge with upper and lower current sources of IOH and IOL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 μF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.

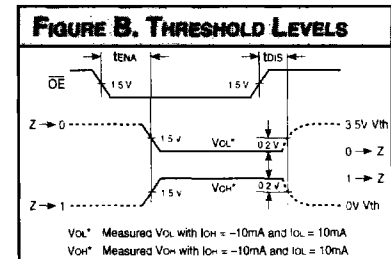
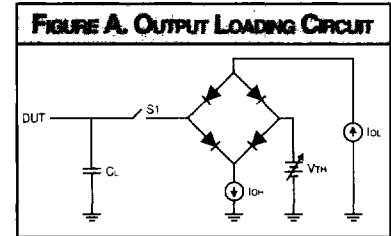
b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the tENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the tDIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

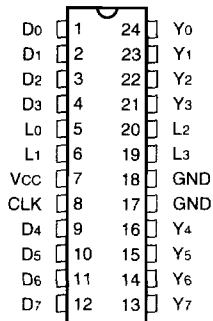
12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.



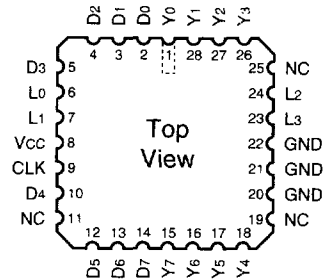
### 8-bit Variable Length Shift Register

#### ORDERING INFORMATION

24-pin — 0.3" wide



28-pin



5

Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)
<b>0°C to +70°C — COMMERCIAL SCREENING</b>				
25 ns	L21C11PC25		L21C11JC25	
20 ns	L21C11PC20		L21C11JC20	
15 ns	L21C11PC15		L21C11JC15	
<b>-55°C to +125°C — COMMERCIAL SCREENING</b>				
30 ns		L21C11CM30		
25 ns		L21C11CM25		
20 ns		L21C11CM20		
<b>-55°C to +125°C — MIL-STD-883 COMPLIANT</b>				
30 ns		L21C11CMB30		L21C11KMB30
25 ns		L21C11CMB25		L21C11KMB25
20 ns		L21C11CMB20		L21C11KMB20