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SSI 32C9001
PC-AT Combo Controller With Reed Solomon, 48 Mbit/s

Advance Information

January 1994

DESCRIPTION

The SSI 32C9001 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. The circuitry of the SSI 32C9001 includes a complete ATA interface, an advanced buffer manager, a high performance disk formatter and an 88-bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9001 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9001 is capable of concurrent transfers of up to 48 megabits per second on the disk interface and 6 megawords (16-bit transfers) per second across the ATA bus. In addition, on-the-fly error corrections and micro controller accesses to the buffer memory will not degrade the throughput during transfers.

The high level of integration within the SSI 32C9001 represents a major reduction in parts count. When the SSI 32C9001 ATA Controller is combined with the

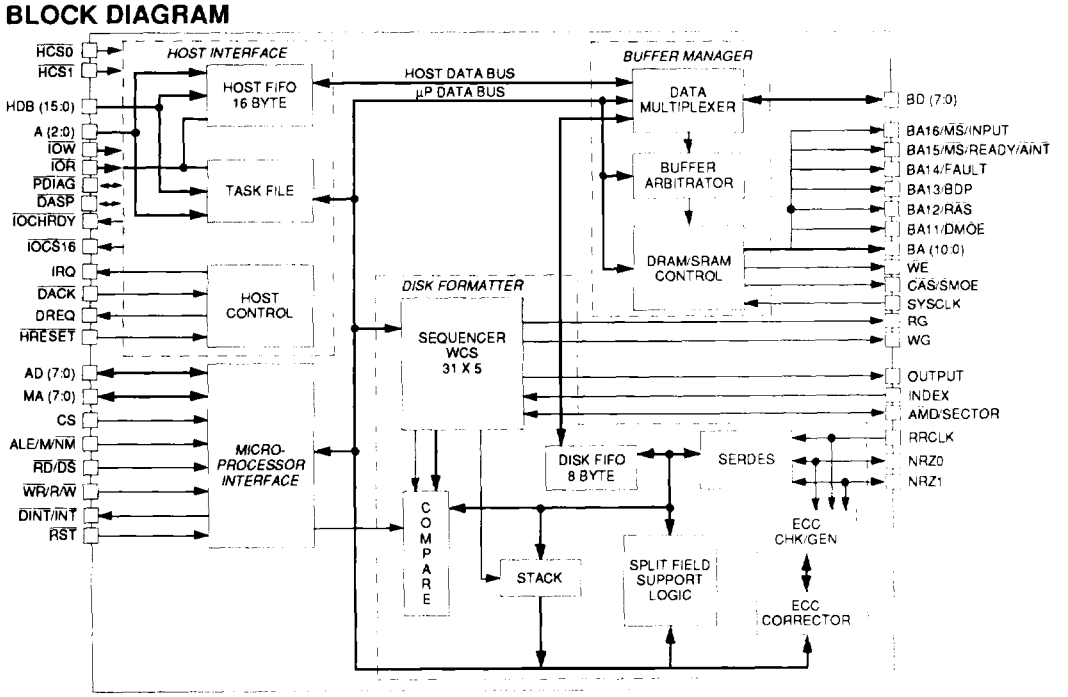
(continued)

FEATURES

- **ATA Interface**
  - **Single Chip PC AT Controller**
  - **Full ANSI ATA Compliance**
  - **Direct PC Bus connection with on board 12 mA drivers**
  - **PC transfers to 6 megawords/second (12 megabytes/second)**
  - **Supports PIO, DMA and multiword DMA (EISA Class B Demand DMA)**
  - **Logic for daisy chaining 2 drives**
  - **Operates as Master, Slave or both**
  - **Automatic command decoding of write, write long, write DMA, write multiple, write buffer and format commands.**
  - **Automatic updates of the host task file registers in both Cyl/Hd/Sec and LBA modes**

(continued)

BLOCK DIAGRAM



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SSI 32C9001
PC-AT Combo Controller
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DESCRIPTION (continued)

SSI 32R2010 Read/Write device, the SSI 32P3000 Pulse Detector, the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, the SSI 32H4631 Servo and Motor Speed Controller, an appropriate micro controller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Hardware support for write-multiple and read-mutiple commands
- Hardware added to provide Multi-Sector data transfers without microprocessor intervention
- Automatic Host Interrupt and Busy for multiple sector transfers
- 16 byte FIFO to improve performance
- Power Down I/O pins

• Buffer Manager
- Direct support of DRAM or SRAM
- SRAM: up to 128k bytes of memory with throughput to 20 megabytes per second
- DRAM: up to 1 megabyte of memory with throughput to 17.78 megabytes per second
- Programmable memory timing
- Supports page mode DRAM access
- Programmable page mode burst length
- Programmable DRAM refresh period
- Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
- Dedicated host, disk and microprocessor address pointers
- Buffer Streaming with internal buffer protection circuit providing buffer integrity

• Disk Formatter
- NRZ Data Rates to 48 megabits per second
- Automatic multi-sector transfer
- Header or microprocessor based split data field support
- Advanced sequencer organized in 31 x 5 bytes
- Advanced branch and interrupt logic
- 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry
- Capable of correcting up to four 10-bit symbols in error

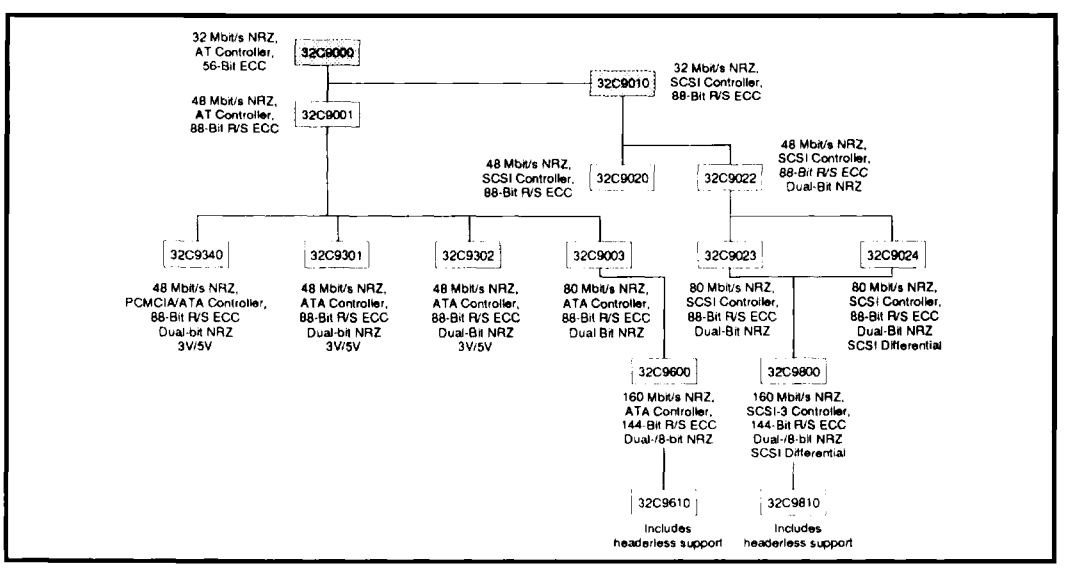

FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of an 11-bit single burst error within a half sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate or combined disk and host interrupts
- Other Features
  - Internal Power Down mode
  - Available in 100-lead TQFP

FUNCTIONAL DESCRIPTION

The SSI 32C9001 contains the following four major functional blocks:

Microprocessor Interface

ATA Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9001 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9001. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9001 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 12 mA drivers allowing for direct connection of the SSI 32C9001 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro controller involvement. The ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the ATA Interface guarantee sustained full speed transfers across the PC AT bus.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The disk interface can be configured through a wide range of capabilities, allowing the SSI 32C9001 to interface with nearly any read/write channel. This allows the user of the SSI 32C9001 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9001 controller and the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32-bit ECC for headers and an 88- bit Reed Solomon code for data. If the checker detects an error using the 88 bit Reed Solomon code, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one quarter of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

The Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9001 can sustain ATA operations at the rate of 6 megawords per second, Disk Formatter operations at 48 megabits per second (6 megabytes per second) and still has sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (O) denotes an output
- (I/O) denotes a bidirectional signal
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — $\overline{AMD}$/SECTOR.

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN
GND		GROUND

HOST INTERFACE

A(2:0)	I	HOST ADDRESS LINES. The Host Address lines A(2:0) are used to access the various PC/AT control/status, and data registers.
$\overline{HCS1}$	I	HOST CHIP SELECT 1. This pin is used to access the control block task file registers.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. This pin is used to access the command block task file resisters.
$\overline{IOCS16}$	OD	16 BIT DATA TRANSFER. An active low output that indicates that a 16-bit transfer is active.
IRQ	O, Z	INTERRUPT REQUEST. Asserted active high to indicate to the Host that the controller needs attention.
IORDY	O, Z	I/O READY. Active low, this signal is asserted to extend the host's I/O cycle.
DREQ	O, Z	DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the controller to initiate DMA Transfers.
$\overline{DACK}$	I	DMA ACKNOWLEDGE. This active low signal is used during DMA to transfer data between the host and the controller.
$\overline{IOR}$	I	INPUT READ SELECT. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or DACK, data from the device is enabled onto the host data bus.
$\overline{IOW}$	I	INPUT WRITE SELECT. Asserted active low by the Host during a Host write operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or DACK, data from the host data bus is strobed into the device.

HOST INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{HRESET}}$	I	HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers — see Design Guide for Register Reset conditions. This signal can also "wake up" the device while it is in power down mode.
HDB (15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; note that for transferring commands, status or ECC only bits (7:0) are used.
$\overline{\text{PDIAG}}$	I, OD	PASSED DIAGNOSTICS. This active low pin is used as the passed diagnostics signal, and may be an input or an open-drain output.
$\overline{\text{DASP}}$	I, OD	DRIVE ACTIVE-SLAVE PRESENT. This pin is used as the Drive Active/Slave Present signal, and is an input or an open-drain output. This pin is used for Master/Slave drive communication and/or for driving an LED.

DISK INTERFACE

INDEX/INPUT	I	INDEX/INPUT. This pin serves as the index function for the disk sequencer. When the INPUT function is not available on the BA 15 pin, this pin can function as input or index.
OUTPUT	O	DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{\text{AMD}}$/SECTOR	I/O	ADDRESS MARK DETECT/SECTOR. In Hard Sector mode, this is the input for the sector pulse from the disk drive. In Soft Sector mode, a low-level input during a read indicates an address mark was detected.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted by the sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9001 device. This input must be glitch-free to ensure correct operation of the chip.
NRZ0	I/O	NRZ BIT 0. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. This pin is used for the least significant bit in dual bit NRZ mode; it is used for the serial data stream in single bit NRZ mode.
NRZ1	I/O	NRZ BIT1. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. This pin is used for the most significant bit in dual bit NRZ mode; it is not used in single bit NRZ mode.

PIN DESCRIPTION (continued)

MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the SSI 32C9001 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/$\overline{M}$/NM	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high, the microprocessor interface is configured as non-multiplexed. When driven low, the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Multiplexed address/data bus mode, when an active low signal is present with CS signal asserted high, the data on the AD0:7 is written to the internal registers. In the Non-Multiplexed address/data bus mode, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a write operation. See table below.

CS	$\overline{WR}$/R/$\overline{W}$	$\overline{RD}$/DS	Mux/Non-Mux	Action
High	Low	High	Intel Multiplexed	Write to internal registers.
High	High	Low	Intel Multiplexed	Read from internal registers.
High	Low	High	Motorola Multiplexed	Write to internal registers.
High	Low	Low	Non-Multiplexed	Write to internal registers.
High	High	High	Motorola Multiplexed	Read from internal registers.
High	High	Low	Non-Multiplexed	Read from internal registers.
Low	X	X	M or N	No action.

Note: X denotes don't care.

$\overline{RD}$/$\overline{DS}$	I	READ STROBE/DATA STROBE. In the Multiplexed address data bus mode, when an active low signal is present with CS signal high, internal registers will be accessed. In the Non-Multiplexed address data mode, this signal acts as the DS signal. A high on R/$\overline{W}$, with the CS and DS signals asserted, indicates a read operation. A low on the R/$\overline{W}$ signal, with the DS and the CS symbols asserted, indicates a write operation to the internal registers. Note: DS is active high in multiplexed mode, active low in non-multiplexed.
$\overline{DINT}$/$\overline{INT}$	O, OD	INTERRUPT. This signal is an interrupt line to the microprocesor. It is the combined interrupt line of the disk side and host side interrupts when pin RDY/$\overline{AINT}$ is programmed as ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as an open drain output. May be programmed as active high or low; reset state is active low.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed address data mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-Multiplexed Microprocessors mode, these lines are bidirectional data lines only.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS. This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the address phase of a Multiplexed address data type microprocessor cycle. These signals are the address input when used with a non-multiplexed bus microprocessor.

BUFFER MANAGER INTERFACE

BA16/$\overline{MS}$/INPUT	I/O	BUFFER ADDRESS 16/MEMORY SELECT/DISK INPUT. In SRAM mode, this pin may be configured as buffer address 16, memory select, or as the input pin to the disk sequencer. In DRAM mode, this pin is configured as the input pin. If the input function is not available on this pin, then the INDEX pin may be used for the index function or the input function.
BA15/$\overline{MS}$/READY/$\overline{AINT}$	O	BUFFER ADDRESS 15/MEMORY SELECT/AT INTERRUPT/READY. In SRAM mode, this pin may be configured as buffer address 15, memory select, as a separate local microprocessor interrupt for the host interface, or as the ready function for adding wait states to local microprocessor accesses. In DRAM mode, AT interrupt or Ready may be selected. After $\overline{RST}$ is asserted, this signal is configured as Ready.
BA14/FAULT	I/O	BUFFER MEMORY ADDRESS 14/DISK FAULT. This signal is used for addressing the buffer memory in SRAM mode, or as the disk fault pin in DRAM mode. Assertion of the fault pin will cause the disk sequencer to halt immediately.
BA13/BDP	I/O	BUFFER MEMORY ADDRESS 13/BUFFER MEMORY PARITY. This signal is used for addressing the buffer memory in SRAM mode, or as the buffer data parity value in DRAM mode.
BA12/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 12/ROW ADDRESS STROBE: This signal is used for addressing the buffer memory in SRAM mode or as the row address strobe in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA11/$\overline{DMOE}$	O	BUFFER MEMORY ADDRESS 11/DRAM MEMORY OUTPUT ENABLE. This signal is used for addressing the buffer memory in SRAM mode, or as the memory output enable pin in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA(10:0)	O	BUFFER MEMORY ADDRESS LINES. These are signals 10-0 for addressing the buffer memory.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. These eight signals are bits 7-0 of the 8-bit parallel data lines to/from the buffer memory. Note that BD6 is used to select between the Intel- and Motorola-style microprocessor interfaces. If BD6 is externally pulled up when $\overline{RST}$ is asserted, Intel mode is used; if BD6 is externally pulled down when $\overline{RST}$ is asserted, Motorola mode is used.

PIN DESCRIPTION (continued)

BUFFER MANAGER INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{CAS}$/SMOE	O	COLUMN ADDRESS STROBE/SRAM MEMORY OUTPUT ENABLE. This signal is used as the column address strobe in DRAM mode, or the memory output enable in SRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
$\overline{WE}$	O	MEMORY OUTPUT ENABLE. This active low output signal is used to strobe the data into the RAMs from the DAta bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable WE, and memory output enable MOE. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC + 0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Power Supply Voltage		4.5		5.5	V
ICC Supply Current				50	mA
ICCS Supply Current	Note 1			250	µA
VIL Input Low Voltage		-0.5		0.8	V
VIH Input High Voltage		2		VCC+0.5	V
VOL Output Low Voltage IOL = 2 mA	Note 2			0.4	V
VOL Output Low Voltage IOL = 24 mA	Note 3			0.5	V
VOH Output High Voltage IOH = -400 µA		2.4			V
IL Input Leakage Current 0 < VIN < VCC		-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

ELECTRICAL CHARACTERISTICS (continued)

Note: (1) 4DH bit 6, 87H bits 4 and 3 set. RRCLK and SYSCLK internally inhibited.
(2) All interface pins except Host Interface pins.
(3) Host Interface pins.

MULTIPLEXED BUS MICROPROCESSOR INTERFACE TIMING PARAMETERS (FIGURES 2 THROUGH 5)

Ta	Ale Width		20			ns
Tma	Address valid to MA0:7 valid				30	ns
Tr	$\overline{RD}$ Width		80			ns
As	Address Valid to ALE ↓		5			ns
Ah	ALE ↓ to Address Invalid		10			ns
Cs	CS Valid to $\overline{RD}$ ↓ or $\overline{DS}$ ↓		20			ns
Ch	$\overline{RD}$ ↑ or $\overline{DS}$ ↑ to CS ↓		0			ns
Tda	$\overline{RD}$ ↓ or DS ↓ to Read Data Valid	Except Read of WCS			30	ns
	$\overline{RD}$ ↓ or DS ↓ to Read Data Valid	Read of WCS			50	ns
Tds	$\overline{DS}$ width		80			ns
Tdh	$\overline{RD}$ ↑ or $\overline{DS}$ ↑ to Read Data Invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to $\overline{DS}$ ↓		20			ns
Thrw	$\overline{DS}$ ↑ to R/W Invalid		20			ns
Tdrdy	$\overline{RD}$ ↓ to READY ↓ (Intel) or $\overline{DS}$ ↓ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or $\overline{DS}$ ↑		40			ns
Wdh	$\overline{WR}$ ↑ or $\overline{DS}$ ↑ to write data invalid		10			ns
Note:	↑ indicates rising edge	↓ indicates falling edge				

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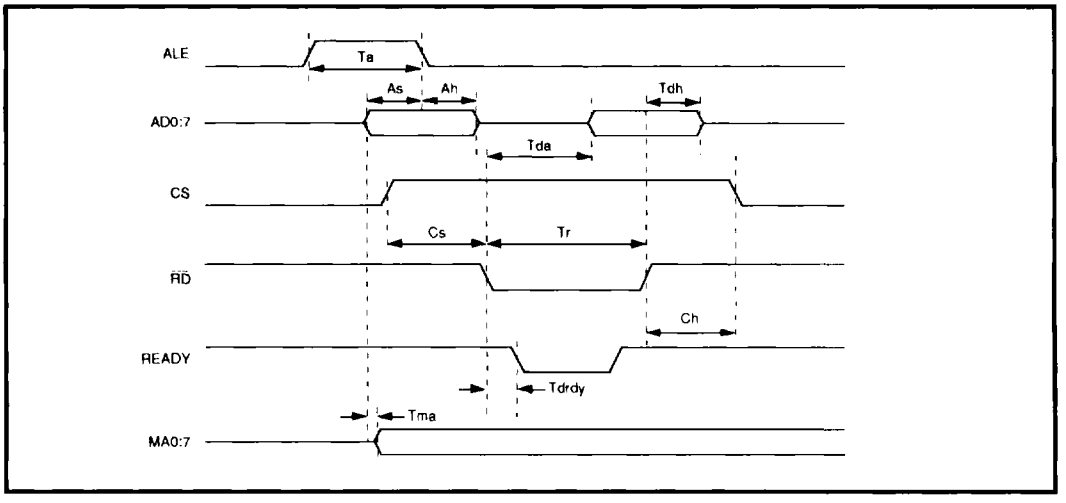

FIGURE 2: Intel Register Read Timing

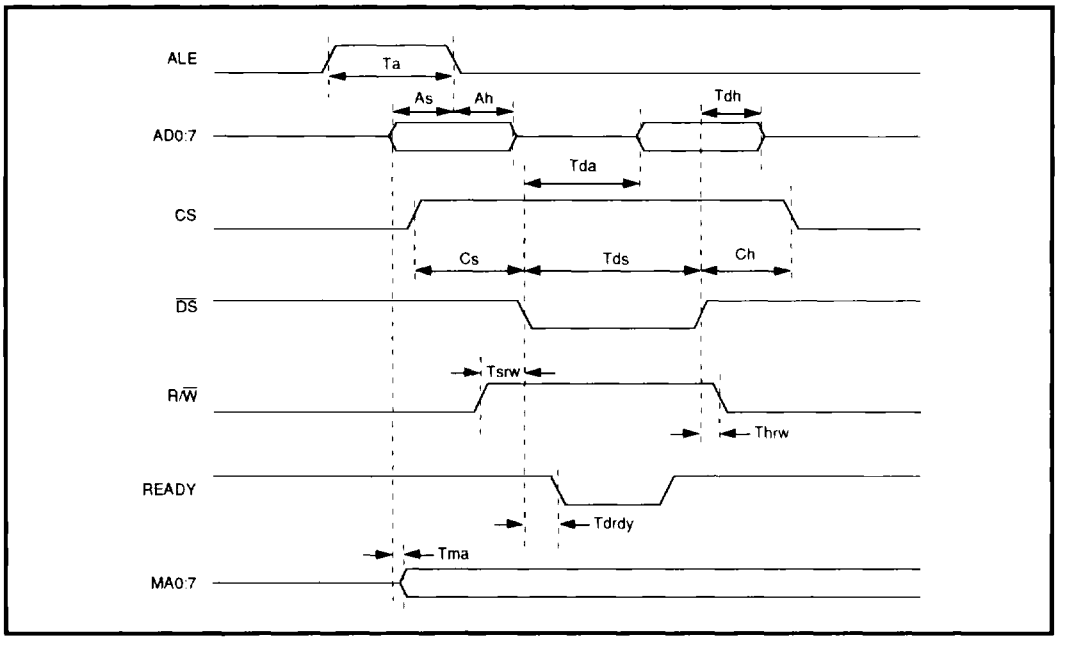

FIGURE 3: Motorola Register Multiplexed Read Timing

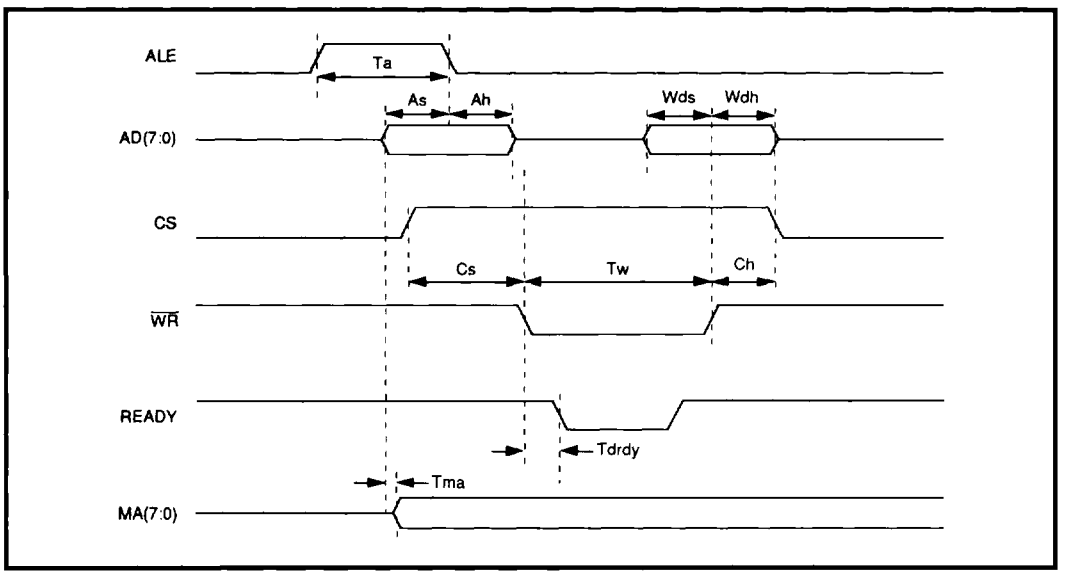

FIGURE 4: Intel Register Multiplexed Write Timing

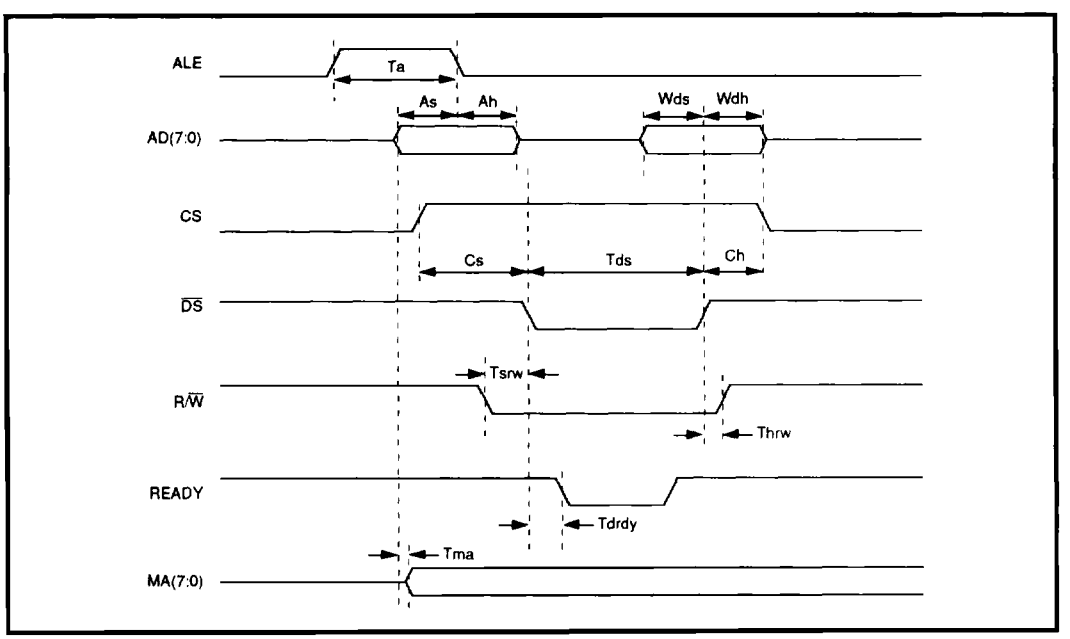

FIGURE 5: Motorola Register Multiplexed Write Timing

ELECTRICAL SPECIFICATIONS (continued)

NON-MULTIPLEXED BUS MICROPROCESSOR INTERFACE TIMINGS (FIGURE 6)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Tmas	MA(7:0) valid to $\overline{DS}$ ↑		5			ns
Tmah	$\overline{DS}$ ↓ to MA(7:0) invalid		5			ns
Cs	CS valid to $\overline{DS}$ ↑		20			ns
Ch	$\overline{DS}$ ↓ to CS ↓		0			ns
Tda	$\overline{RD}$ ↓ or DS ↓ to Read Data Valid	Except Read of WCS			30	ns
	$\overline{RD}$ ↓ or DS ↓ to Read Data Valid	Read of WCS			50	ns
Tds	DS width		80			ns
Tdh	$\overline{DS}$ ↓ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to $\overline{DS}$ ↑		20			ns
Thrw	DS ↑ to R/$\overline{W}$ invalid		20			ns
Tdrdy	$\overline{DS}$ ↑ to READY ↓ (Motorola) Note 3				30	ns
Wds	Write data valid to R/$\overline{W}$ ↑ or $\overline{DS}$ ↓		40			ns
Wdh	R/$\overline{W}$ ↑ or $\overline{DS}$ ↓ to write data invalid		10			ns

Note 1: ↑ indicates rising edge ↓ indicates falling edge

Note 2: Loading capacitor = 30pF

Note 3: Ready is not shown and is not used by Motorola processors. Timing provided for information only.

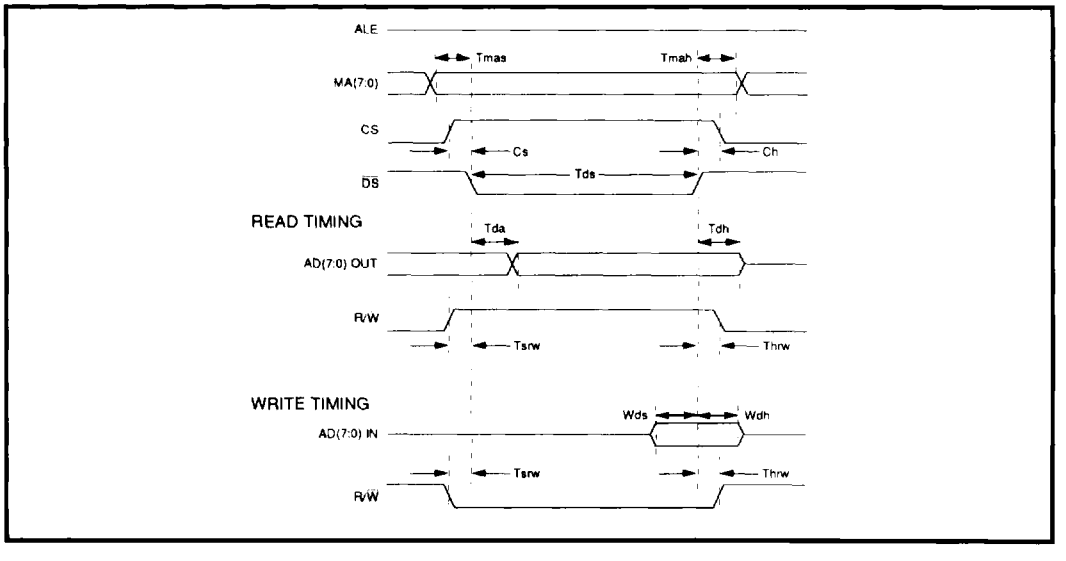

FIGURE 6: Non-Multiplexed Bus Timing Diagrams

DISK READ/WRITE TIMING (FIGURES 7 AND 8)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
T	RRCLK	Single bit NRZ	20.8			ns
		Dual bit NRZ	41			ns
T/2	RRCLK high/low time	Single bit NRZ	8.5			ns
		Dual bit NRZ	16			ns
Tr = Tf	RRCLK rise and fall time		0		2	ns
Ds	NRZ in valid to RRCLK ↑		3			ns
Dh	RRCLK ↑ to NRZ in invalid		4			ns
As*	$\overline{AMD}$ valid to RRCLK ↑		3			ns
Dv	RRCLK ↑ to NRZ out		3		20	ns
Wv*	RRCLK ↑ to WAM out		3		20	ns

Note: ↑ indicates rising edge ↓ indicates falling edge

* These specifications are only applicable in the Soft Sector mode.

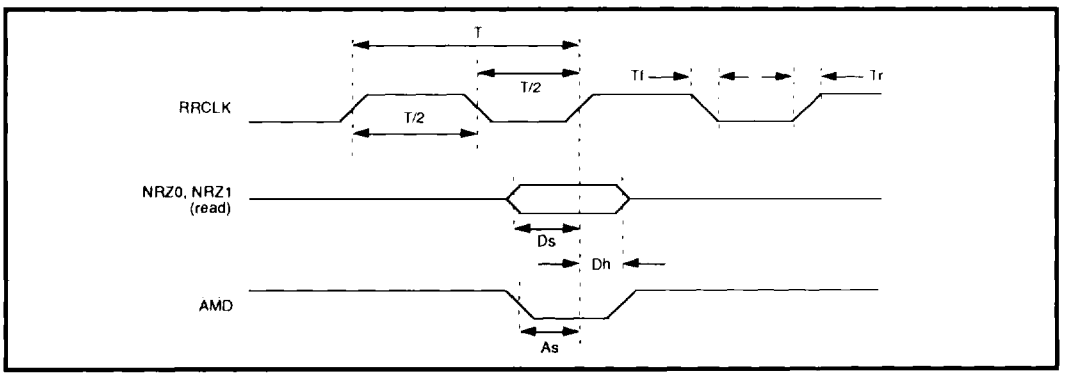

FIGURE 7: Disk Read Timing

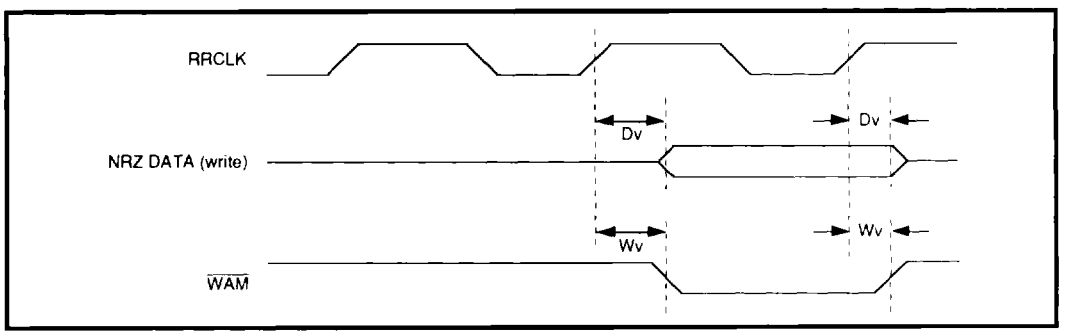

FIGURE 8: Disk Write Timing

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ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (FIGURES 9 THROUGH 13)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
T	SYSCLK period		25			ns
T/2	SYSCLK high/low time		10			ns
Tav	SYSCLK ↑ to address valid	Note 1			18	ns
Tmsv	SYSCLK ↑ to $\overline{MS}$↓	Notes 1, 6			18	ns
Tmsh	SYSCLK ↑ to $\overline{MS}$↑	Note 1			18	ns
Tmv	SYSCLK ↑ to $\overline{MOE}$↓	Note 1			18	ns
Tmh	SYSCLK ↑ to $\overline{MOE}$↑	Note 1			18	ns
Twv	SYSCLK ↑ to $\overline{WE}$↓	Note 1			18	ns
Twh	SYSCLK ↑ to $\overline{WE}$↑	Note 1			18	ns
Tdov	SYSCLK ↑ to data out valid	Note 1			18	ns
Tdoh	SYSCLK ↑ to data out invalid	Note 1			18	ns
Tdis	Data in valid to $\overline{MOE}$ ↑ (SRAM)		5			ns
	Data in valid to $\overline{CAS}$ ↑ (DRAM)		5			ns
Tdih	$\overline{MOE}$ ↑ to data in valid (SRAM)		0			ns
	$\overline{CAS}$ ↑ to data in valid (DRAM)		0			ns
Trv	SYSCLK ↑ to $\overline{RAS}$↓	Note 1			18	ns
Trh	SYSCLK ↑ to $\overline{RAS}$↑	Note 1			18	ns
Trav	SYSCLK to row address valid	Note 1			18	ns
Trah	SYSCLK ↑ to row address invalid	Note 1			18	ns
Tcv	SYSCLK ↑ to $\overline{CAS}$↓	Note 1			18	ns
Tch	SYSCLK ↑ to $\overline{CAS}$↑	Note 1			18	ns
Tcav	SYSCLK ↑ to column address valid	Note 1			18	ns
Tcah	SYSCLK ↑ to column address invalid		0			ns

BUFFER MEMORY READ/WRITE FUNCTIONAL PARAMETERS (FIGURES 9 THROUGH 13) (continued)

PARAMETER		CONDITIONS	MIN	UNIT
Trwl	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 3	((RWL + 3)•T)	ns
Trwh	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 4	((RWH + 1)•T)	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Note 2	((CWL + 1)•T)	ns
Tcwl	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Notes 2, 5	((CWL + 1)•T)	ns

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±2 ns.

Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memeory access cycle except when multiple page mode accesses are performed. When multiple page mdoe accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the ocmpletion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.

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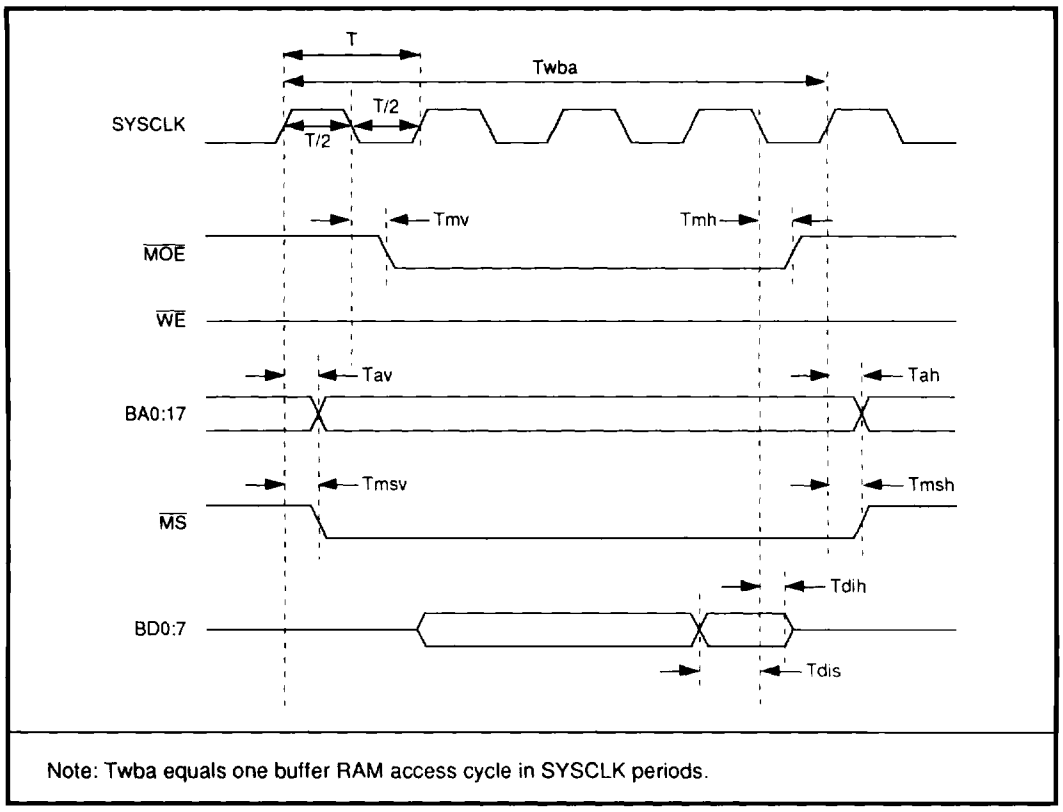
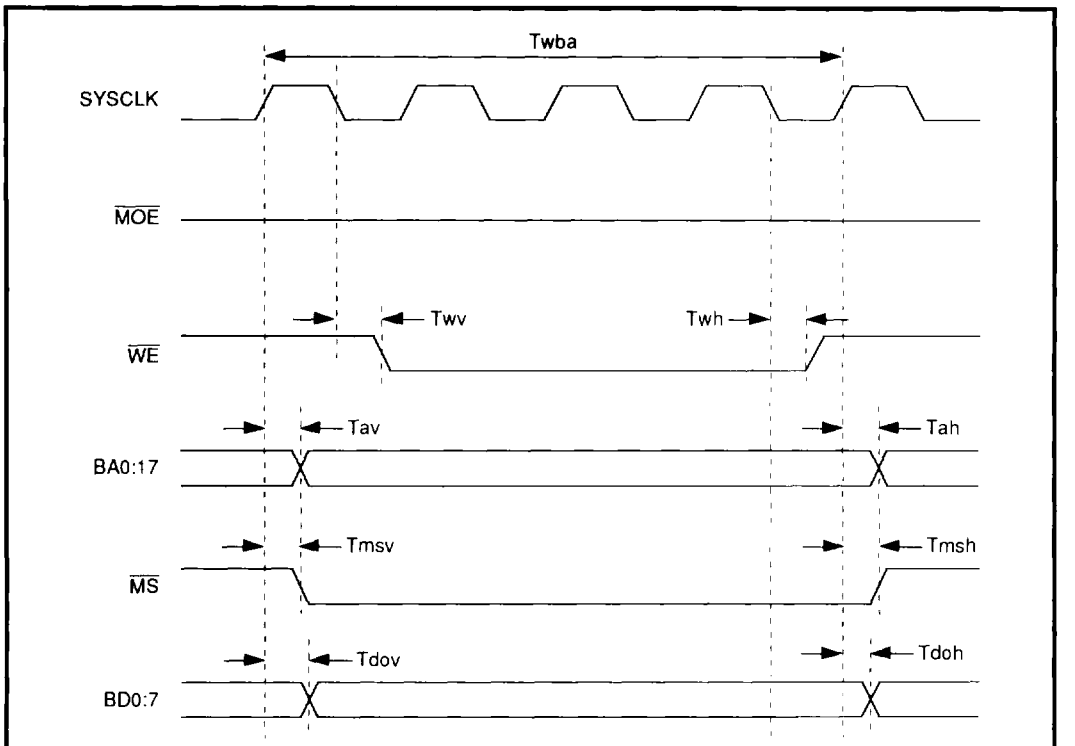


Note: Twba equals one buffer RAM access cycle in SYSCLK periods.

FIGURE 9: SRAM Read Timing



Note: Twba equals one buffer RAM access cycle in SYSCLK periods.

FIGURE 10: SRAM Write Timing

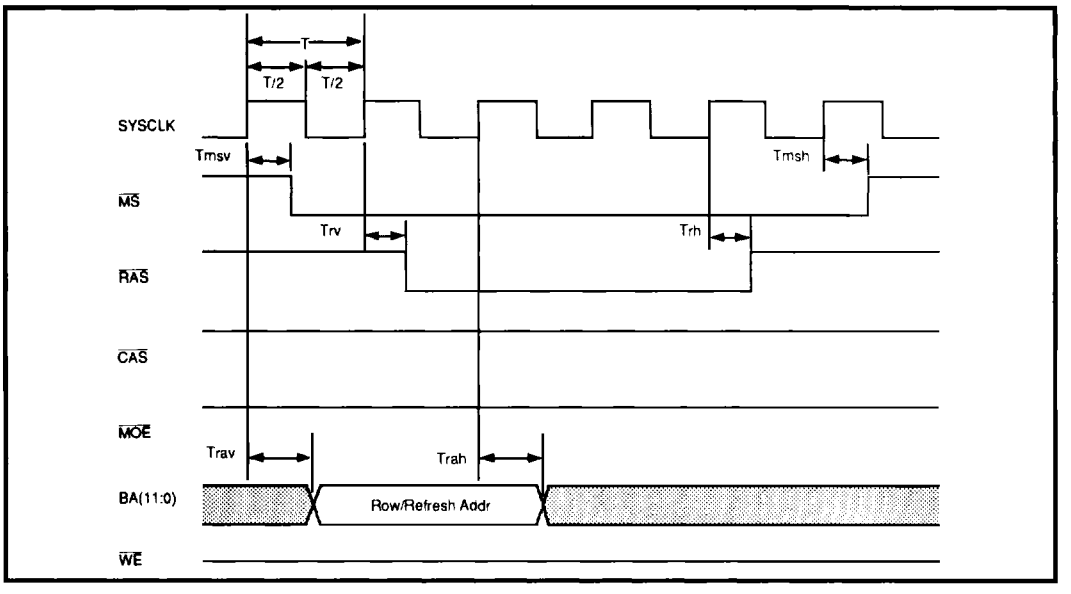


FIGURE 11: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

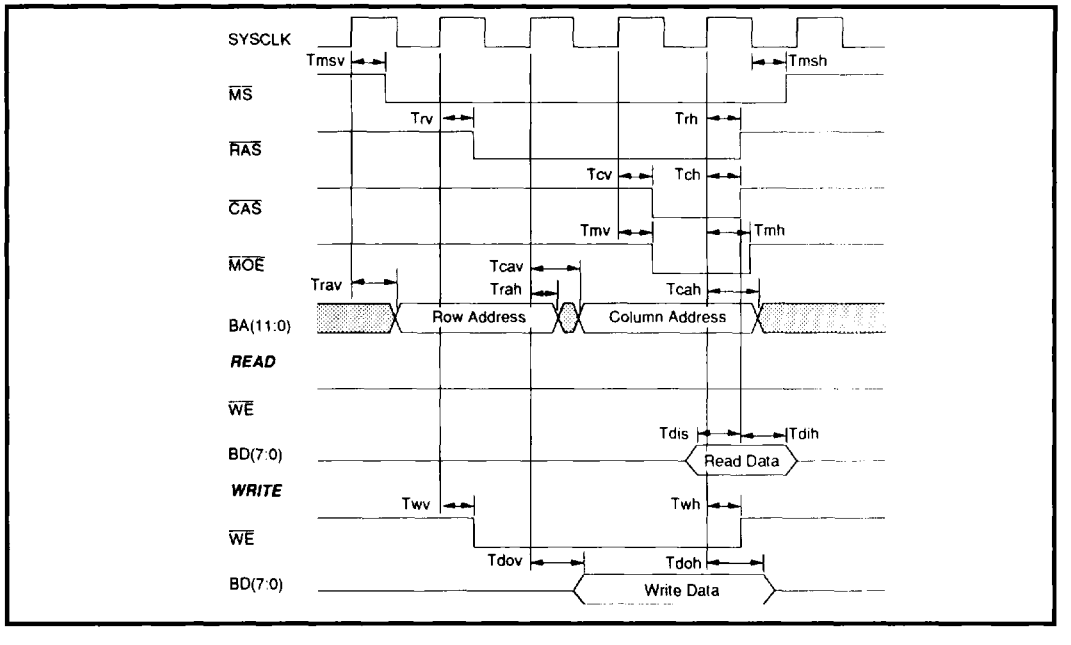


FIGURE 12: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)

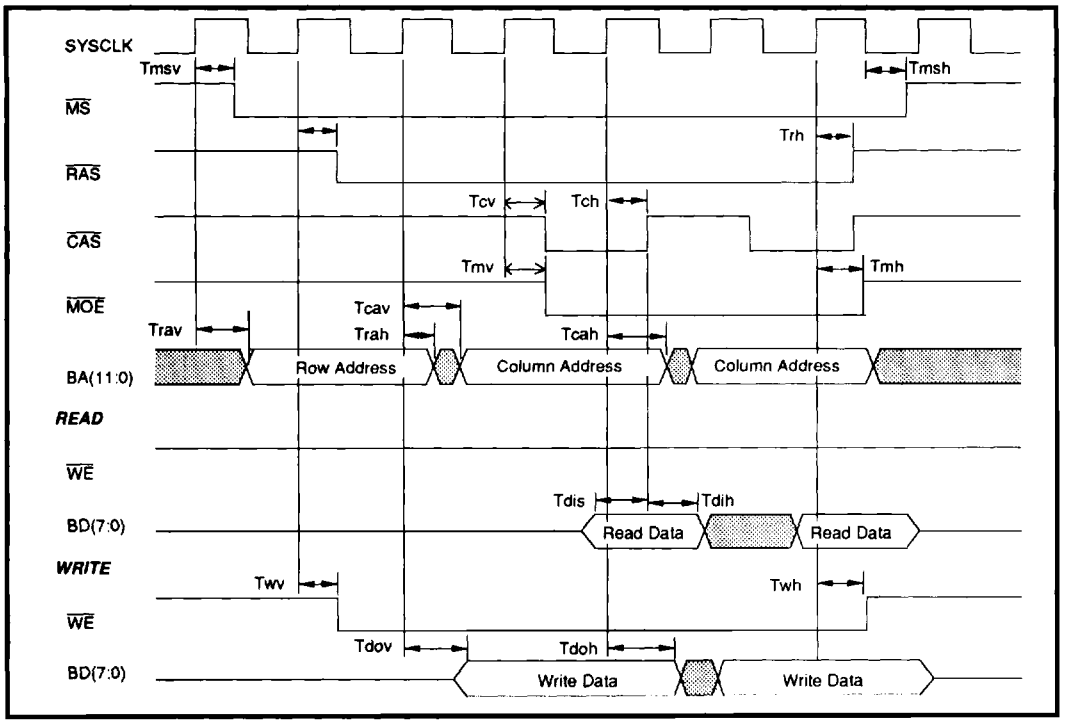


FIGURE 13: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)

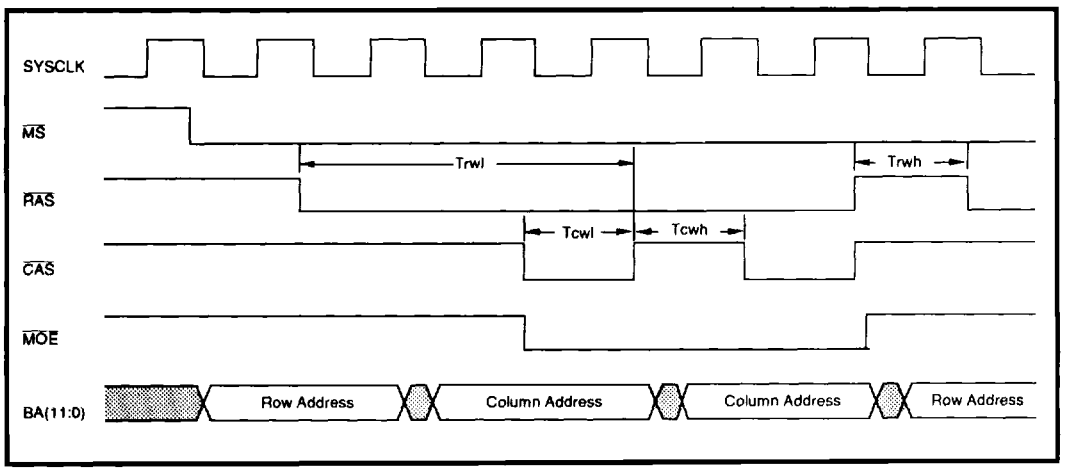


FIGURE 14: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)

ELECTRICAL SPECIFICATIONS (continued)

HOST DMA 8/16-BIT INTERFACE TIMING PARAMETERS (FIGURE 15)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
DREQL	DREQ ↓ from $\overline{DACK}$ ↓				40	ns
RDTA	$\overline{IOR}$ ↓ to HD[0:15] valid				50	ns
RDHLD	$\overline{IOR}$ ↑ to HD[0:15] tri-state		2		25	ns
WDS	HD[0:15] setup to $\overline{IOW}$ ↑		30			ns
WDHLD	HD[0:15] hold from $\overline{IOW}$ ↑		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		80			ns
DMASET	$\overline{DACK}$ ↓ to $\overline{IOR}$/$\overline{IOW}$ ↓		0			ns
DMAHLD	$\overline{DACK}$ hold from $\overline{IOR}$/$\overline{IOW}$ ↑		0			ns

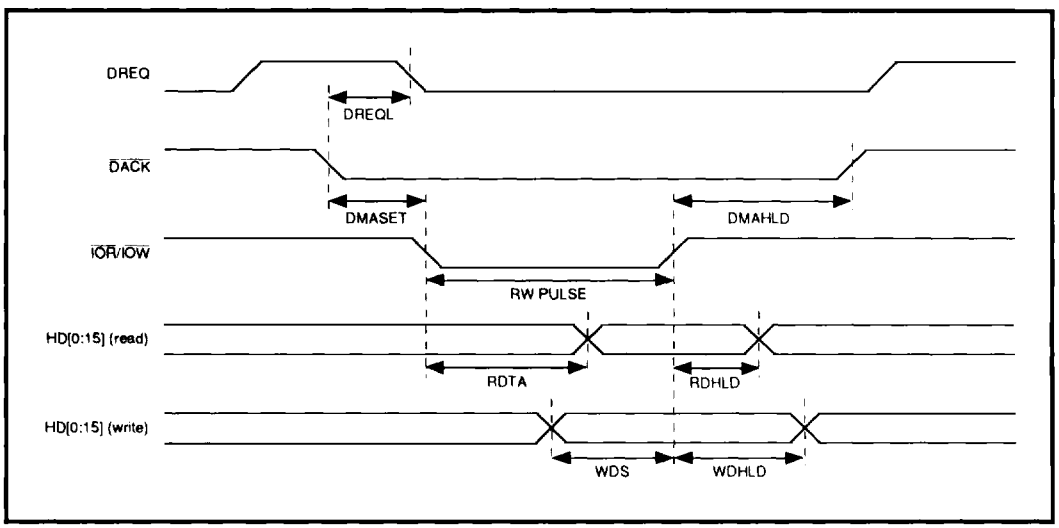


FIGURE 15: Host DMA 8/16-Bit Interface Timing

HOST DMA 8/16-BIT INTERFACE TIMING PARAMETERS (DEMAND MODE) (FIGURE 16)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
DMASET	$\overline{DACK}$ ↓ to $\overline{IOR}$/$\overline{IOW}$ ↓		0			ns
RDTA	$\overline{IOR}$ ↓ to HD [0:15] valid				50	ns
RDHLD	$\overline{IOR}$ ↑ to HD [0:15] tristate		2		25	ns
WDS	HD [0:15] setup to $\overline{IOW}$ ↑		30			ns
WDHLD	HD [0:15] hold from $\overline{IOW}$ ↑		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ low		80			ns
RWPAUSE	$\overline{IOR}$/$\overline{IOW}$ high		40			ns
DREQL	DREQ ↓ from $\overline{IOR}$/$\overline{IOW}$ ↓				40	ns
DMAHLD	$\overline{DACK}$ hold from $\overline{IOR}$/$\overline{IOW}$ ↑		0			ns

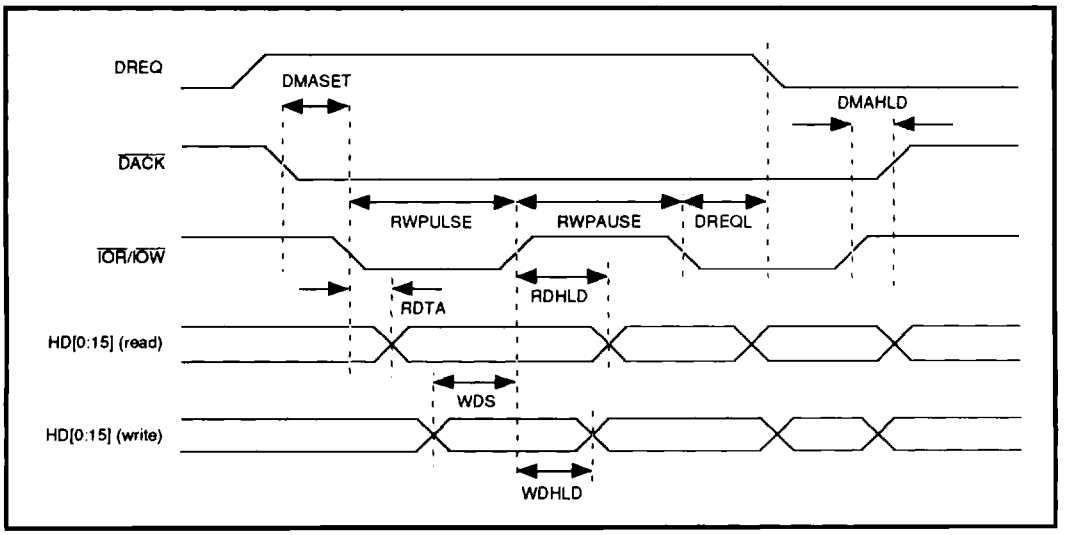


FIGURE 16: Host DMA 8/16-Bit Interface Timing (Demand Mode)

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ELECTRICAL SPECIFICATIONS (continued)

HOST PROGRAMMED I/O TIMING PARAMETERS (FIGURE 16)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
CS16L	$\overline{HCS0}$ ↓, A0:2, A9 ↓, or $\overline{HSC1}$ ↑ to $\overline{IOCS16}$ ↓				25	ns
IOCHL	$\overline{IOR}$/$\overline{IOW}$ ↓ to $\overline{IOCHRDY}$ ↓				30	ns
IOCHTW *	IOCHRDY pulse width		0		5 x BCLK	ns
RDTA	$\overline{IOR}$ ↓ to HD[0:15] valid				50	ns
RDHLD	$\overline{IOR}$ ↑ to HD[0:15] tri-state		2		20	ns
WDS	HD[0:15] setup to $\overline{IOW}$ ↑		30			ns
WDHLD	HD[0:15] hold from $\overline{IOW}$ ↑		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		80			ns
ADRSET	$\overline{HCS0}$, A0:2, A9/$\overline{HCS1}$ setup to $\overline{IOR}$/$\overline{IOW}$ ↓		25			ns
ADRHLD	$\overline{HCS0}$, A0:2, A9,$\overline{HCS1}$ hold, from $\overline{IOR}$/$\overline{IOW}$ ↑		5			ns

* Maximum specification applies when Auto Wait State Generation is disabled (Register 40H, Bit 2 is reset)

RESET ASSERTION TIMING PARAMETERS (FIGURE 17)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Trpwl	$\overline{RST}$ pulse width low	Not power on reset	500			ns
		Power on reset	7.5			µs

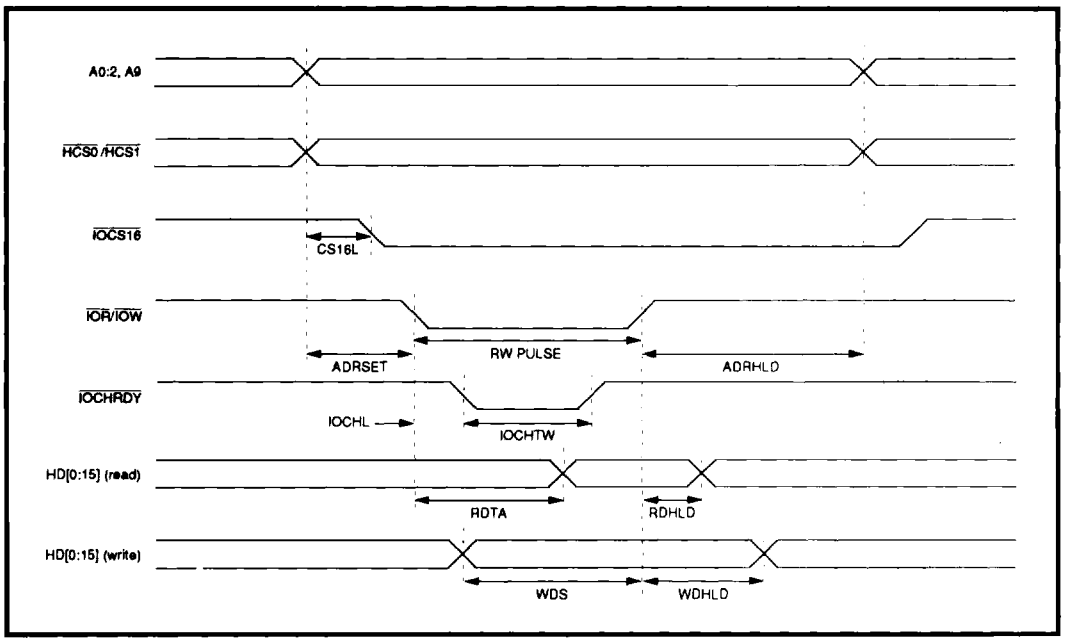
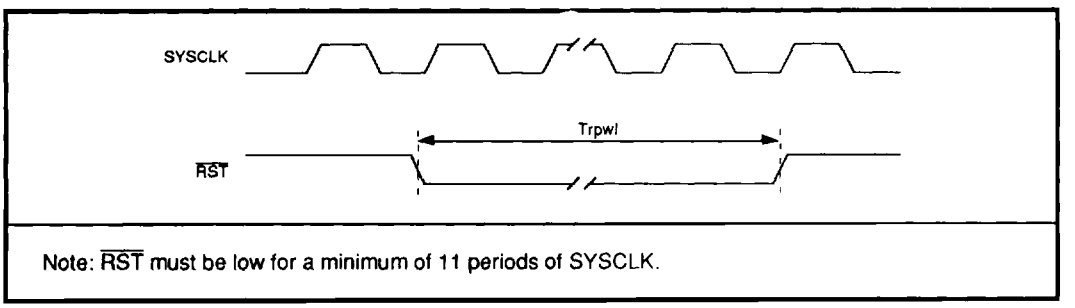


FIGURE 16: Host Programmed I/O 8/16-Bit Timing



Note: $\overline{RST}$ must be low for a minimum of 11 periods of SYSCLK.

FIGURE 17: RESET Assertion Timing

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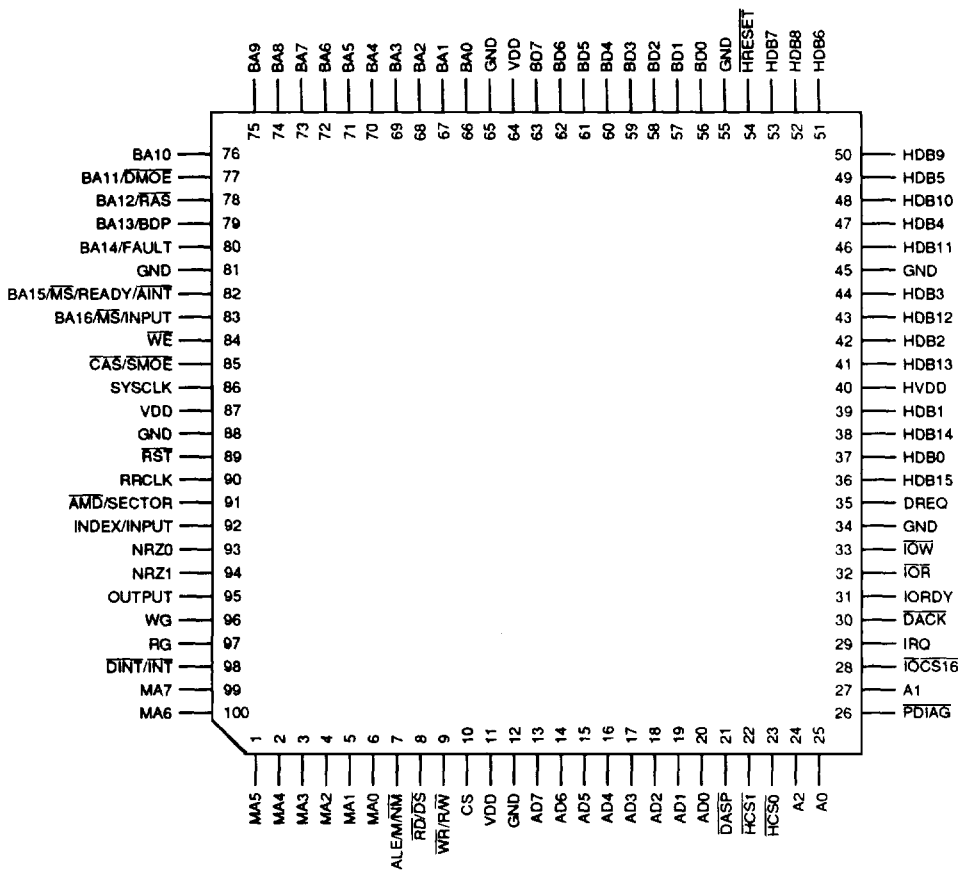
SSI 32C9001
PC-AT Combo Controller
With Reed Solomon, 48 Mbit/s

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914